SDFE-4

Symmetrical DSL Front End, 4 Channels

PEF 24624, V1.1

System Description

Wired Communications

Infineon technologies

Never stop thinking.

User's Manual
CONFIDENTIAL
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1 Overview

The SDFE-4 implements all functions of a 4-channel symDSL[1)] front end (SHDSL, SDSL, HDSL2, HDSL4, HDSL and 2B1Q-SDSL supported) including the *M*-pair mode according to ITU-T G.991.2 and ITU-T G.shdsl.bis. This device offers the capability to run the different symDSL services in parallel and is optimized for the requirements of a TDM system.

Note: For packet data based systems Infineon offers its 16 channel symDSL device Socrates-16bis.

Payload data rates from 144 kbit/s up to 6392 kbit/s with 8 kbit/s granularity per channel are supported.

The following functions are integrated:

- Analog Front End including integrated Line Driver
- Digital Signal Processing Circuit (Data Pump)
- Line Probing according to ITU-T G.shdsl.bis
- Line Prequalification Support
- Flexible setting of PSD shaping
- S(H)DSL over POTS
- SRAM for complete firmware integrated
- 4 x HDLC Controller for EOC
- Serial Data Interface (dedicated interface for each symDSL channel, various bus modi supported)
- *M*-pair functionality fully integrated
- *M*-pair mode with on chip delay compensation (no external memory required)
- One Serial Microcontroller Interface for all 4 channels

The SDFE-4 is interoperable with the Infineon S(H)DSL chips Socrates (PEB 22622), Socrates-4 (PEF 24622), Socrates-U (PEF 22623) and the Socrates-bis family and all other standard compliant symDSL transceivers from third party vendors.

The Serial Data Interface, i.e. TDM or DSL3 transfers data from/to the digital side to/from the loop interface.

Synchronous and plesiochronous data transfer on the symDSL line is possible.

The symDSL front end is based on the highly sophisticated TC PAM transmission technology.
The modulation format for S(H)DSL[2)] uses PAM with 3 information bits per symbol and a 16-level coded constellation from 192 kbit/s up to 2312 kbit/s payload data rate. The SDFE-4 supports 144 kbit/s up to 3832 kbit/s with 3 information bits per symbol. 2, 4 and 5 information bits per symbol modulation is also possible resulting in a payload data rate

1) symDSL stands for symmetrical DSL supporting ETSI TS 101 524 (SDSL), ITU-T G.991.2 (SHDSL), ITU-T G.shdsl.bis (SHDSL bis), ITU-T G.991.1 (HDSL), ETSI TS 101 135 (HDSL), T1E1.4/2001-006R3 (HDSL2/ HDSL4) and 2B1Q-SDSL

2) S(H)DSL stands for ETSI TS 101 524, ITU-T G.991.2 and ITU-T G.shdsl.bis

from 144 kbit/s up to 2552 kbit/s, 144 kbit/s up to 5112 kbit/s or 144 kbit/s up to 6392 kbit/s respectively.

The data pump supports N x 64 kbit/s plus framing where N stands for 2 to 39 B-channels (64 kbit/s-channels) for 2 information bits per symbol, 2 to 59 for 3 information bits per symbol, 2 to 79 for 4 information bits per symbol and 2 to 99 for 5 information bits per symbol.

Additional Z-bits are provided, carrying e.g. a 16 kbit/s D-channel for signalling and a 8 kbit/s channel suitable for framing and performance monitoring of the loop. The Z-bit capacity can be set in steps of 8 kbit/s.

High integration and low power dissipation make the SDFE-4 ideal for high density DSLAM, DLC and Central Office linecards as well as for T1/E1 replacement, fractional T1/E1 applications and regenerator applications.

Duplex Transmission is achieved by using adaptive echo cancellation that removes images of the transmit signal from the receive signal.

Trellis encoding and Viterbi decoding in conjunction with a Tomlinson precoder improve performance against channel noise and achieve a significant increase in loop length.

A high linear Analog/Digital converter in the receiver combined with equalizer and adaptive filtering reproduce the original transmit data.

The flexibility of the device allows identical external circuitry including crystal for all data rates and signal constellations (bits per symbol).

This document describes

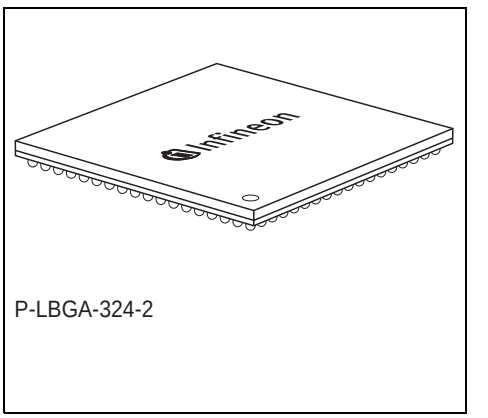
- the pinning of the chip set
- the features (functional description)
- the interfaces
- the electrical characteristics
- the package

Programming of the device and the description of the message-based device controller interface is described in the User' Manual - Programmers Reference Manual. Layout Requirements and board specific needs are described in the Solution Guide.

SDFE-4 PEF 24624
Symmetrical DSL Front End, 4 Channels

V1.1

1.1 Features



P-LBGA-324-2

- Fully integrated 4 channel transceiver solution (DSP, AFE and Line Driver)
- Serial Data Interface, one per channel
- *M*-pair mode fully integrated
- SHDSL-, SDSL, 2B1Q-SDSL, HDSL, HDSL2 and HDSL4-framing supported
- Either SHDSL- and HDSL-framing or SHDSL-, HDSL2- and HDSL4-framing can be mixed between channels
- Analog frontend and integrated Line Driver for 4 channels in one single package
- Integrated hybrid which adapts automatically to the real line conditions
- In Compliance with:
  - ETSI SDSL (ETSI TS 101 524)
  - ITU G.shdsl (ITU-T G.991.2)
  - ITU G.shdsl.bis (ITU-T G.shdsl.bis)
  - ANSI HDSL2/HDSL4 (T1E1.4/2001-006R3)
  - HDSL (ETSI TS 101 135, ITU-T G.991.1)
  - 2B1Q-SDSL
- Interoperable with Infineon S(H)DSL Socrates and Socrates-bis family and other standard compliant symDSL transceivers
- Integrated Bit Error Tester
- One Serial Controller Interface for all 4 chanels
- Power Supply:
  - Digital Part: + 1.8 V
  - Analog Part: + 3.3 V
  - Pads: + 3.3 V
- Fully autonomous operation including *M*-pair mode handled by integrated controller
- ITU G.hs (ITU-T G.994.1) support
- Digital Inputs and Outputs TTL compatible

Type	Package
SDFE-4 (PEF 24624)	P-LBGA-324-2

- Power dissipation below 400 mW per symDSL channel
- Only passive external components required
- API driver including firmware

Modes

- Line Termination Unit (LTU, STU-C), Network Termination Unit (NTU, STU-R), Regenerator Unit COT (SRU-C) and Regenerator Unit RT (SRU-R)
- Analog, digital and remote loop backs

Loop Interface

- Asymmetric PSDs according to ITU-T G.shdsl.bis Annex A and B fully supported without external line driver
- Transmitting up to16.5 dBm line power
- Software configured operating speed at any payload bitrate between 144 kbit/s and 6392 kbit/s[1)] (5 information bits per symbol) with a single crystal as reference clock and without the need of any hardware change
- Highly sophisticated TC PAM line coding
- 2B1Q line code selectable for 2B1Q-SDSL and HDSL interoperability
- Distances of more than 25 kft can be achieved on 26 AWG (0.4 mm) cable. For detailed information please refer to Infineon's Performance Report.
- Programmable Framer
- Synchronous or plesiochronous (bit stuffing) data transfer possible
- Spectral compatible with all existing services
- Two, three, four or five bits per symbol TC PAM
- Adaptive echo cancellation and equalization
- Warm start capability (< 500 ms)
- Capable of transmission over ETSI TS 101 135, ITU-T G.991.2, ITU-T G.shdsl.bis Annex A/B and ANSI HDSL test loops
- Line Probing according to ITU-T G.shdsl.bis
- Line Prequalification
- Fully digital clock recovery
- Tolerates input jitter according to G.823/G.824. Jitter transfer function is better than specified in I.430/I.431.
- Integrated RAM for start-up procedure
- Coefficients of all filters readable and writable for fast bitrate change, i.e. only warm start required after change of bitrate
- Loop delay measurement
- Serial Data Interface
- Supported clocks in TDM mode:
- 1.544 MHz clock, 193 bits / 125 µs frame

1) In transparent mode transmission at any rate between 152 kbit/s and 6400 kbit/s in increments of 8 kbit/s is possible.

- 2.048 MHz clock, 256 bits / 125 µs frame
- 2.312 MHz clock, 289 bits / 125 µs frame
- 4.096 MHz clock, 512 bits / 125 µs frame
- 8.192 MHz clock, 1024 bits / 125 µs frame
- 16.384 MHz clock, 2048 bits / 125 µs frame
- Master/Slave configuration programmable independent of selected mode (LTU/NTU)
- Frame start programmable in TDM bit granularity
- Generic Bit Serial Mode

Microcontroller Interface

- One Serial Control Interface for all 4 channels comprising of three pins
- Configuration and maintenance of the SDFE-4 by messages

4 HDLC Controllers for EOC

- 128 byte FIFO for transmit and receive direction per channel

Supported Standards

The following table summarizes the supported standards of the SDFE-4. The reference model is shown in **Figure 39**.

Table 1 Supported Standard of the SDFE-4

Block of the Reference Modell	Name	Standard
TPS-TC	STM including *M*-pair	ETSI TS 101 524, ITU-T G.991.2, ITU-T G.shdsl.bis
PMD	ETSI SDSL	ETSI TS 101 524
PMD	ITU G.shdsl	ITU-T G.991.2
PMD	ITU G.shdsl.bis	ITU-T G.shdsl.bis
PMD	ANSI HDSL2/ HDSL4	ANSI T1E1.4/2001-006
PMD	HDSL	ETSI TS 101 135, ITU-T G.991.1
PMD	2B1Q-SDSL	

1.2 Logic Symbol

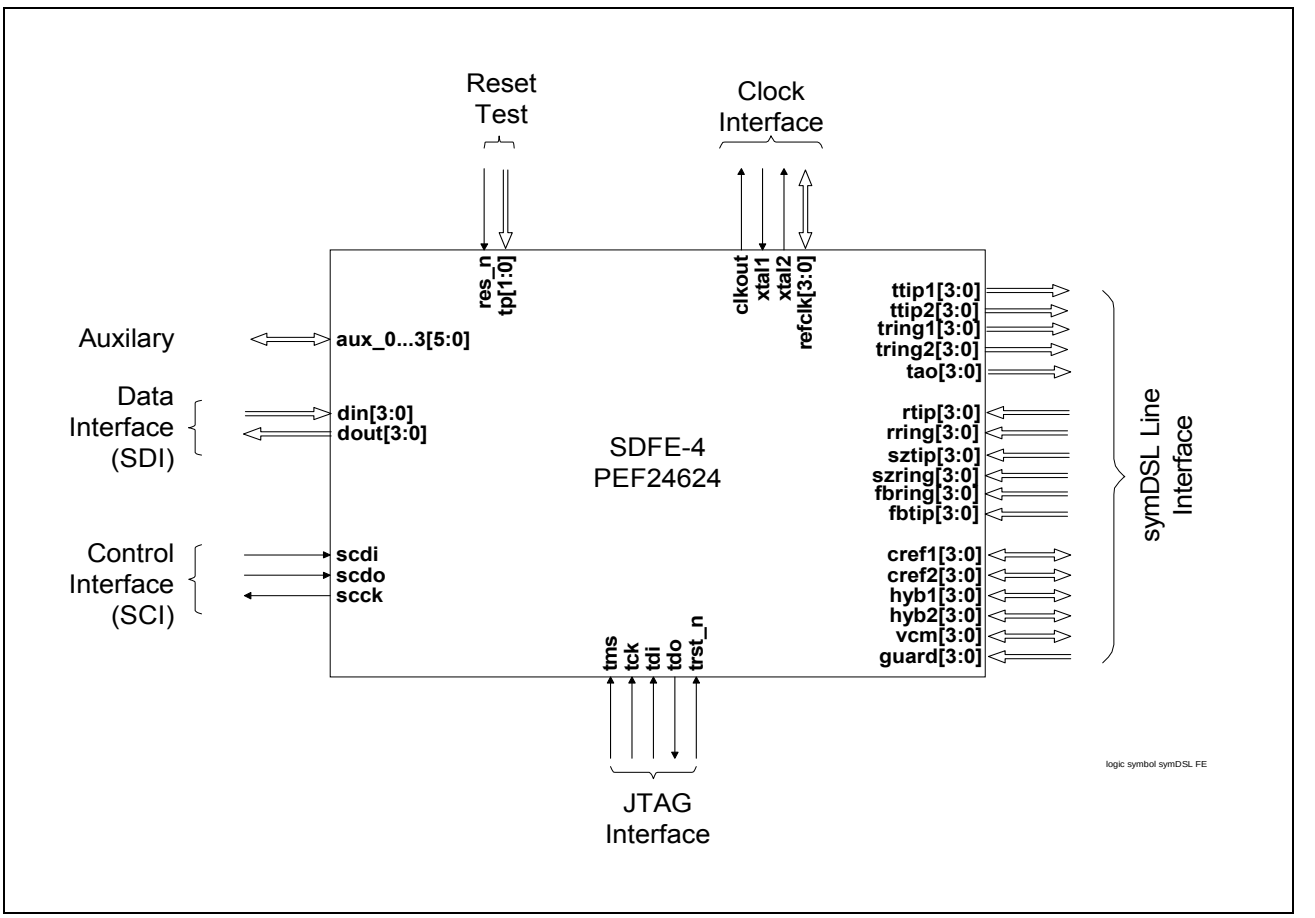


Figure 1 Logic Symbol

1.3 Typical Applications

SDFE-4 is designed to handle up to 4 symDSL lines. The following typical applications can be addressed:

- N-channel PCM-x systems
- Extended range full and fractional T1/E1
- Digital Loop Carrier (DLC) systems
- ISDN Primary rate access replacement
- Mobile Infrastructure (RNC, Node B)
- RITL and WLL systems
- SDH and SONET termination
- Leased line services
- Frame Relay services

2 Pin Description

2.1 External Signal List

2.1.1 Ball Diagram

	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	VSSA	TTIP1_0	TRING1_0	VCM_0	VSSA	TTIP1_1	TRING1_1	VCM_1	VSSA	VSSA	VCM_2	TRING1_2	TTIP1_2	VSSA	VCM_3	TRING1_3	TTIP1_3	VSSA
2	VDDA	TTIP2_0	TRING2_0	VDDA	VDDA	TTIP2_1	TRING2_1	VDDA	VDDA	VDDA	VDDA	TRING2_2	TTIP2_2	VDDA	VDDA	TRING2_3	TTIP2_3	VDDA
3	VSSA	SZTIP_0	SZRING_0	VSSA	VSSA	SZTIP_1	SZRING_1	VSSA	VSSA	VSSA	VSSA	SZRING_2	SZTIP_2	VSSA	VSSA	SZRING_3	SZTIP_3	VSSA
4	CREF1_0	RTIP_0	RRING_0	VDDA	VDDA	RTIP_1	RRING_1	VDDA	VDDA	VDDA	VDDA	RRING_2	RTIP_2	VDDA	VDDA	RRING_3	RTIP_3	CREF1_3
5	CREF2_0	HYB1_0	HYB2_0	VSSA	VSSA	HYB1_1	HYB2_1	VSSA	VSSA	VSSA	VSSA	HYB2_2	HYB1_2	VSSA	VSSA	HYB2_3	HYB1_3	CREF2_3
6	VSSA	FBTIP_0	FBRING_0	VDDA	VDDA	FBTIP_1	FBRING_1	VDDA	VDDA	VDDA	VDDA	FBRING_2	FBTIP_2	VDDA	VDDA	FBRING_3	FBTIP_3	VSSA
7	CREF1_1	TAO_0	TAO_1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	TAO_2	TAO_3	CREF1_2
8	CREF2_1	GUARD_0	GUARD_1	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	GUARD_2	GUARD_3	CREF2_2
9	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
10	XTAL2	XTAL1	CLKOUT	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA
11	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD
12	AUX_1_3	TP2	AUX_1_2	VDDP	VDDP	VDDP	VDDP	VDDP	VDDP	NC	VDDP	VDDP	VDDP	VDDP	AUX_2_5	AUX_3_4	TDI	TMS
13	RES_N	AUX_1_1	VDDD	VDDD	VDDD	VDDD	VDDD	VDDP	VDDP	VDDP	VDDP	VDDP	VDDP	VDDP	VDDP	VDDP	AUX_3_5	TRST_N
14	AUX_1_0	TP1	DOUT_1	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDP	AUX_2_4	TDO	TCK
15	AUX_0_3	REFCLK_1	DIN_1	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VDDD	VDDP	REFCLK_3	AUX_3_3	AUX_3_2
16	AUX_0_2	AUX_0_5	AUX_0_4	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDP	DOUT_3	AUX_3_1	AUX_3_0
17	AUX_0_1	REFCLK_0	AUX_0_0	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	DOUT_2	REFCLK_2	AUX_2_0	AUX_2_3	DIN_3
18	DOUT_0	DIN_0	SCDI	SCCK	SCDO	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	DIN_2	AUX_1_5	AUX_1_4	AUX_2_1	AUX_2_2

RES_N: $\overline{\text{RES}}$
TRST_N: $\overline{\text{TRST}}$

Figure 2 Pin Diagram (Top View)

2.1.2 Ball Definitions and Functions

Table 2 Analog Front End[1)]

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
					Analog Front End, Channel 0
V4	CREF1_0	I/O			V_{DD} Reference Voltage
V5	CREF2_0	I/O			V_{SS} Reference Voltage
U4	RTIP_0	I			Receive Tip input
T4	RRING_0	I			Receive Ring input
R1	VCM_0	I/O			Midband for Line Driver
U1	TTIP1_0	O			Transmit Tip, Line driver 1 output
U2	TTIP2_0	O			Transmit Tip, Line driver 2output
T1	TRING1_0	O			Transmit Ring, Line driver 1 output
T2	TRING2_0	O			Transmit Ring, Line driver 2 output
U3	SZTIP_0	I			Synthesized Impedance Input Tip
T3	SZRING_0	I			Synthesized Impedance Input Ring
T6	FBRING_0	I			Line Driver Feed-Back Input Ring
U6	FBTIP_0	I			Line Driver Feed-Back Input Tip
U5	HYB1_0	I/O			Hybrid (Connect to hybrid circuit)
T5	HYB2_0	I/O			Hybrid (Connect to hybrid circuit
U7	TAO_0	O			Analog output For test purposes only Has to be left open during normal operation
U8	GUARD_0	I			Guard, has to be connected to quiet V_{SS}
Analog Front End, Channel 1					
V7	CREF1_1	I/O			V_{DD} Reference Voltage
V8	CREF2_1	I/O			V_{SS} Reference Voltage
N4	RTIP_1	I			Receive Tip input
M4	RRING_1	I			Receive Ring input
L1	VCM_1	I/O			Midband for Line Driver
N1	TTIP1_1	O			Transmit Tip, Line driver 1 output

Table 2 Analog Front End[1)] (cont'd)

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
N2	TTIP2_1	O			Transmit Tip, Line driver 2 output
M1	TRING1_1	O			Transmit Ring, Line driver 1 output
M2	TRING2_1	O			Transmit Ring, Line driver 2 output
N3	SZTIP_1	I			Synthesized Impedance Input Tip
M3	SZRING_1	I			Synthesized Impedance Input Ring
M6	FBRING_1	I			Line Driver Feed-Back Input Ring
N6	FBTIP_1	I			Line Driver Feed-Back Input Tip
N5	HYB1_1	I/O			Hybrid (Connect to hybrid circuit)
M5	HYB2_1	I/O			Hybrid (Connect to hybrid circuit
T7	TAO_1	O			Analog output For test purposes only Has to be left open during normal operation
T8	GUARD_1	I			Guard, has to be connected to quiet V_{SS}
Analog Front End, Channel 2					
A7	CREF1_2	I/O			V_{DD} Reference Voltage
A8	CREF2_2	I/O			V_{SS} Reference Voltage
F4	RTIP_2	I			Receive Tip input
G4	RRING_2	I			Receive Ring input
H1	VCM_2	I/O			Midband for Line Driver
F1	TTIP1_2	O			Transmit Tip, Line driver 1 output
F2	TTIP2_2	O			Transmit Tip, Line driver 2 output
G1	TRING1_2	O			Transmit Ring, Line driver 1 output
G2	TRING2_2	O			Transmit Ring, Line driver 2 output
F3	SZTIP_2	I			Synthesized Impedance Input Tip
G3	SZRING_2	I			Synthesized Impedance Input Ring
G6	FBRING_2	I			Line Driver Feed-Back Input Ring
F6	FBTIP_2	I			Line Driver Feed-Back Input Tip
F5	HYB1_2	I/O			Hybrid (Connect to hybrid circuit)
G5	HYB2_2	I/O			Hybrid (Connect to hybrid circuit

Table 2 Analog Front End[1)] (cont'd)

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
C7	TAO_2	O			Analog output For test purposes only Has to be left open during normal operation
C8	GUARD_2	I			Guard, has to be connected to quiet V_{SS}
Analog Front End, Channel 3					
A4	CREF1_3	I/O			V_{DD} Reference Voltage
A5	CREF2_3	I/O			V_{SS} Reference Voltage
B4	RTIP_3	I			Receive Tip input
C4	RRING_3	I			Receive Ring input
D1	VCM_3	I/O			Midband for Line Driver
B1	TTIP1_3	O			Transmit Tip, Line driver 1 output
B2	TTIP2_3	O			Transmit Tip, Line driver 2 output
C1	TRING1_3	O			Transmit Ring, Line driver 1 output
C2	TRING2_3	O			Transmit Ring, Line driver 2 output
B3	SZTIP_3	I			Synthesized Impedance Input Tip
C3	SZRING_3	I			Synthesized Impedance Input Ring
C6	FBRING_3	I			Line Driver Feed-Back Input Ring
B6	FBTIP_3	I			Line Driver Feed-Back Input Tip
B5	HYB1_3	I/O			Hybrid (Connect to hybrid circuit)
C5	HYB2_3	I/O			Hybrid (Connect to hybrid circuit
B7	TAO_3	O			Analog output For test purposes only Has to be left open during normal operation
B8	GUARD_3	I			Guard, has to be connected to quiet V_{SS}

Table 2 Analog Front End[1)] (cont'd)

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
					Crystal
U10	XTAL1	I			Oscillator or 20.48 MHz input (± 65 ppm in all timing modes except internal timed and ± 32 ppm in internal timed mode)
V10	XTAL2	O			Oscillator output
T10	CLKOUT	O			20.48 MHz output

1) All pins of the Analog Front End are anlog pins, there drivers and pullup/pulldown description as used in other chapters is not applicable

Table 3 Reset and Test

Ball No.	Symbol	In[1)]/Out	Driver	Pullup/ -down	Function
V13	RES	I			Reset
U14	TP1	I			Testpin Has to be connected to V_{SS} during normal operation
U12	TP2	I			Testpin Has to be connected to V_{SS} during normal operation

1) Each input pin without internal pull-up or pull-down resistor must be driven with any logical level according to **Chapter 7.5** when V_{DDP} is applied.

Table 4 Serial Control Interface

Ball No.	Symbol	In[1)]/Out	Driver	Pullup/ -down	Function
T18	SCDI	I			Serial Control Data In
P18	SCDO	O	C		Serial Control Data Out, Reset: '1'
R18	SCCLK	I			Serial Control Interface Clock

1) Each input pin without pull-up or pull-down resistor must be driven with any logical level according to **Chapter 7.5** when V_{DDP} is applied.

Table 5 Serial Data Interface

Ball No.	Symbol	In[1]/Out	Driver	Pullup/ -down	Function
Serial Data Interface, Channel 0					
U18	DIN_0	I		-	Serial Data In
V18	DOUT_0	O_{ts}	C	PUB[2]	Serial Data Out, Reset: 'Z'
U17	REFCLK_0	I/O	C	PUB[2]	Reference Clock (see **Figure 3**), Reset: Input
Serial Data Interface, Channel 1					
T15	DIN_1	I		-	Serial Data In
T14	DOUT_1	O_{ts}	C	PUB[2]	Serial Data Out, Reset: 'Z'
U15	REFCLK_1	I/O	C	PUB[2]	Reference Clock (see **Figure 3**), Reset: Input
Serial Data Interface, Channel 2					
E18	DIN_2	I		-	Serial Data In
E17	DOUT_2	O_{ts}	C	PUB[2]	Serial Data Out, Reset: 'Z'
D17	REFCLK_2	I/O	C	PUB[2]	Reference Clock (see **Figure 3**) Reset: Input
Serial Data Interface, Channel 3					
A17	DIN_3	I		-	Serial Data In
C16	DOUT_3	O_{ts}	C	PUB[2]	Serial Data Out, Reset: 'Z'
C15	REFCLK_3	I/O	C	PUB[2]	Reference Clock (see **Figure 3**) Reset: Input

[1] Each input pin without pull-up or pull-down resistor must be driven with any logical level according to **Chapter 7.5** when V_{DDP} is applied.

[2] Pull-Up activated during initialization only

Table 6 Auxiliary Interface

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
Auxiliary Bus, Channel 0					
U16	AUX_0_[5]	I/O	C	PUB[1)]	
T16	AUX_0_[4]	I/O	C	PUB[1)]	
V15	AUX_0_[3]	I/O	C	PUB[1)]	
V16	AUX_0_[2]	I/O	C	PUB[1)]	
V17	AUX_0_[1]	I/O	C	PUB[1)]	
T17	AUX_0_[0]	I/O	C	PUB[1)]	
Auxiliary Bus, Channel 1					
D18	AUX_1_[5]	I/O	C	PUB[1)]	
C18	AUX_1_[4]	I/O	C	PUB[1)]	
V12	AUX_1_[3]	I/O	C	PUB[1)]	
T12	AUX_1_[2]	I/O	C	PUB[1)]	
U13	AUX_1_[1]	I/O	C	PUB[1)]	
V14	AUX_1_[0]	I/O	C	PUB[1)]	

Table 6 Auxiliary Interface (cont'd)

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
Auxiliary Bus, Channel 2					
D12	AUX_2_[5]	I/O	C	PUB[1)]	
C14	AUX_2_[4]	I/O	C	PUB[1)]	
B17	AUX_2_[3]	I/O	C	PUB[1)]	
A18	AUX_2_[2]	I/O	C	PUB[1)]	
B18	AUX_2_[1]	I/O	C	PUB[1)]	
C17	AUX_2_[0]	I/O	C	PUB[1)]	
Auxiliary Bus, Channel 3					
B13	AUX_3_[5]	I/O	C	PUB[1)]	
C12	AUX_3_[4]	I/O	C	PUB[1)]	
B15	AUX_3_[3]	I/O	C	PUB[1)]	
A15	AUX_3_[2]	I/O	C	PUB[1)]	
B16	AUX_3_[1]	I/O	C	PUB[1)]	
A16	AUX 3 [0]	I/O	C	PUB[1)]	

[1)] Pull-Up activated during initialization only

Note: After reset all pins are configured as inputs. If the Auxiliary Interface is not used and the AUX ports remain configured as input, connect them to '1'.

Table 7 JTAG Interface

Ball No.	Symbol	In/Out	Driver	Pullup/ -down	Function
B12	TDI	I		PUB	Test Data Input
B14	TDO	O	C		Test Data Output Reset: Z, Reset Value activated by $\overline{\text{TRST}}$ reset, not by $\overline{\text{RES}}$ Push-Pull
A12	TMS	I		PUB	Test Mode Select for Boundary Scan
A13	TRST	I		PUB	Test Reset for Boundary Scan A low signal resets the Boundary Scan mode. In normal operation of the chip the boundary scan has to be reset as well. Therefore this pin has either to be connected to pin $\overline{\text{RES}}$ or to ’0’ during normal operation.
A14	TCK	I		PUB	Test Clock for Boundary Scan

Table 8 Not Connected Balls

Ball No.	Handling on Board
J12	Pin not connected, leave open

Table 9 Power Supply

Ball No.	Symbol	Function
A2,D2,E2,H2, J2,K2,L2,P2,R2, V2,D4,E4,H4,J4, K4,L4,P4,R4, D6, E6,H6,J6,K6,L6, P6,R6,D8,E8, F8, G8,H8,J8,K8,L8, M8,N8,P8,R8, A10,B10,C10, D10,E10,F10, G10,H10,J10, K10,L10,M10, N10,P10,R10	V_{DDA}	Supply Voltage for the analog part 3.3 V
M13,N13,P13, R13,T13,E14, F14,G14,H14, J14,K14,L14, M14,N14,P14, R14,E15,E16, F16,G16,H16, J16,K16,L16, M16,N16,P16, R16,F18,G18, H18,J18,K18, L18,M18,N18	V_{DDD}	Supply Voltage for the digital part 1.8 V
E12,F12,G12, H12,K12,L12, M12,N12,P12, R12,C13,D13, E13,F13,G13, H13,J13,K13, L13,D14,D15, D16	V_{DDP}	Supply Voltage for the digital pads 3.3 V
A1,E1,J1,K1, P1,V1,A3,D3, E3,H3,J3,K3,L3,P3,R3, V3,D5,E5,H5,J5, K5,L5,P5,R5,A6,V6,D7,E7, F7, G7,H7,J7,K7,L7, M7,N7,P7,R7, A9,B9,C9,D9,E9,F9,G9,H9,J9,K9,L9,M9,N9 P9,R9,T9,U9,V9	V_{SSA}	Ground for the analog part
A11,B11,C11, D11,E11,F11, G11,H11,J11, K11,L11,M11, N11,P11,R11, T11,U11,V11, F15,G15,H15, J15,K15,L15, M15,N15,P15, R15,F17,G17, H17,J17,K17, L17,M17,N17, P17, R17	V_{SSD}	Ground for the digital part

3 System Integration

3.1 Used Terms

Timing Modes mentioned in this chapter

- Internal Timed means that the transmit baud clock is directly derived from the 20.48 MHz clock (pin XTAL1).
- External Timed means that the transmit baud clock is synchronized to the reference clock input (pin REFCLK as input).
- Loop Timed means that the reference clock is synchronous to the received symDSL frame (pin REFCLK as output).
- TDM Timed means that the transmit baud clock is synchronized to the TDM interface (pin REFCLK as output).

Names for the Clock Modes mentioned in this chapter

The names of the clock modes are composed as follows:

Clock Mode Name:	*u* clock *v_wx_y*
u:	stands for the transceiver or regenerator unit (LTU, NTU, SRU-C or SRU-R)
v:	stands for the clocking mode according to ITU-T G.shdsl.bis (1, 2, 3a or 3b)
w:	stands for the timing mode (I = internal timed, E = external timed, L = loop timed or T = TDM timed)
x:	stands for the Serial Data Interface mode (D = DSL3, T = TDM, B = Bit Serial)
y:	stands for the TDM interface configuration (only valid for *x* == T) (S = Split or A = Aligned)
	Split: TDM receive clock independent from TDM transmit clock
	Aligned: TDM transmit clocks (PCLK_#, TFSC_#) looped back internally to the TDM receive clocks (RCLK_#, RFSC_#). Receive clock in phase with transmit clocks.

3.2 Clocking Scheme

3.2.1 Reference Clock

The clock reference options described in this chapter apply to the reference clock architecture described in the ITU-T G.991.2 standard and are described in more detail in the following chapters.

Figure 3 shows a simplified SHDSL reference model and **Table 10** lists the timing modes standardized in ITU-T G.991.2.

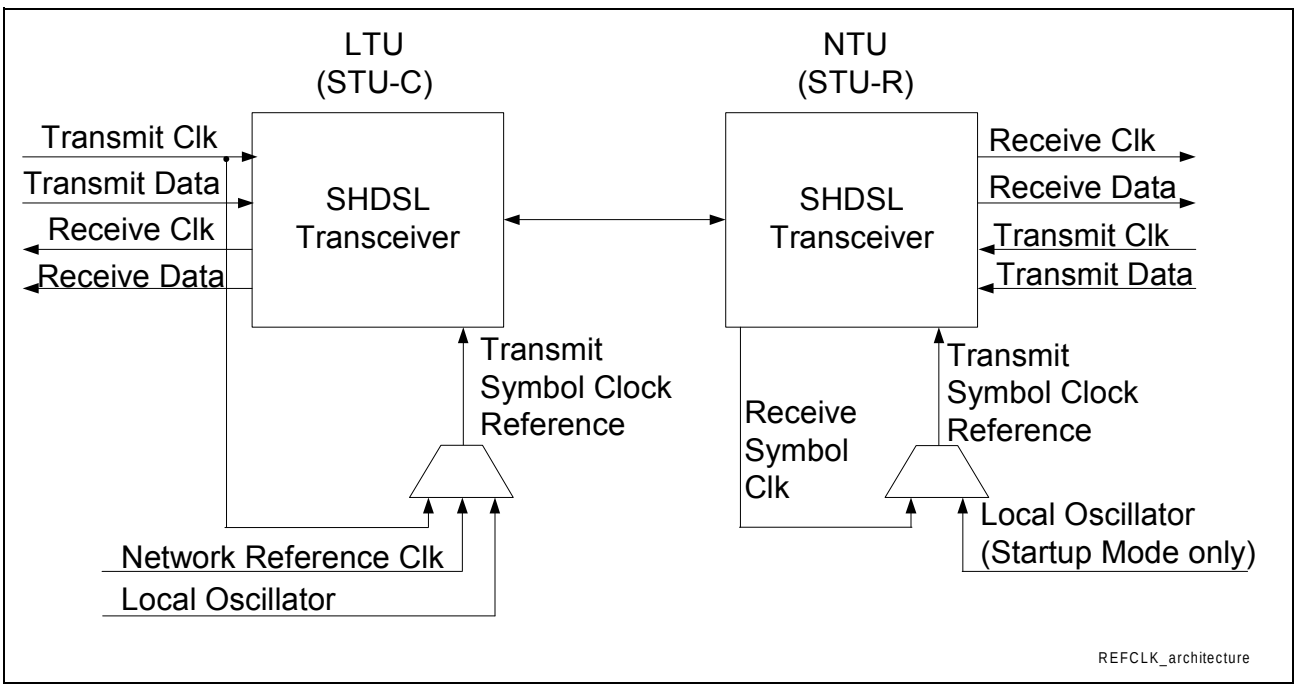


Figure 3 Reference Clock Architecture Customer Interface Clock

Table 10 Clock Synchronization Configuration

Timing Mode#	LTU(STU-C) Symbol Clock Reference	NTU(STU-R) Symbol Clock Reference	Example Application	Mode
1	Local oscillator	Received symbol clock	"Classic" HDSL	Plesiochronous
2	Network reference clock	Received symbol clock	"Classic" HDSL with embedded timing reference	Plesiochronous with timing reference
3a	Transmit data clock or network reference clock	Received symbol clock	Main application	Synchronous
3b	Transmit data clock	Received symbol clock	Synchronous downstream and bit-stuffed upstream	downstream: synchronous upstream: plesiochronous

3.2.1.1 Reference Clock Frequencies

For the reference clock pin a wide range of frequencies can be programmed. **Table 11** shows the possible reference clock frequencies when pin REFCLK is programmed to input and **Table 12** for pin REFCLK programmed as output.

Table 11 Supported Input Frequencies of Pin REFCLK

Frequency	Minimum Low/High Phase
8 kHz	One 60 MHz period
1536 kHz	One 60 MHz period
1544 kHz	One 60 MHz period
2048 kHz	One 60 MHz period
4096 kHz	One 60 MHz period
8192 kHz	One 60 MHz period
15.36 MHz	One 60 MHz period
20.48 MHz	One 60 MHz period

Table 12 Supported Output Frequencies of Pin REFCLK

Frequency[1)]	Duty Cycle	Clock Source
8 kHz	40-60 to 60-40	Rx Data Clk, Rx Symbol Clk or 20.48 MHz
1536 kHz	40-60 to 60-40	Rx Data Clk
1544 kHz	40-60 to 60-40	Rx Data Clk
2048 kHz	40-60 to 60-40	Rx Data Clk
4096 kHz	40-60 to 60-40	Rx Data Clk
8192 kHz	40-60 to 60-40	Rx Data Clk
15.36 MHz	40-60 to 60-40	Rx Data Clk
19.44 MHz	40-60 to 60-40	Rx Data Clk
20.48 MHz	40-60 to 60-40	Rx Data Clk
24.576 MHz	40-60 to 60-40	Rx Data Clk

1) An intrinsic jitter of ± 8.14 ns

3.3 Supported Clock and Interface Modes

3.3.1 Supported Clock and Interface Modes for STU-C

Table 13 Settings of Clock Modes, STU-C

Clock Mode [1]	Clock Mode Name: LTU Clock ...	SD [2] Mode	Line Tx [3] synchr. Baud Ref.	Line Tx [3] synchr. Frame Sync	Line Rx [4] sync. Frame Sync	REFCLK Dir.	REFCLK Source	SD Rx Frame/ data clock Source	Figure #
1	1_ID	DSL3	Local Osci.	Plesio.	Plesio.	O	Local Osci.	Rx Frame	Figure 4
	1_IT_A	TDM	Local Osci.	Plesio.	Plesio.	O	Local Osci.	SD Tx	Figure 5
	1_IT_S	TDM	Local Osci.	Plesio.	Plesio.	O	Local Osci.	Rx Frame	Figure 6
	1_IB	Bit Serial	Local Osci.	Plesio.	Plesio.	O	Local Osci.	Rx Frame	Figure 7
2	2_ED	DSL3	NTR	Plesio.	Plesio.	I	NTR	Rx Frame	Figure 8
	2_ET_A	TDM	NTR	Plesio.	Plesio.	I	NTR	SD Tx	Figure 9
	2_ET_S	TDM	NTR	Plesio.	Plesio.	I	NTR	Rx Frame	Figure 10
	2_EB	Bit Serial	NTR	Plesio.	Plesio.	I	NTR	Rx Frame	Figure 11
3a	3a_TD	DSL3	TDM	Sync.	Sync.	O	TDM	Rx Frame	Figure 12
	3a_TT_A	TDM	TDM	Sync.	Sync.	O	TDM	SD Tx	Figure 13
	3a_TB	Bit Serial	TDM	Sync.	Sync.	O	TDM	Rx Frame	Figure 14

Table 13 Settings of Clock Modes, STU-C (cont'd)

Clock Mode [1]	Clock Mode Name: LTU Clock ...	SD[2] Mode	Line Tx[3] synchr.		Line Rx[4] sync.	REFCLK		SD Rx Frame/ data clock	Figure #
			Baud Ref.	Frame Sync	Frame Sync	Dir.	Source	Source	
3b	3b_TD	DSL3	TDM	Sync.	Plesio.	O	TDM	Rx Frame	Figure 15
	3b_TT_A	TDM	TDM	Sync.	Plesio.	O	TDM	SD Tx	Figure 16
	3b_TT_S	TDM	TDM	Sync.	Plesio.	O	TDM	Rx Frame	Figure 17
	3b_TB	Bit Serial	TDM	Sync.	Plesio.	O	TDM	Rx Frame	Figure 18

[1] **Clock Mode according to ITU-T G.shdsl.bis**

[2] SD stands for Serial Data Interface

[3] Tx stands for the transmit direction and refers to the line interface

[4] Rx stands for the receive direction and refers to the line interface

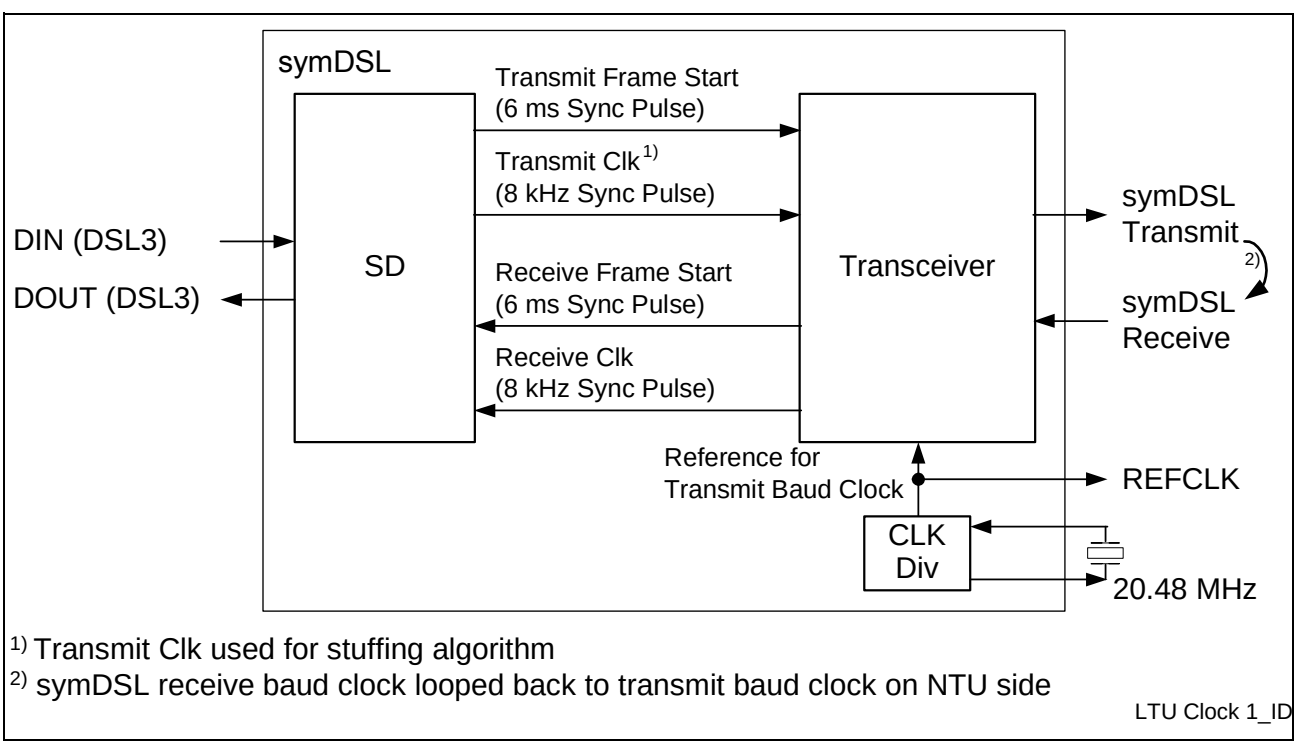


Figure 4 LTU Clock 1_ID, Clock Propagation

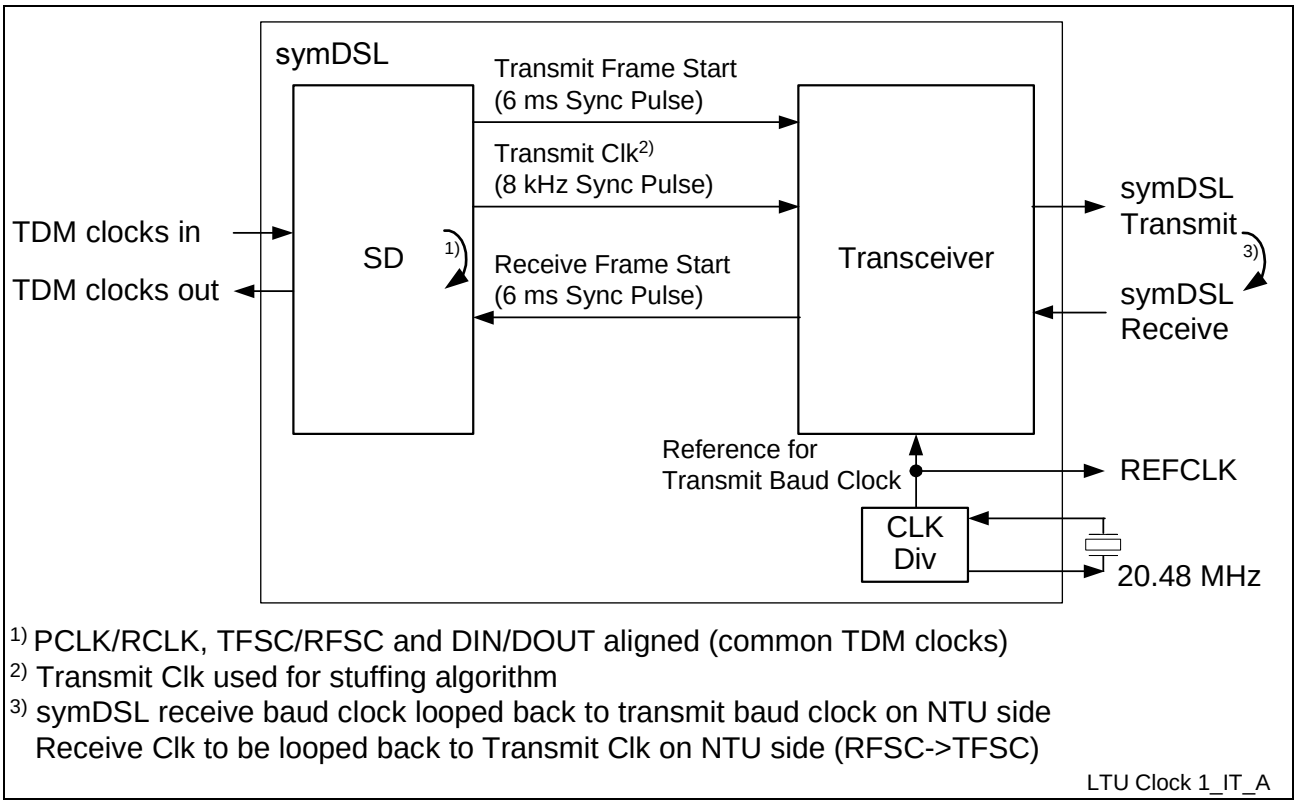


Figure 5 LTU Clock 1_IT_A, Clock Propagation

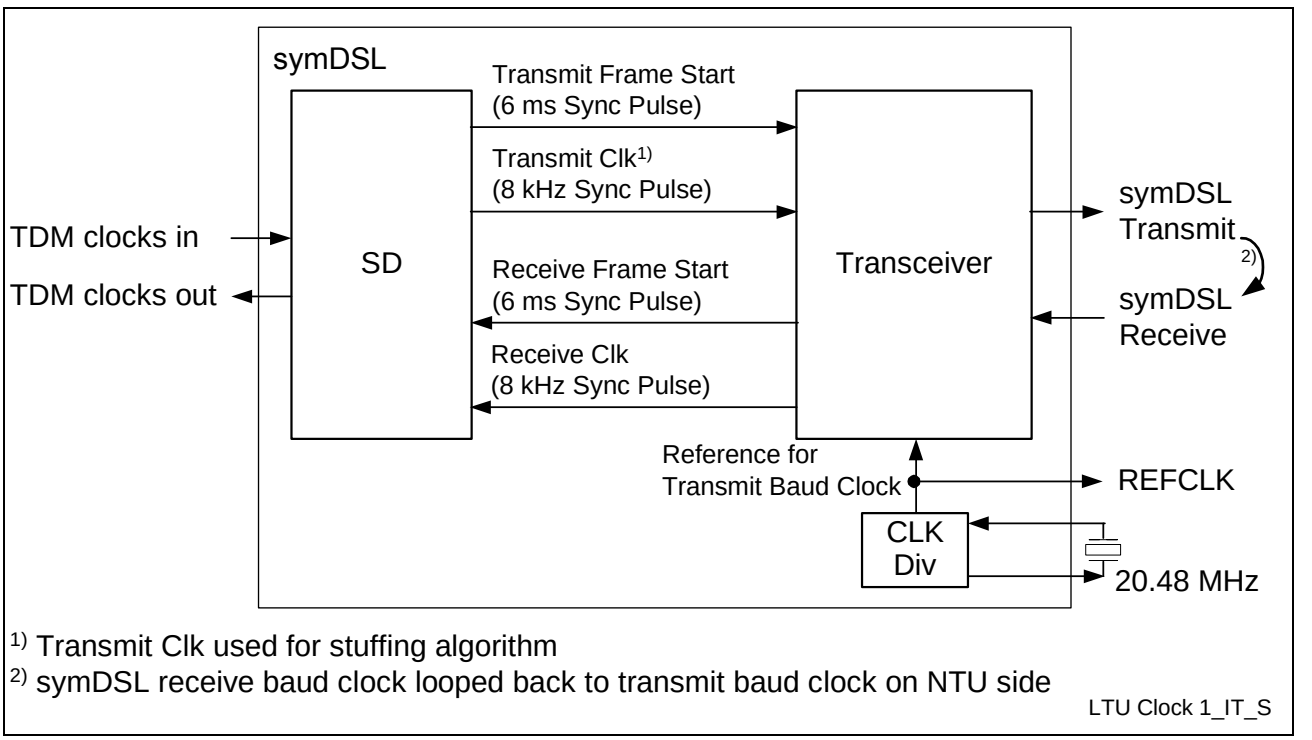


Figure 6 LTU Clock 1_IT_S, Clock Propagation

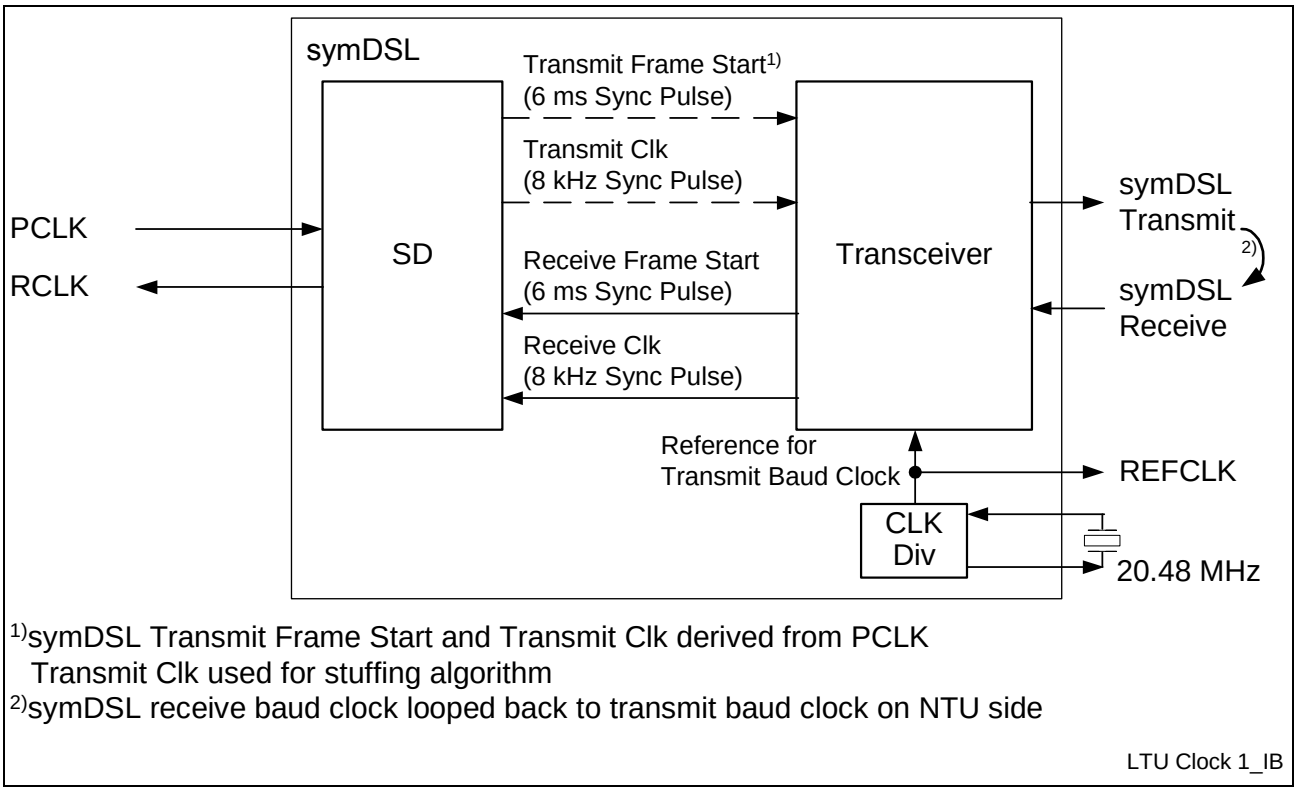


Figure 7 LTU Clock 1_IB, Clock Propagation

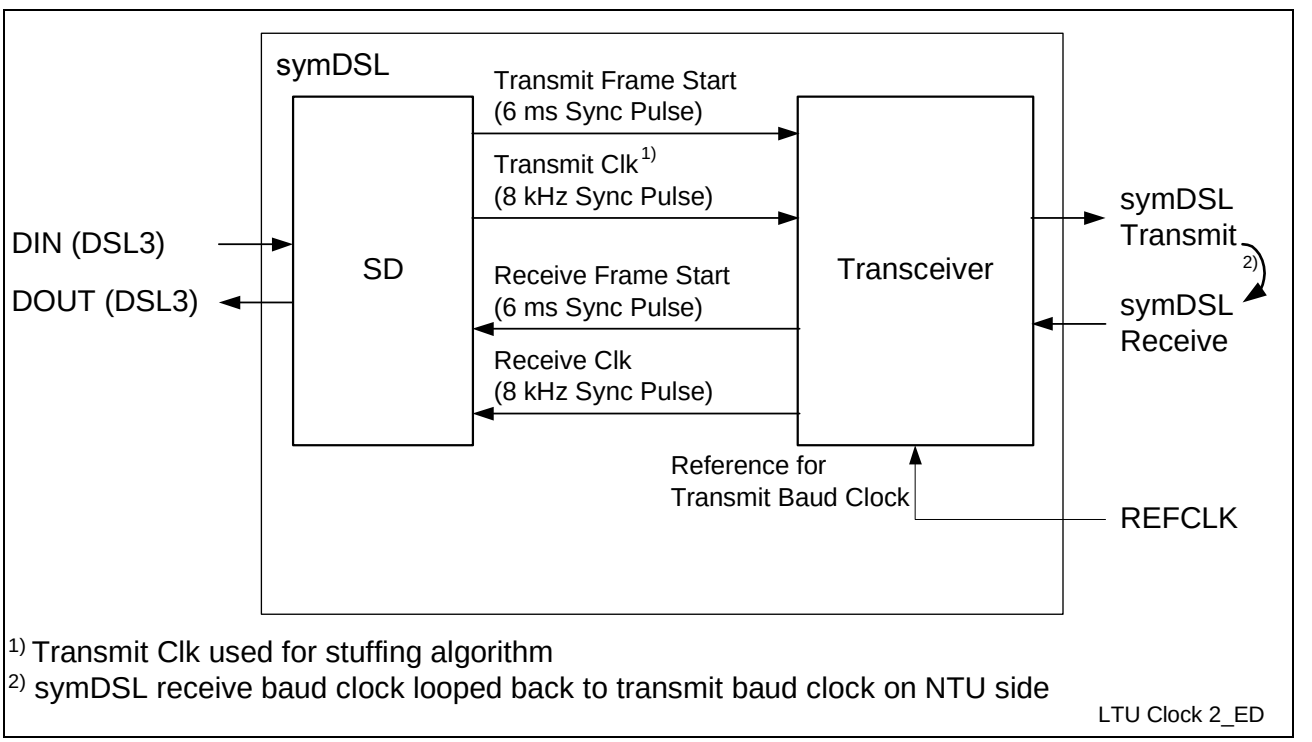


Figure 8 LTU Clock 2_ED, Clock Propagation

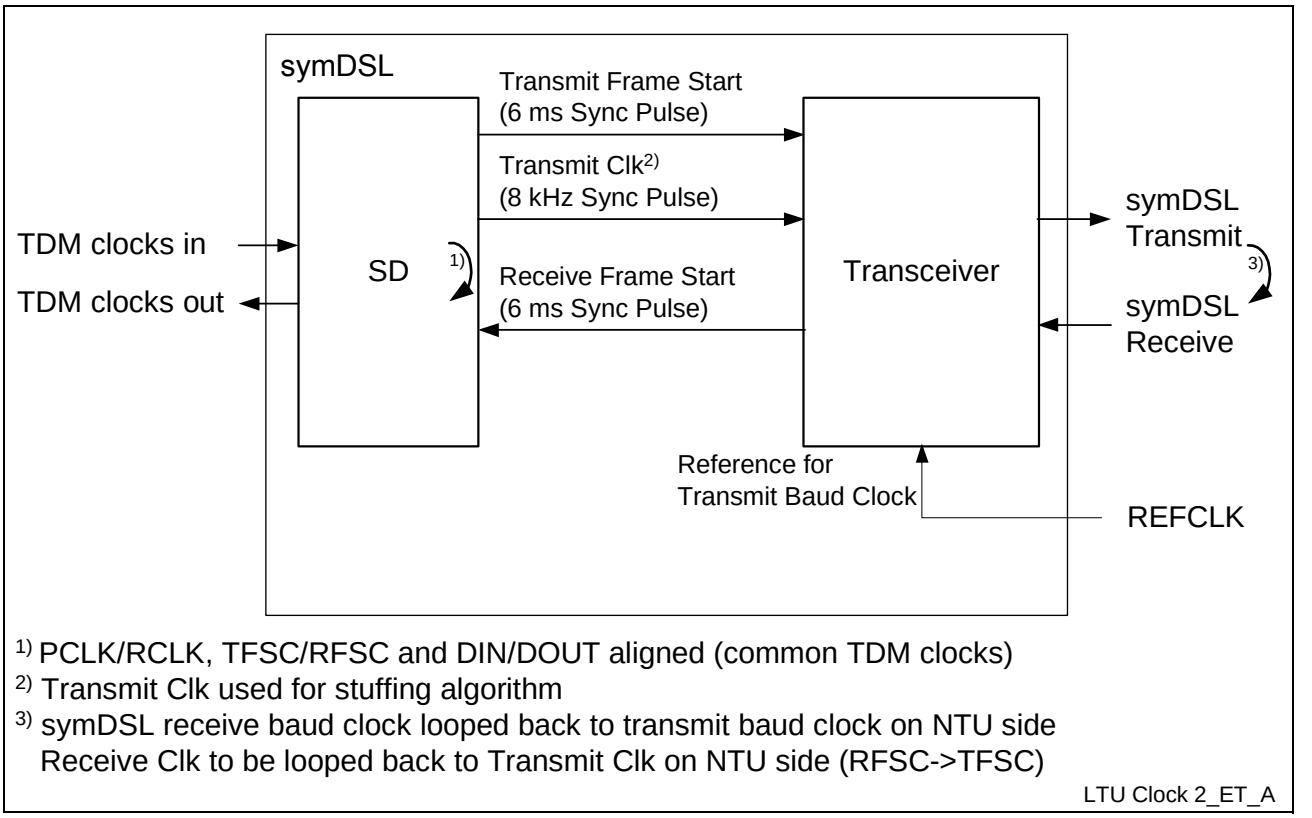


Figure 9 LTU Clock 2_ET_A, Clock Propagation

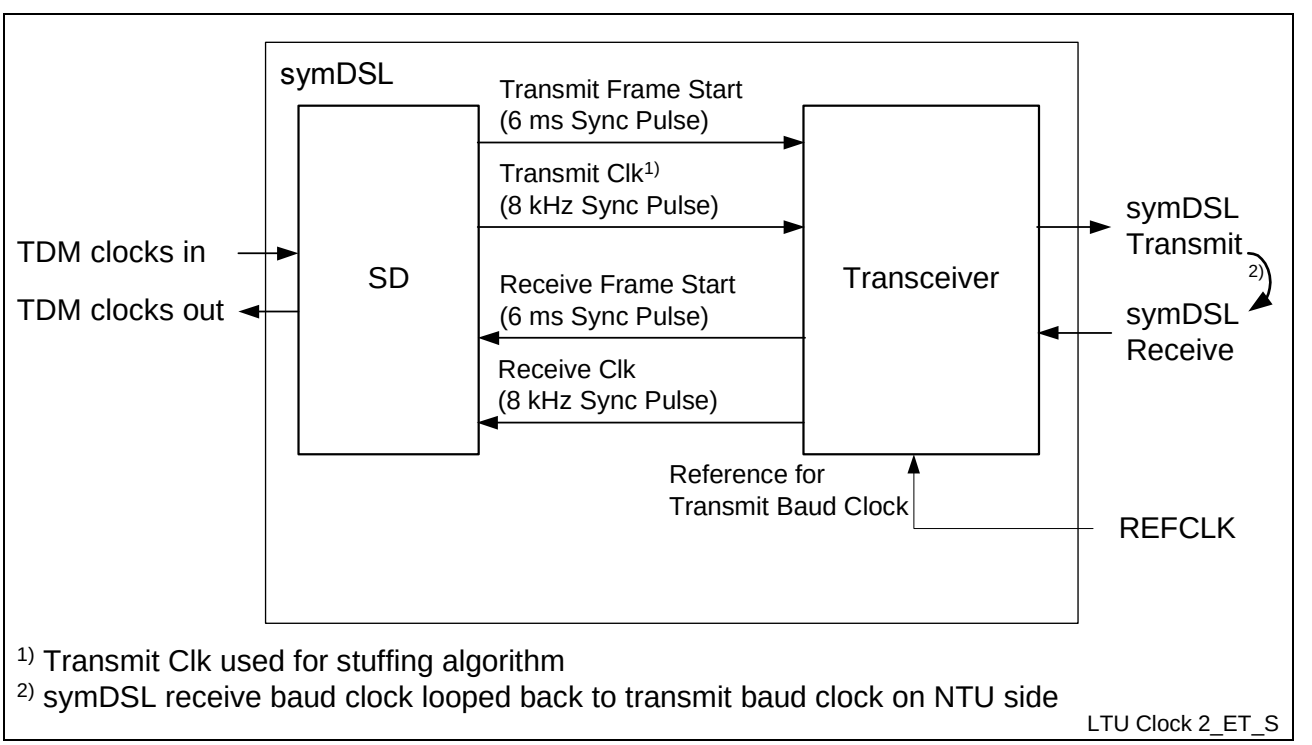


Figure 10 LTU Clock 2_ET_S, Clock Propagation

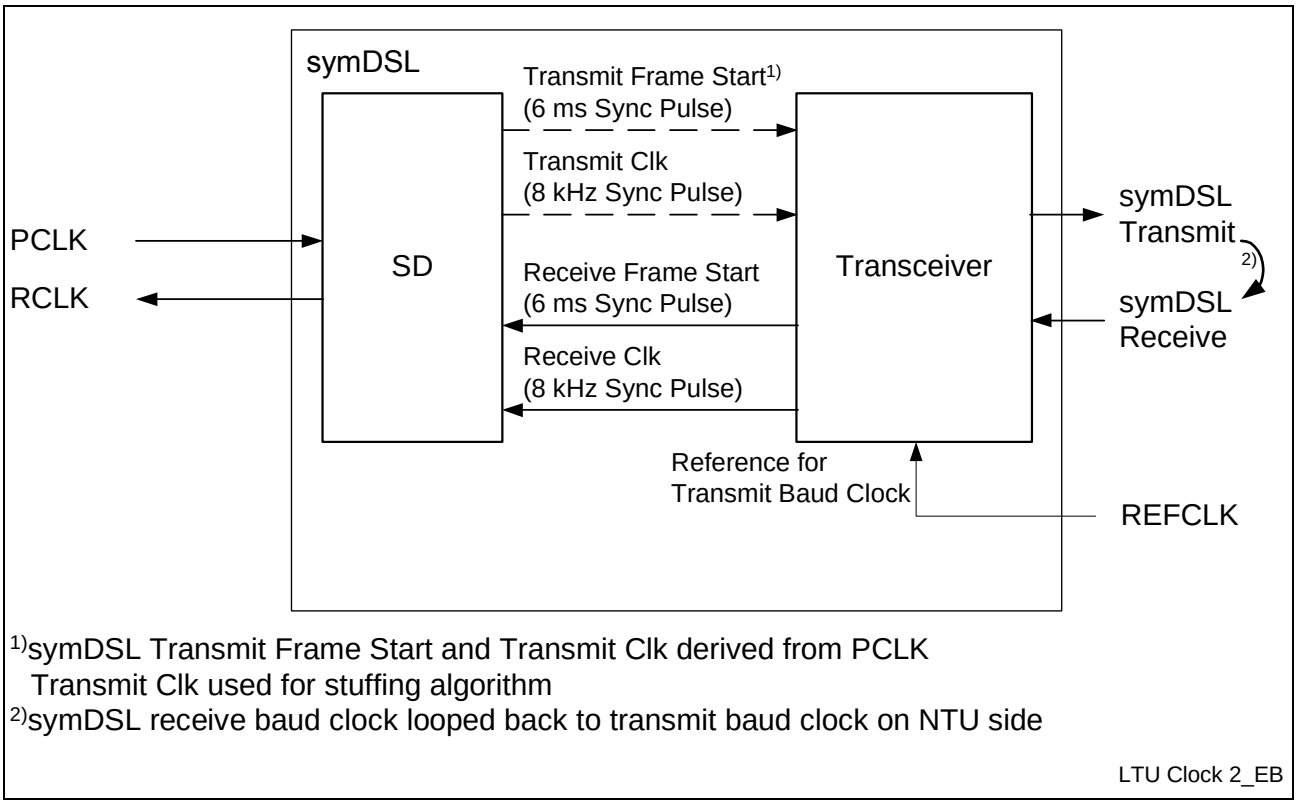


Figure 11 LTU Clock 2_EB, Clock Propagation

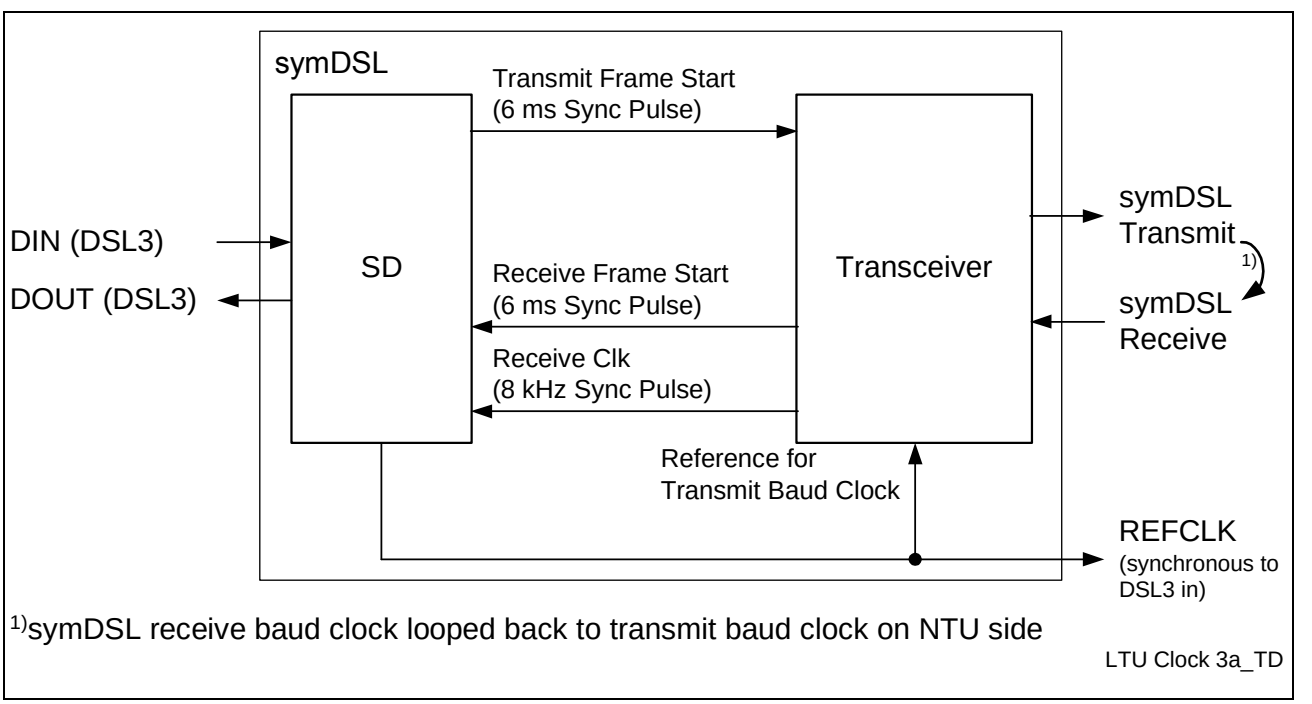


Figure 12 LTU Clock 3a_TD, Clock Propagation

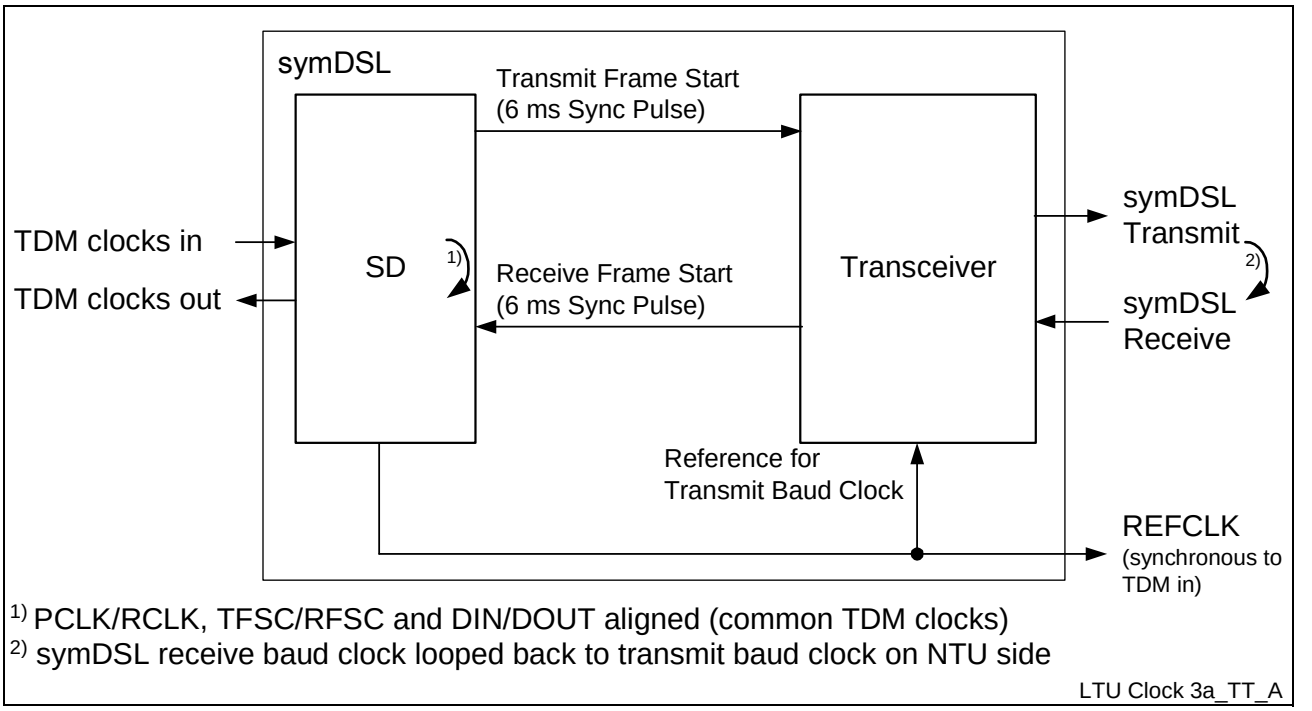


Figure 13 LTU Clock 3a_TT_A, Clock Propagation

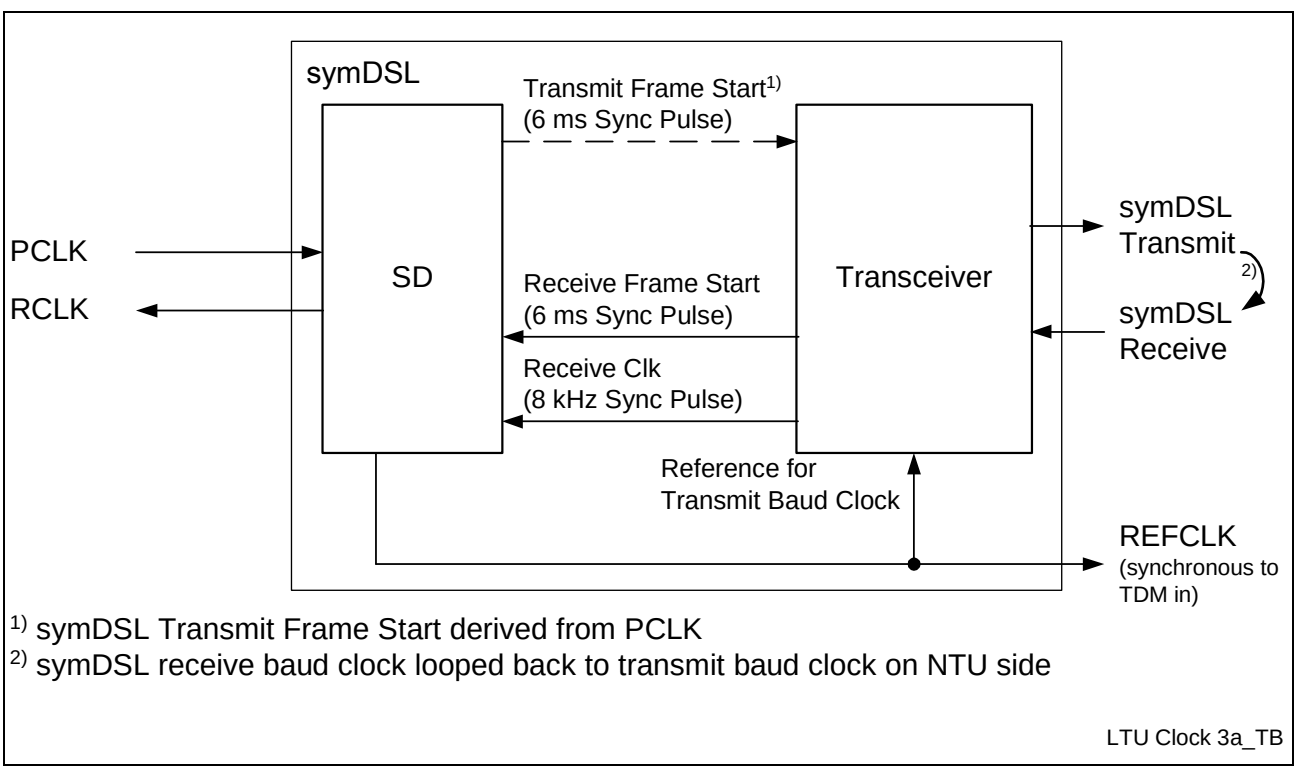


Figure 14 LTU Clock 3a_TB, Clock Propagation

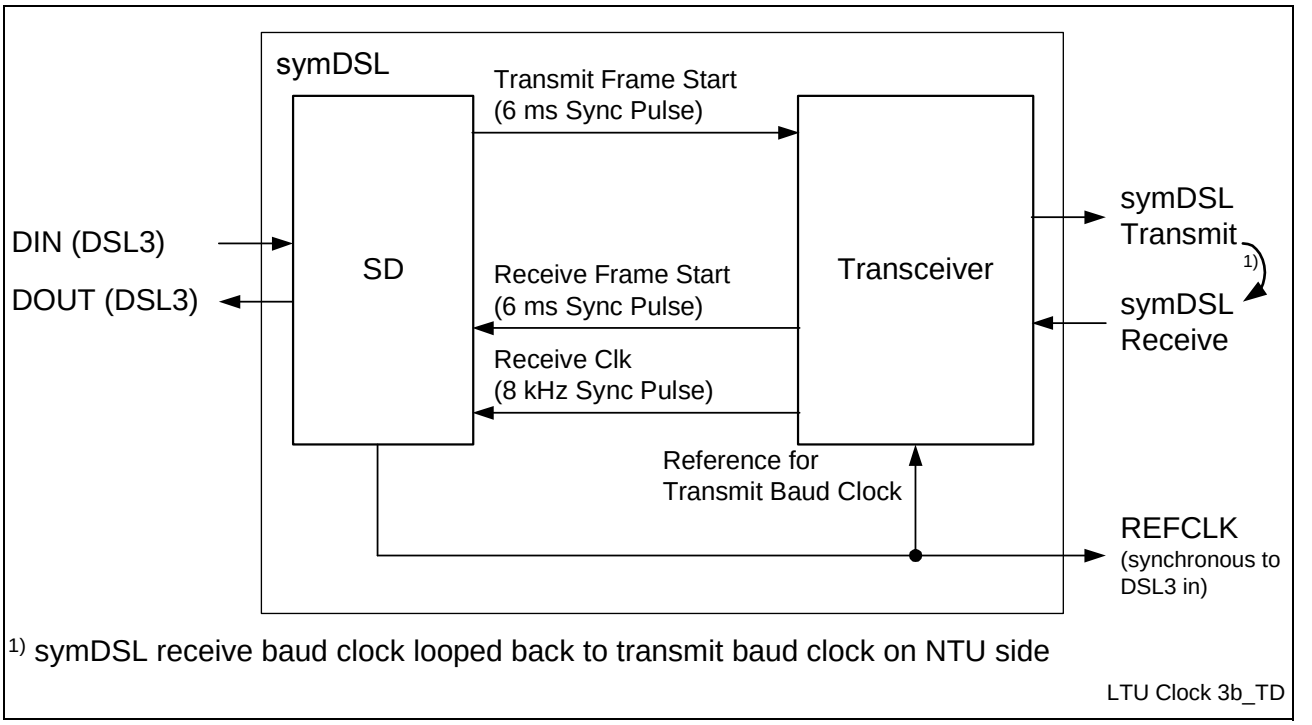


Figure 15 LTU Clock 3b_TD, Clock Propagation

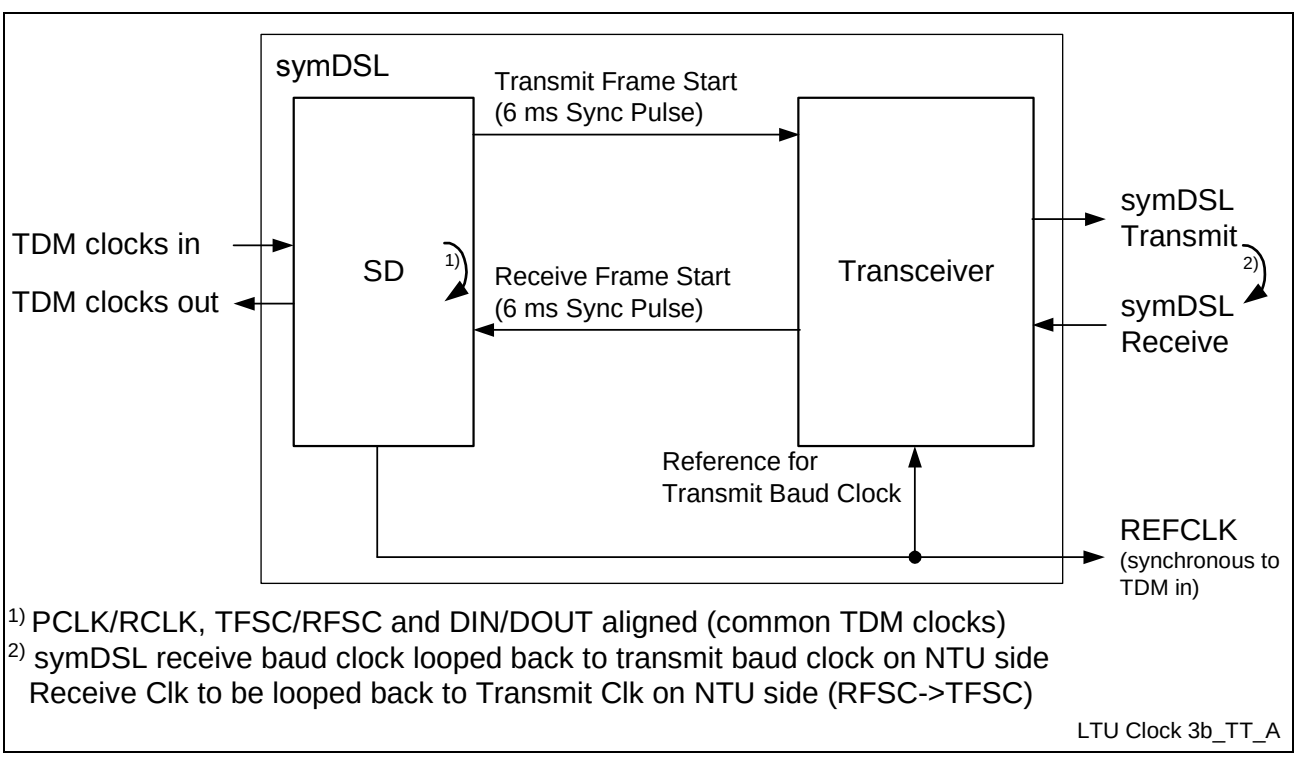


Figure 16 LTU Clock 3b_TT_A, Clock Propagation

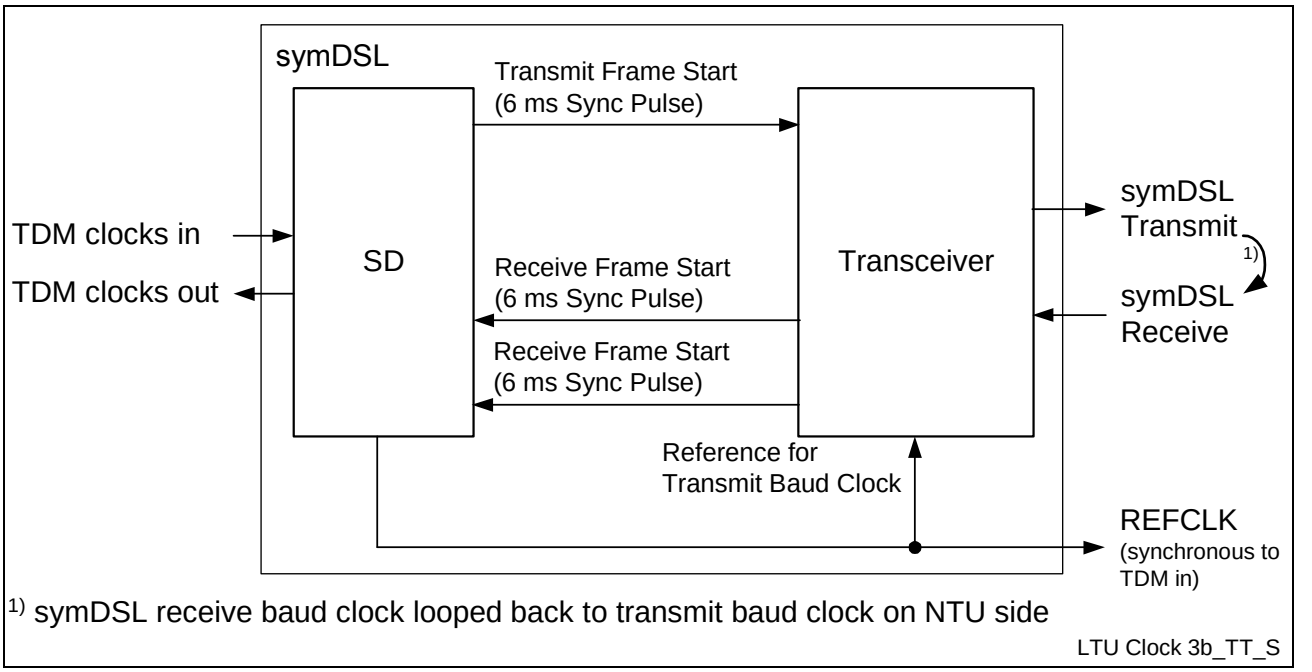


Figure 17 LTU Clock 3b_TT_S, Clock Propagation

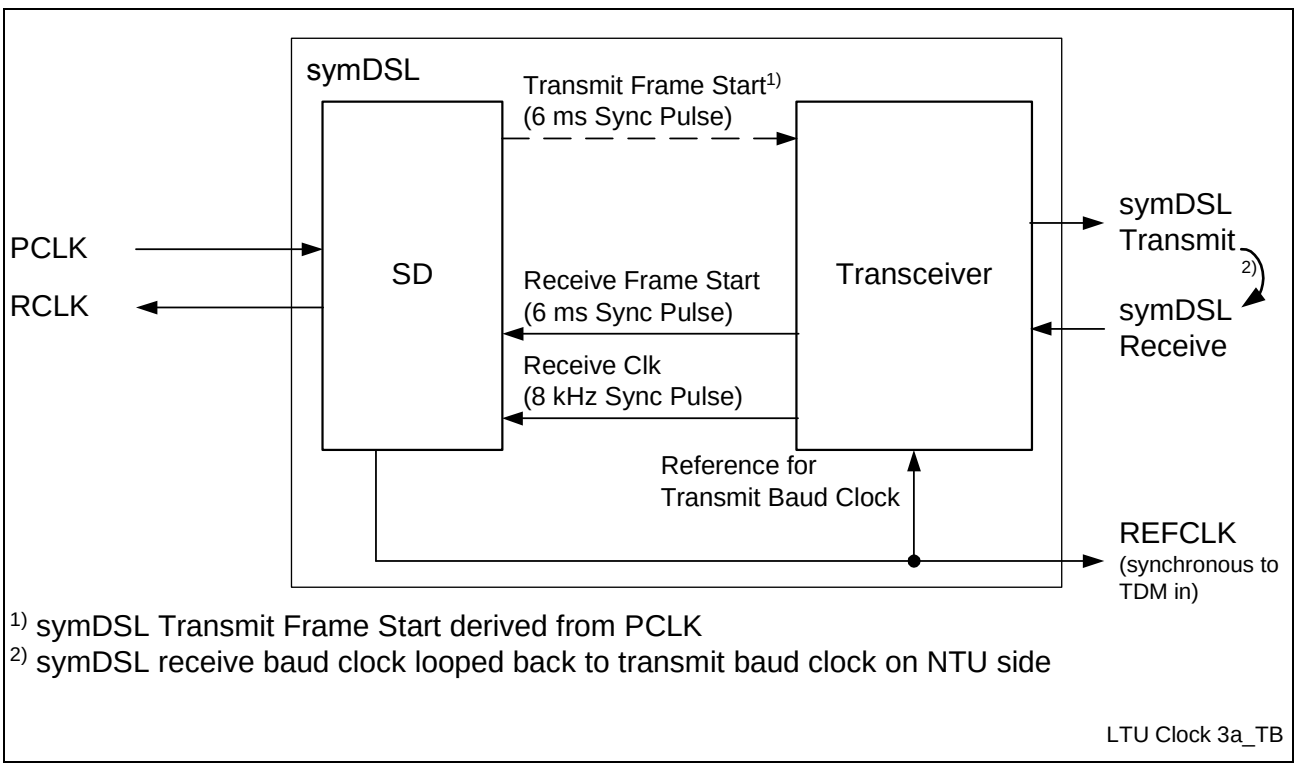


Figure 18 LTU Clock 3b_TB, Clock Propagation

3.3.2 Supported Clock and Interface Modes for STU-R

Table 14 Settings of Clock Modes, STU-R

Clock Mode [1]	Clock Mode Name: NTU Clock ...	SD [2] Mode	Line Tx [3] synchr.		Line Rx [4] sync.	REFCLK		SD Rx Frame/ data clock	Figure #
			Baud Ref.	Frame Sync	Frame Sync	Dir.	Source	Source	
1/2	1_LD	DSL3	Rx Baud	Plesio.	Plesio.	O	Rx Frame	Rx Frame	Figure 19
	1_LT_A [5]	TDM	Rx Baud	Plesio.	Plesio.	O	Rx Frame	SD Tx	Figure 20
	1_LT_S	TDM	Rx Baud	Plesio.	Plesio.	O	Rx Frame	Rx Frame	Figure 21
	1_LB	Bit Serial	Rx Baud	Plesio.	Plesio.	O	Rx Frame	Rx Frame	Figure 22
3a	3a_LD	DSL3	Rx Baud	Sync.	Sync.	O	Rx Frame	Rx Frame	Figure 23
	3a_LT_A [5]	TDM	Rx Baud	Sync.	Sync.	O	Rx Frame	SD Tx	Figure 24
	3a_LT_S	TDM	Rx Baud	Sync.	Sync.	O	Rx Frame	Rx Frame	Figure 25
	3a_LB	Bit Serial	Rx Baud	Sync.	Sync.	O	Rx Frame	Rx Frame	Figure 26

Table 14 Settings of Clock Modes, STU-R (cont'd)

Clock Mode [1]	Clock Mode Name: NTU Clock ...	SD[2] Mode	Line Tx[3] synchr.		Line Rx[4] sync.	REFCLK		SD Rx Frame/ data clock	Figure #
			Baud Ref.	Frame Sync	Frame Sync	Dir.	Source	Source	
3b	3b_LD	DSL3	Rx Baud	Plesio.	Sync.	O	Rx Frame	Rx Frame	Figure 27
	3b_LT_A [5]	TDM	Rx Baud	Plesio.	Sync.	O	Rx Frame	SD Tx	Figure 28
	3b_LT_S	TDM	Rx Baud	Plesio.	Sync.	O	Rx Frame	Rx Frame	Figure 29
	3b_LB	Bit Serial	Rx Baud	Plesio.	Sync.	O	Rx Frame	Rx Frame	Figure 30

1) Clock Mode according to ITU-T G.shdsl.bis

2) SD stands for Serial Data Interface

3) Tx stands for the transmit direction and refers to the line interface

4) Rx stands for the receive direction and refers to the line interface

5) TDM clock in must be synchronous to REFCLK. This clock mode is useful for applications with common TDM clocks for all TDM ports. The common TDM clock can be derived from one TDM receive port.

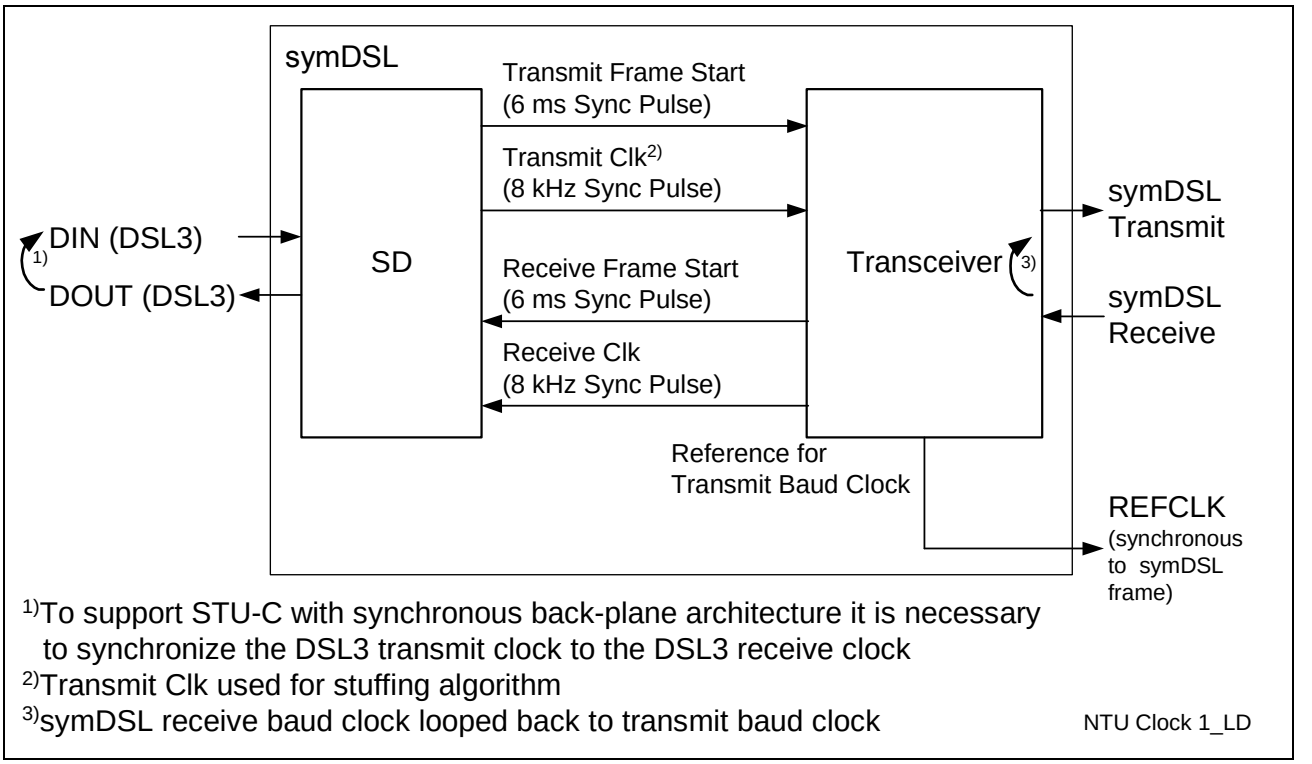


Figure 19 NTU Clock 1_LD, Clock Propagation

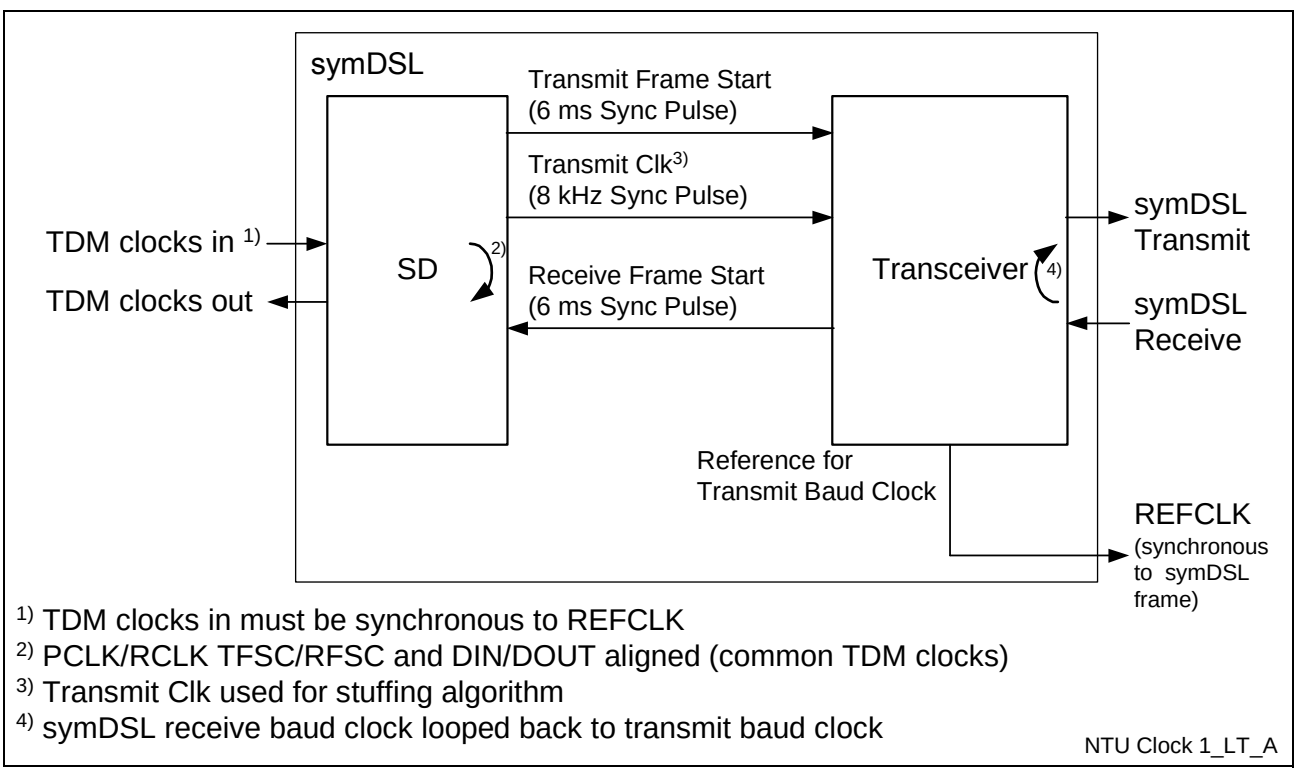
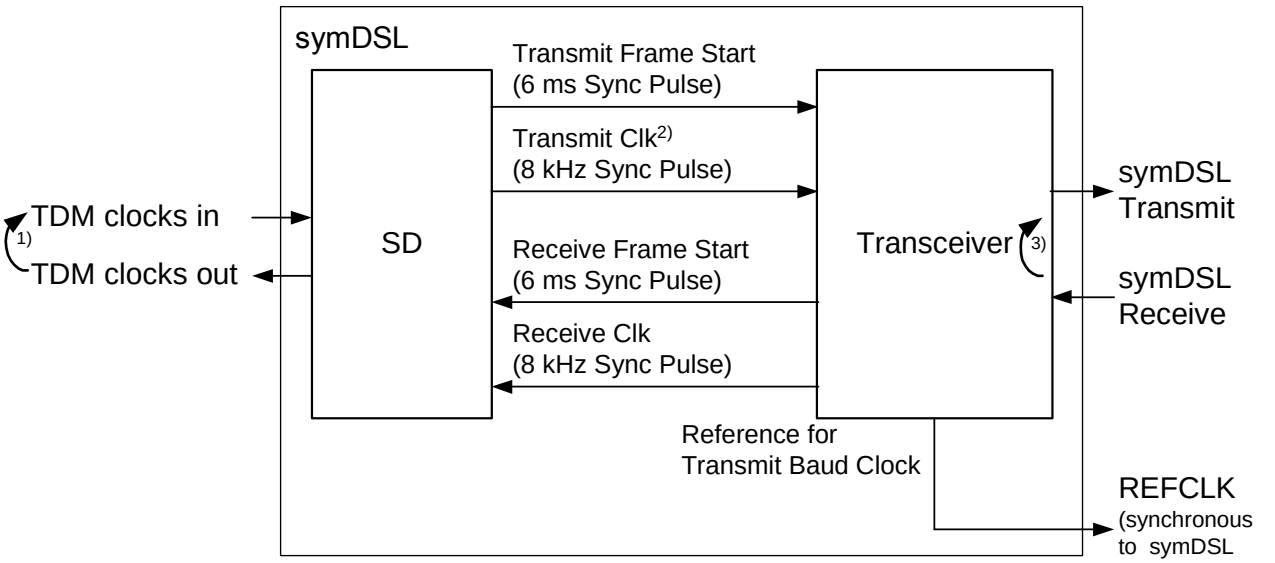


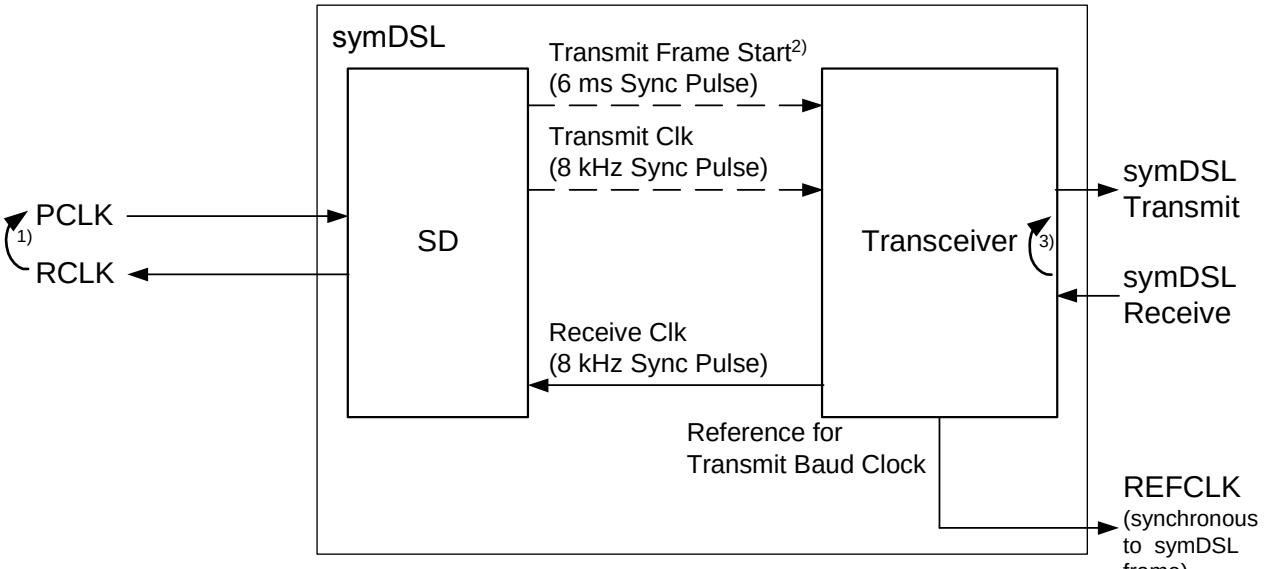
Figure 20 NTU Clock 1_LT_A, Clock Propagation



1)To support STU-C with synchronous back-plane architecture it is necessary to synchronize the TDM transmit clock to the TDM receive clock
2)Transmit Clk used for stuffing algorithm
3)symDSL receive baud clock looped back to transmit baud clock

NTU Clock 1_LT_S

Figure 21 NTU Clock 1_LT_S, Clock Propagation



1)To support STU-C with synchronous back-plane architecture it is necessary to synchronize the TDM transmit clock to the TDM receive clock
2)symDSL Transmit Frame Start and Transmit Clk derived from PCLK
Transmit Clk used for stuffing algorithm
3)symDSL receive baud clock looped back to transmit baud clock

NTU Clock 1_LB

Figure 22 NTU Clock 1_LB, Clock Propagation

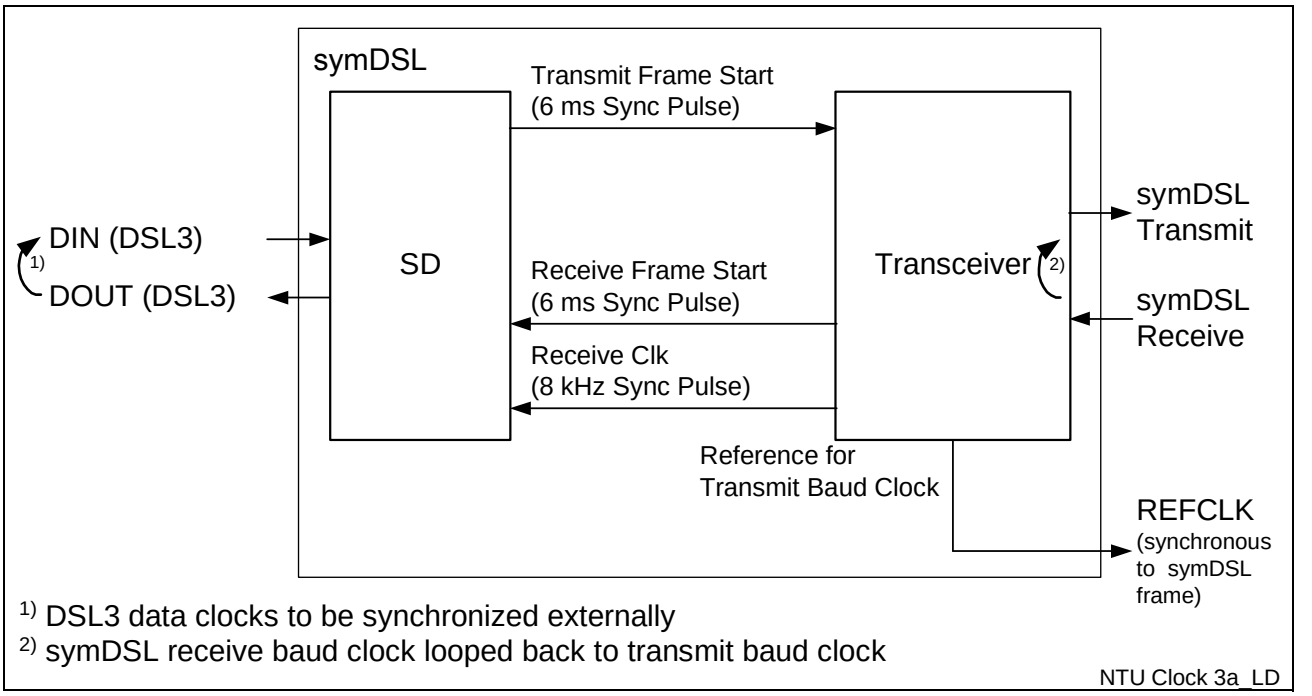


Figure 23 NTU Clock 3a_LD, Clock Propagation

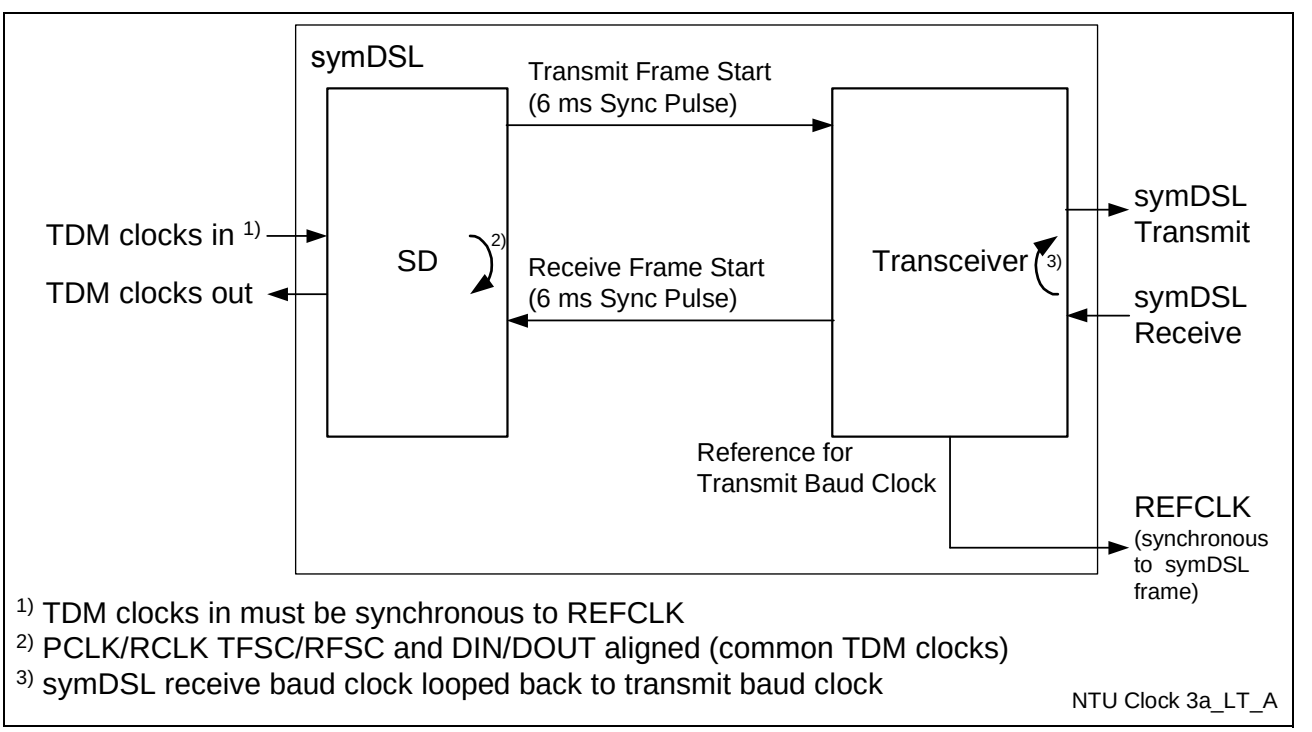


Figure 24 NTU Clock 3a_LT_A, Clock Propagation

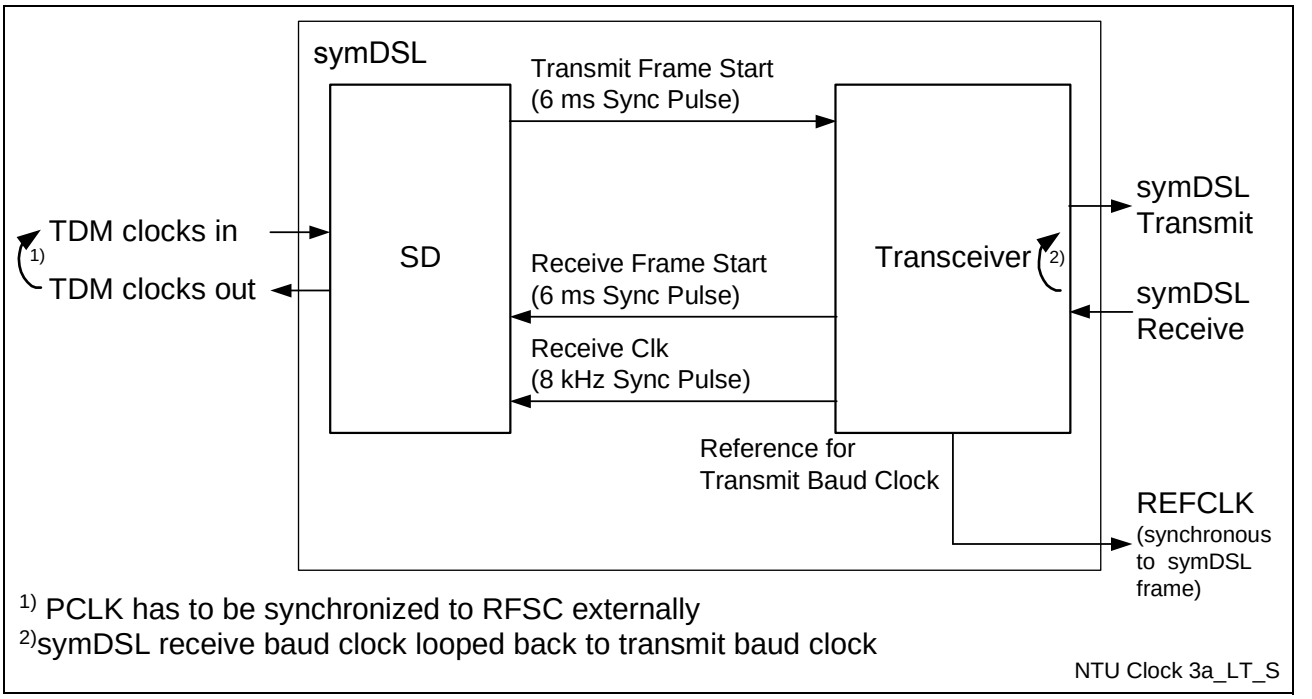


Figure 25 NTU Clock 3a_LT_S, Clock Propagation

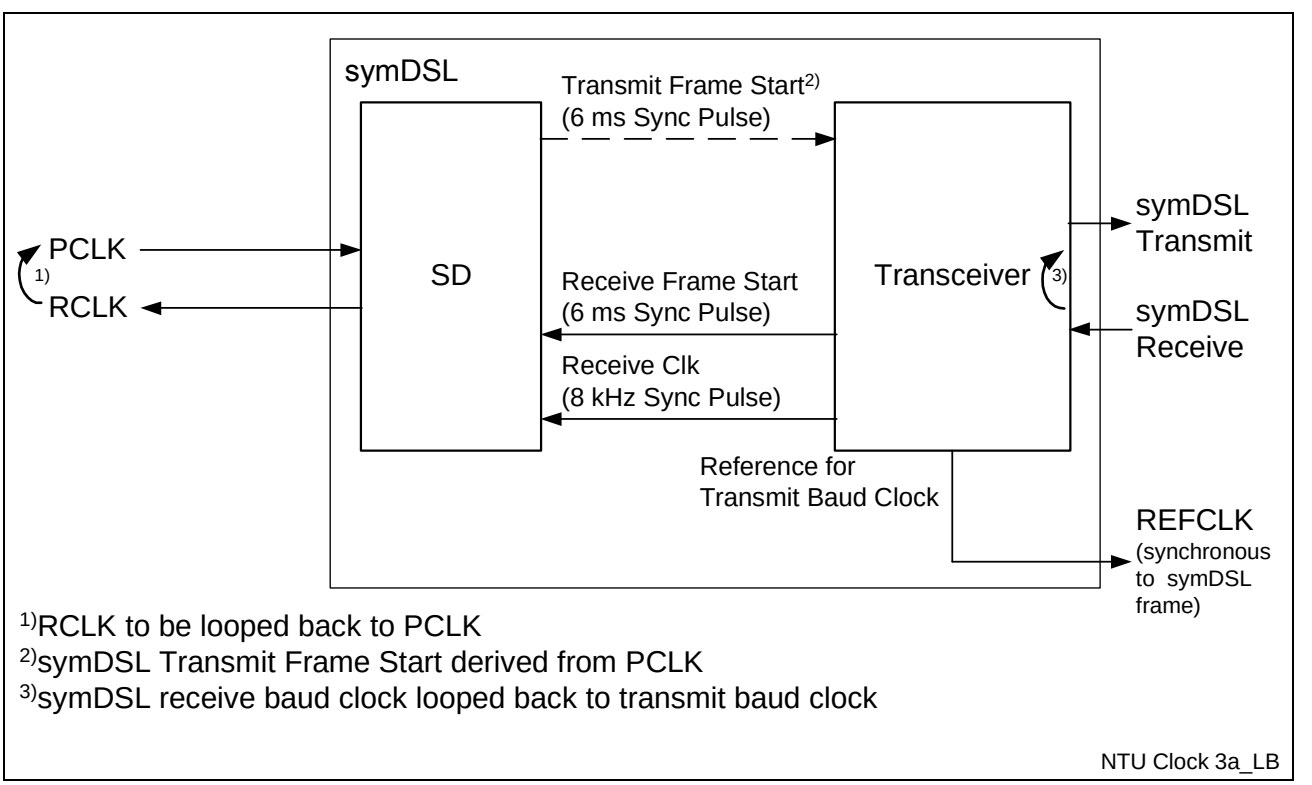


Figure 26 NTU Clock 3a_LB, Clock Propagation

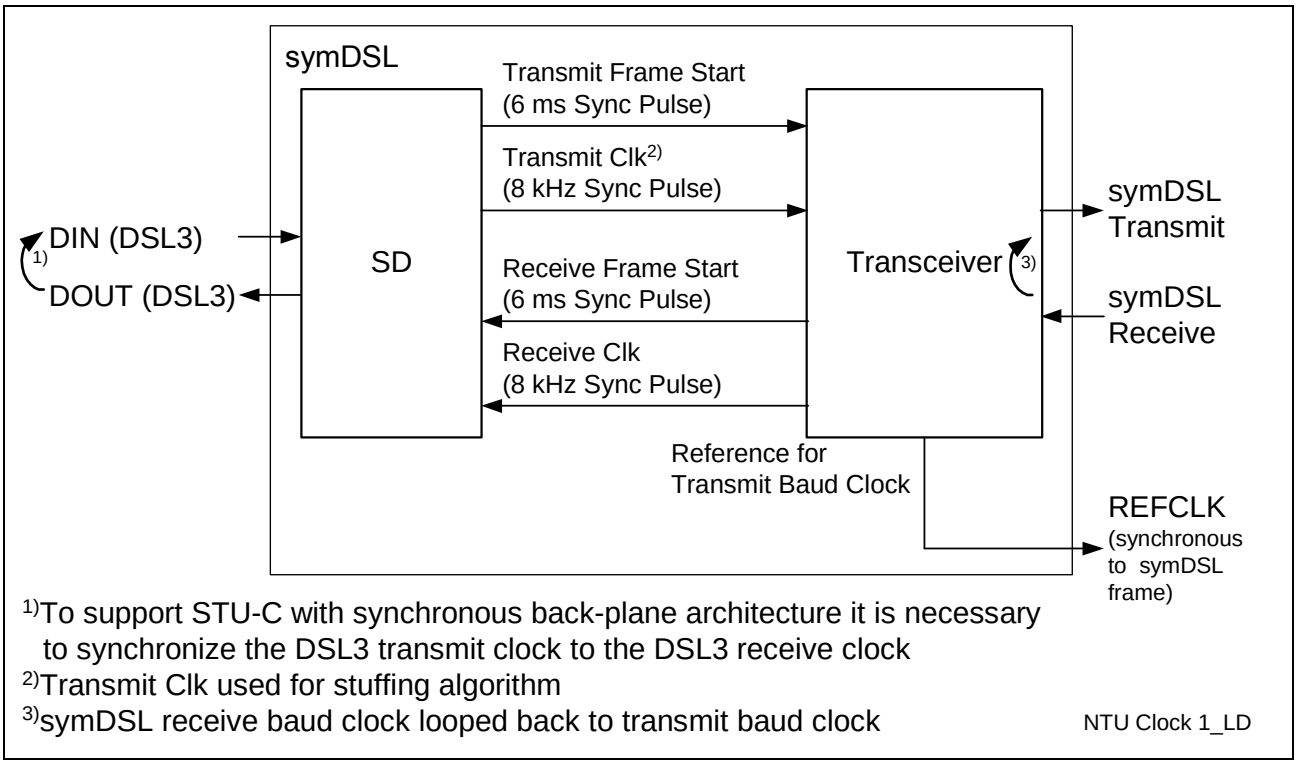


Figure 27 NTU Clock 3b_LD, Clock Propagation

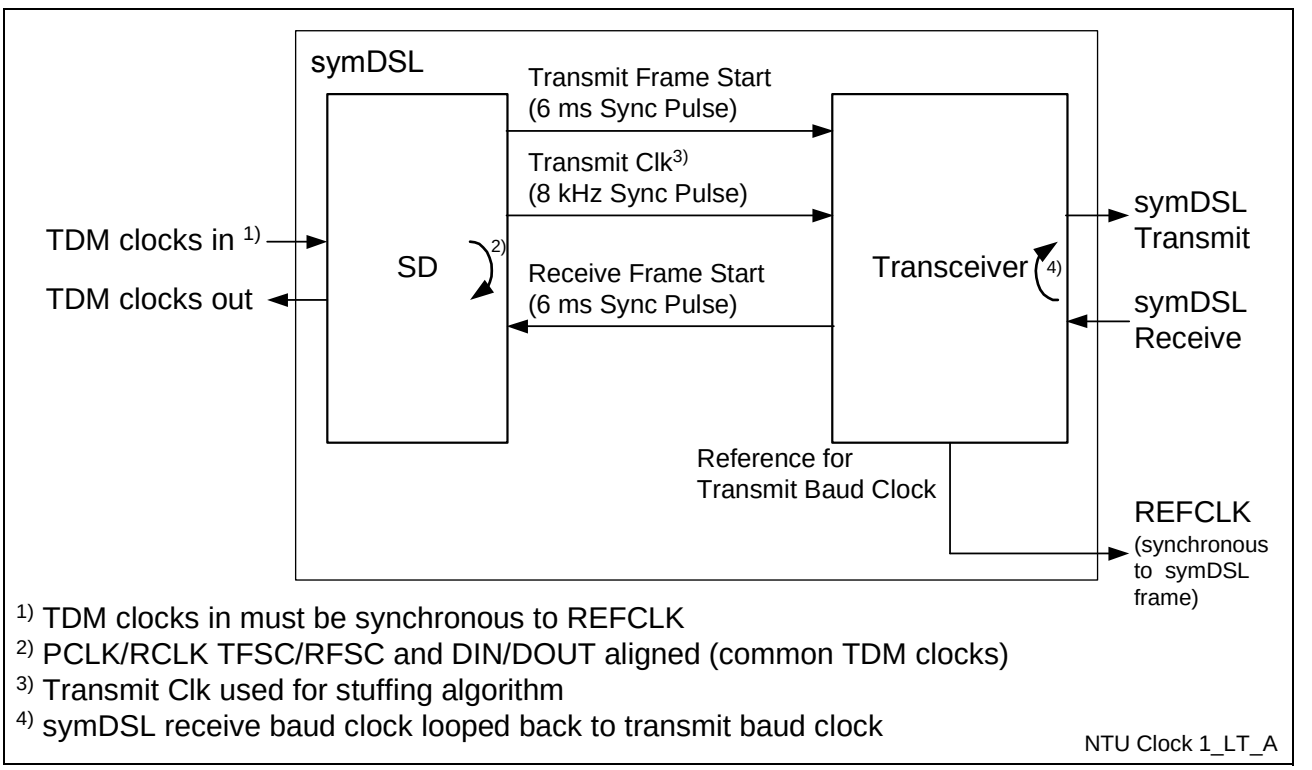
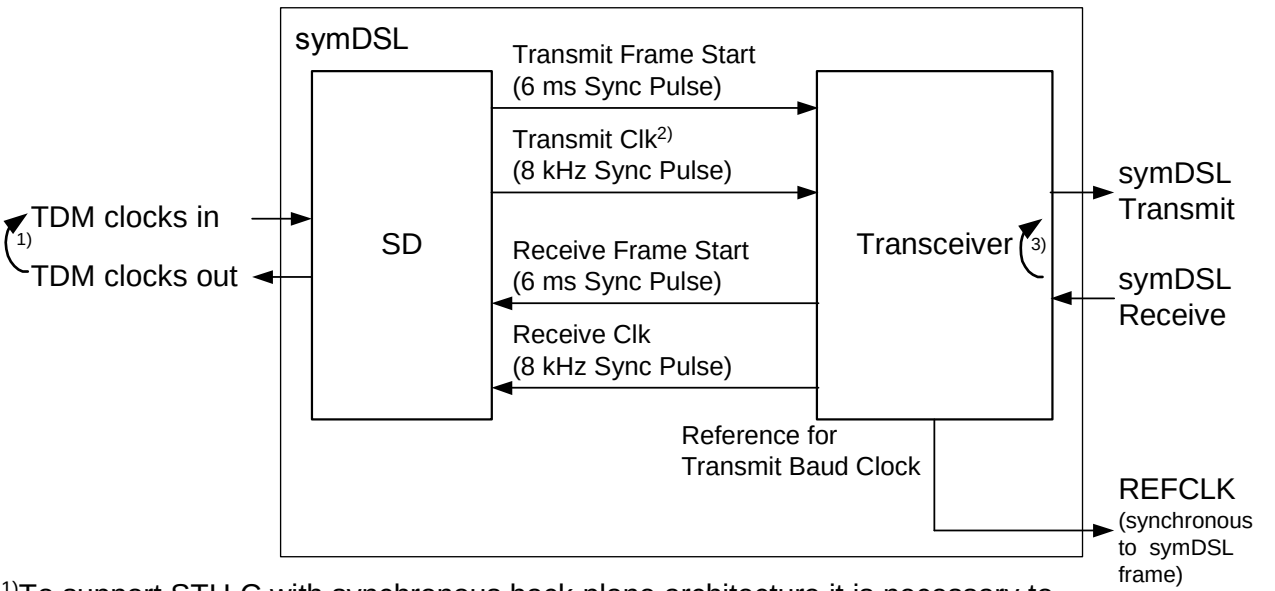


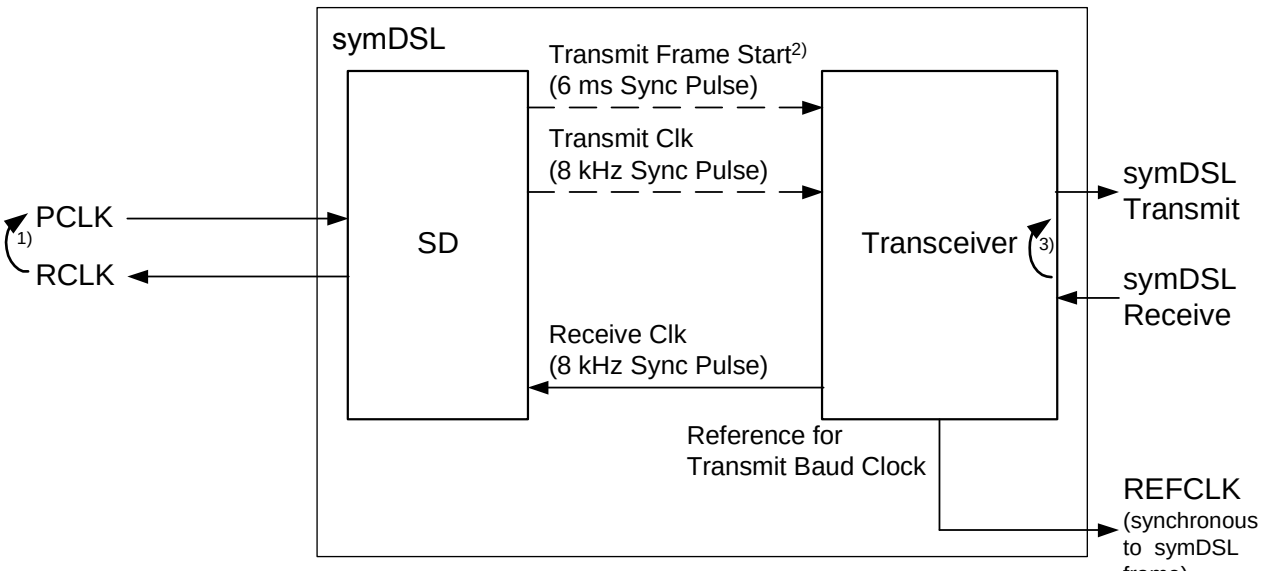
Figure 28 NTU Clock 3b_LT_A, Clock Propagation



1)To support STU-C with synchronous back-plane architecture it is necessary to synchronize the TDM transmit clock to the TDM receive clock
2)Transmit Clk used for stuffing algorithm
3)symDSL receive baud clock looped back to transmit baud clock

NTU Clock 1_LT_S

Figure 29 NTU Clock 3b_LT_S, Clock Propagation



1)To support STU-C with synchronous back-plane architecture it is necessary to synchronize the TDM transmit clock to the TDM receive clock
2)symDSL Transmit Frame Start and Transmit Clk derived from PCLK
Transmit Clk used for stuffing algorithm
3)symDSL receive baud clock looped back to transmit baud clock

NTU Clock 1_LB

Figure 30 NTU Clock 3b_LB, Clock Propagation

3.3.3 Supported Clock and Interface Modes for SRU-C

Table 15 Settings of Clock Modes, SRU-C

Clock Mode [1]	Clock Mode Name: SRU-C Clock ...	SD[2] Mode	Line Tx[3] synchr.		Line Rx[4] sync.	REFCLK		SD Rx Frame/ data clock	Fig. #
			Baud Ref.	Frame Sync	Frame Sync	Dir.	Source	Source	
1	1_ID	DSL3	Local Osci.	Plesio.	Plesio.	O	Local Osci.	Rx Frame	Fig. 31
2	2_ED	DSL3	REFCLK of SRU-R	Plesio.	Plesio.	I	REFCLK of SRU-R	Rx Frame	Fig. 32
3a	3a_ED	DSL3	REFCLK of SRU-R	Sync.	Sync.	I	REFCLK of SRU-R	Rx Frame	Fig. 33
3b	3b_ED	DSL3	REFCLK of SRU-R	Sync.	Plesio.	I	REFCLK of SRU-R	Rx Frame	Fig. 34

1) Clock Mode according to ITU-T G.shdsl.bis

2) SD stands for Serial Data Interface

3) Tx stands for the transmit direction and refers to the line interface

4) Rx stands for the receive direction and refers to the line interface

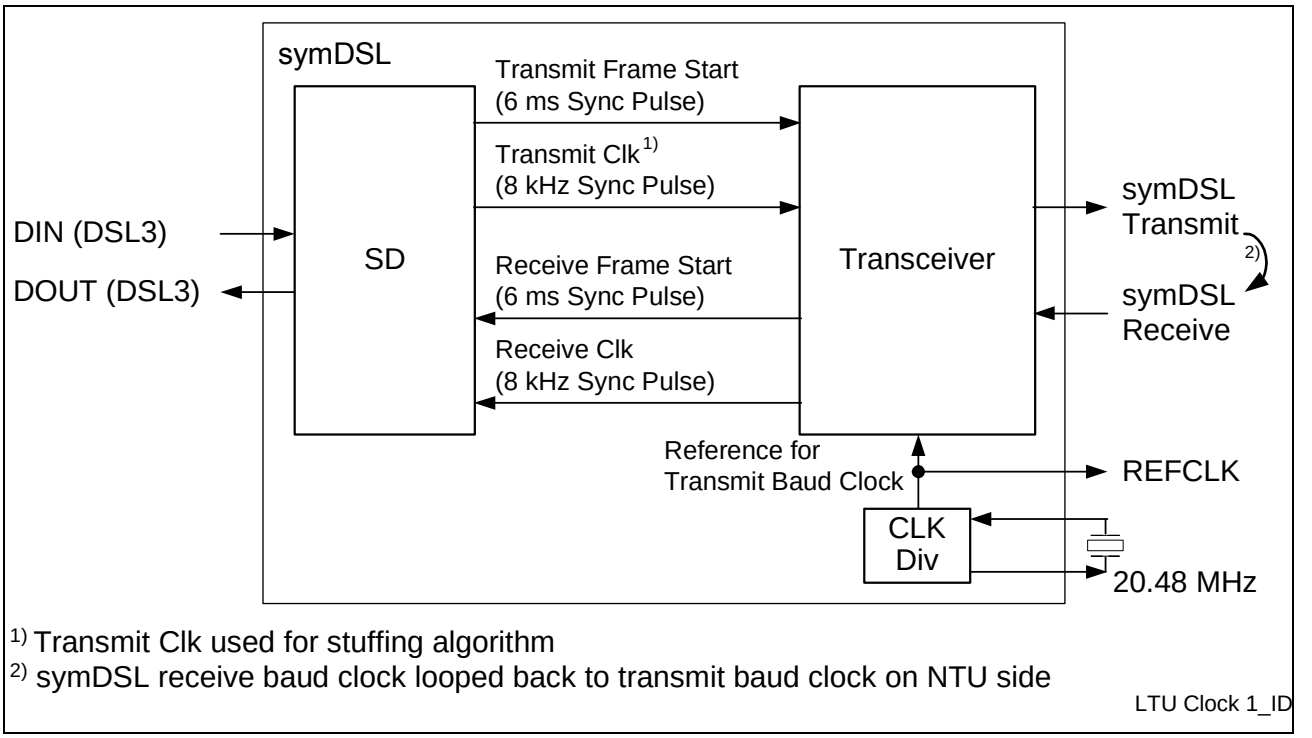


Figure 31 SRU-C Clock 1_ID, Clock Propagation

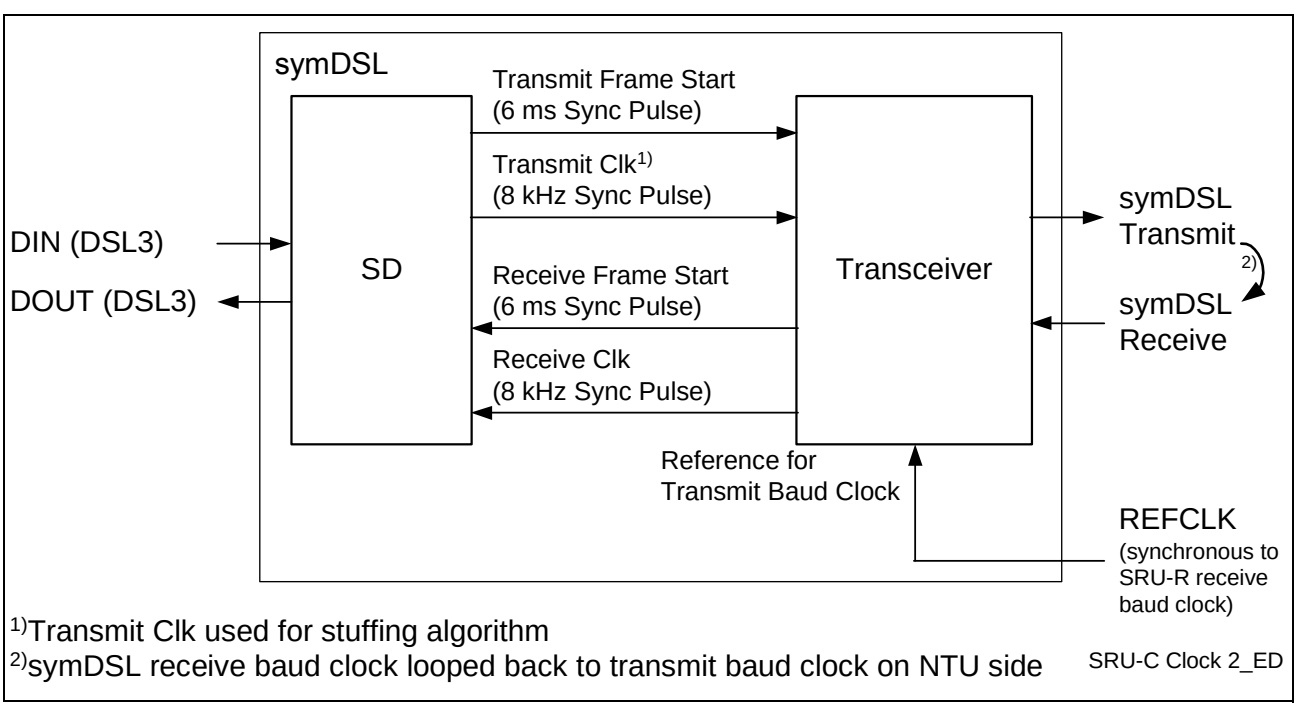


Figure 32 SRU-C Clock 2_ED, Clock Propagation

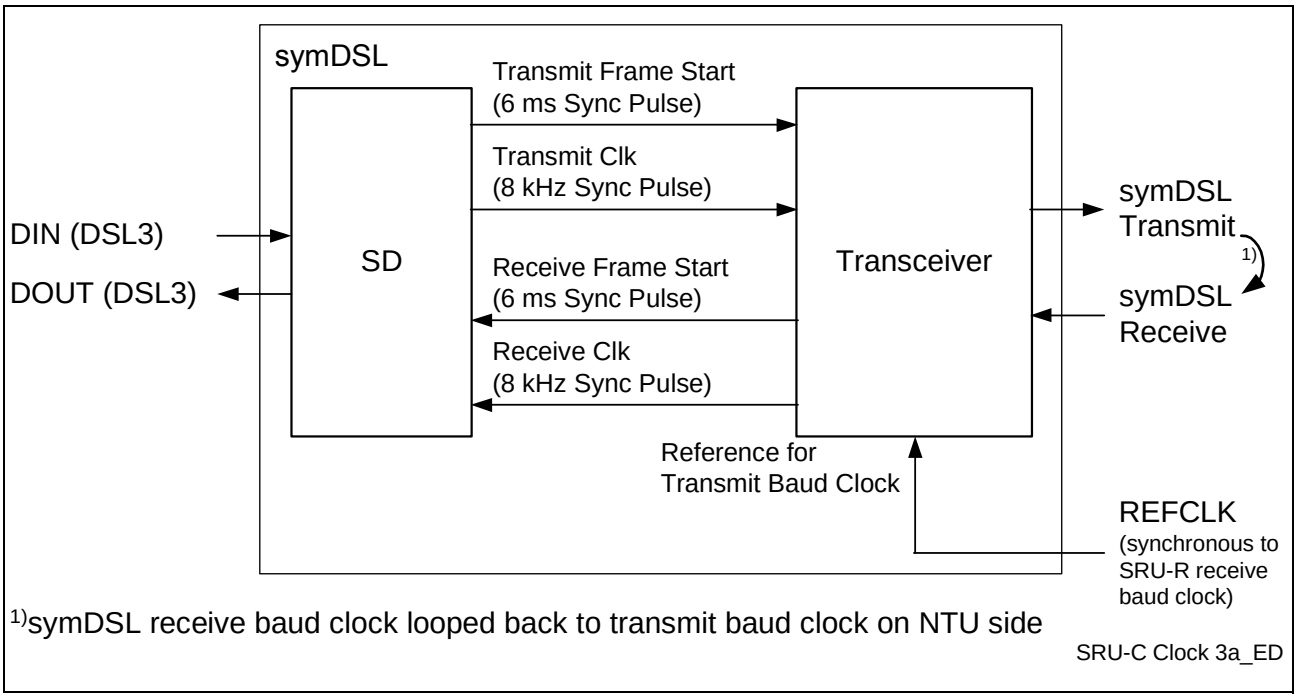


Figure 33 SRU-C Clock 3a_ED, Clock Propagation

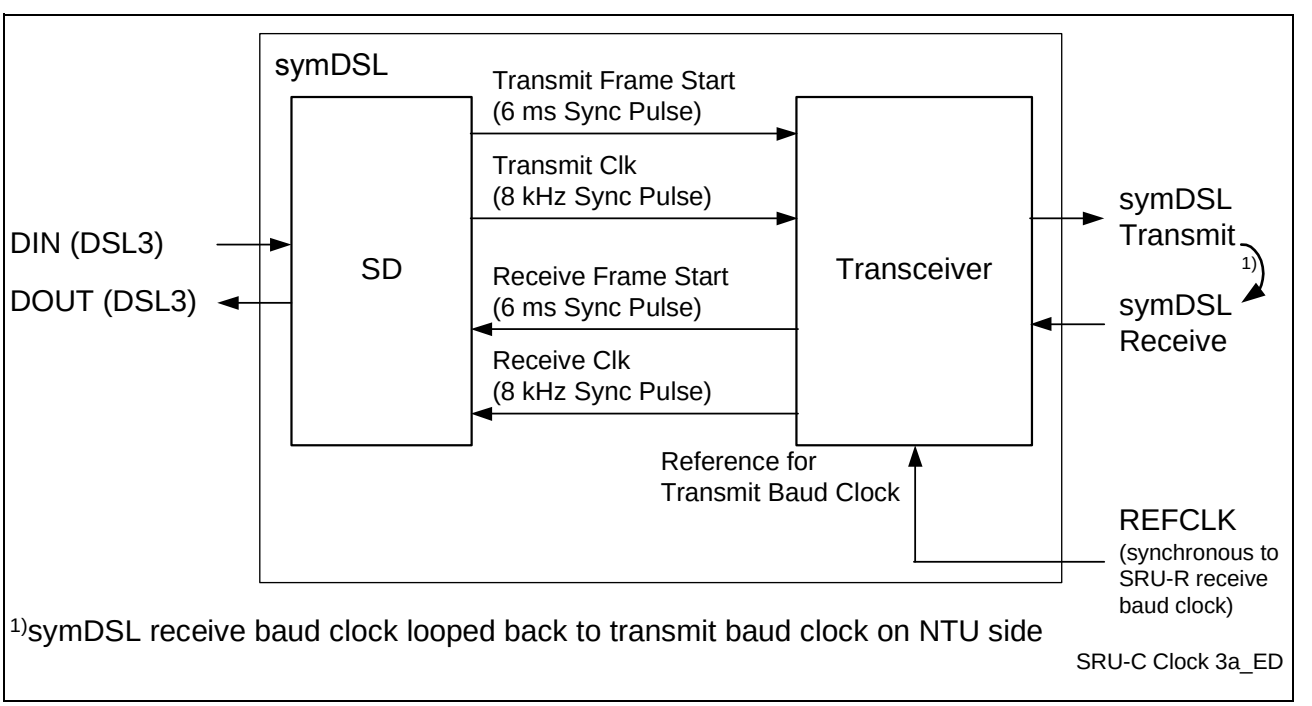


Figure 34 SRU-C Clock 3b_ED, Clock Propagation

3.3.4 Supported Clock and Interface Modes for SRU-R

Table 16 Settings of Clock Modes, SRU-R

Clock Mode [1]	Clock Mode Name: SRU-R Clock ...	SD[2] Mode	Line Tx[3] synchr.		Line Rx[4] sync.	REFCLK		SD Rx Frame/ data clock	Figure #
			Baud Ref.	Frame Sync	Frame Sync	Dir.	Source	Source	
1/2	1_LD	DSL3	Rx Baud	Plesio.	Plesio.	O	Rx Baud	Rx Frame	Figure 35
3a	3a_LD	DSL3	Rx Baud	Sync.	Sync.	O	Rx Baud	Rx Frame	Figure 36
3b	3b_LD	DSL3	Rx Baud	Plesio.	Sync.	O	Rx Baud	Rx Frame	Figure 37

[1] Clock Mode according to ITU-T G.shdsl.bis

[2] SD stands for Serial Data Interface

[3] Tx stands for the transmit direction and refers to the line interface

[4] Rx stands for the receive direction and refers to the line interface

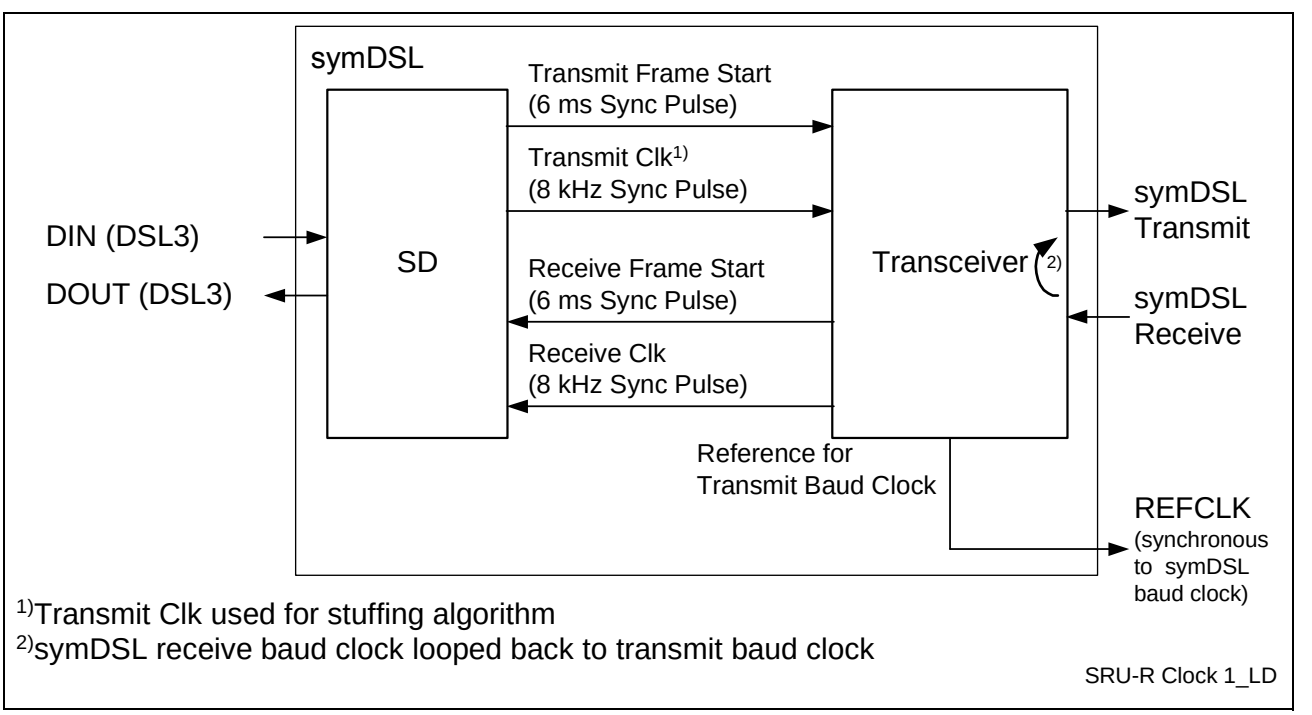


Figure 35 SRU-R Clock 1_LD, Clock Propagation

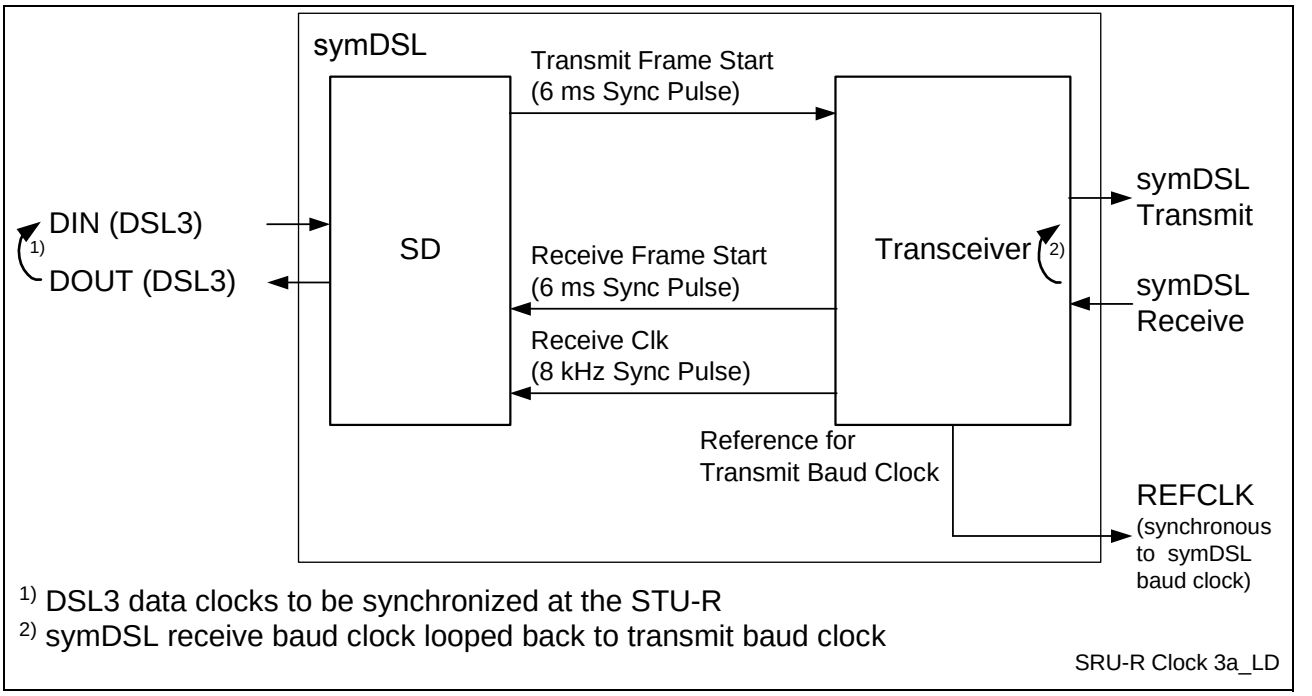


Figure 36 SRU-R Clock 3a_LD, Clock Propagation

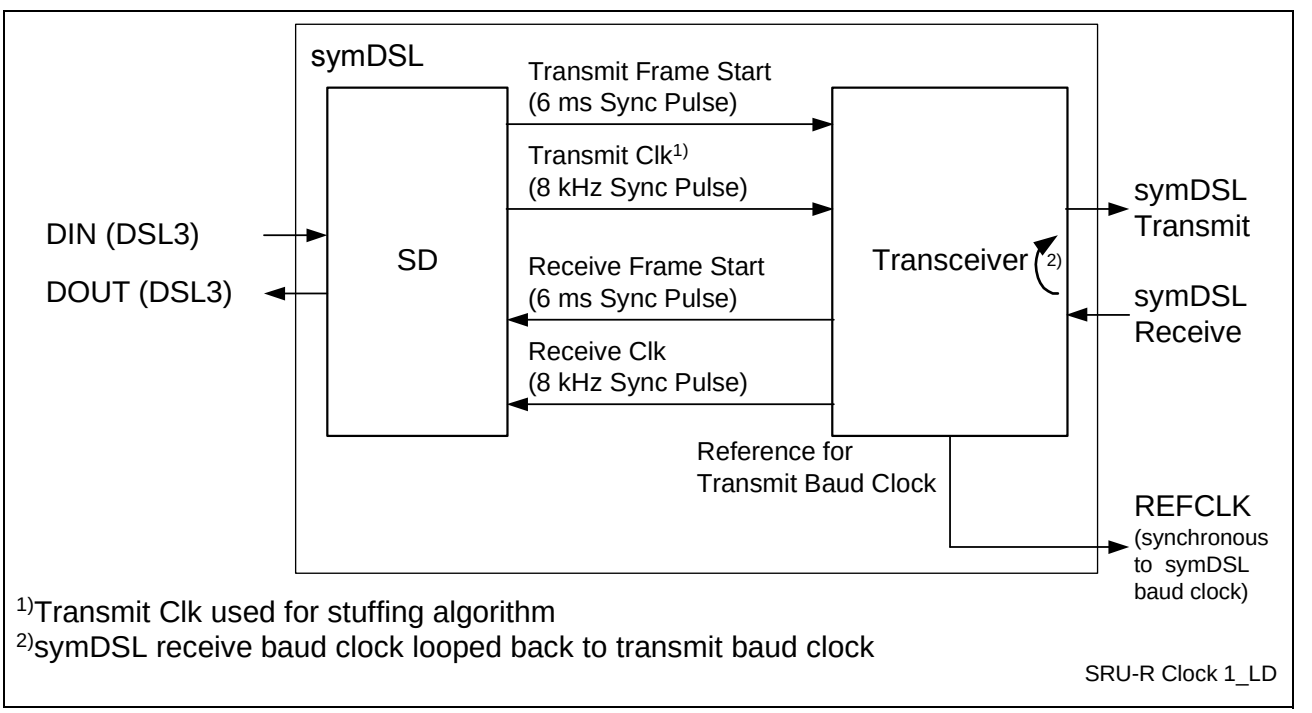


Figure 37 SRU-R Clock 3b_LD, Clock Propagation

3.4 Loop Backs

Figure 38 shows the loops of the SDFE-4, which are implemented for each symDSL channel.

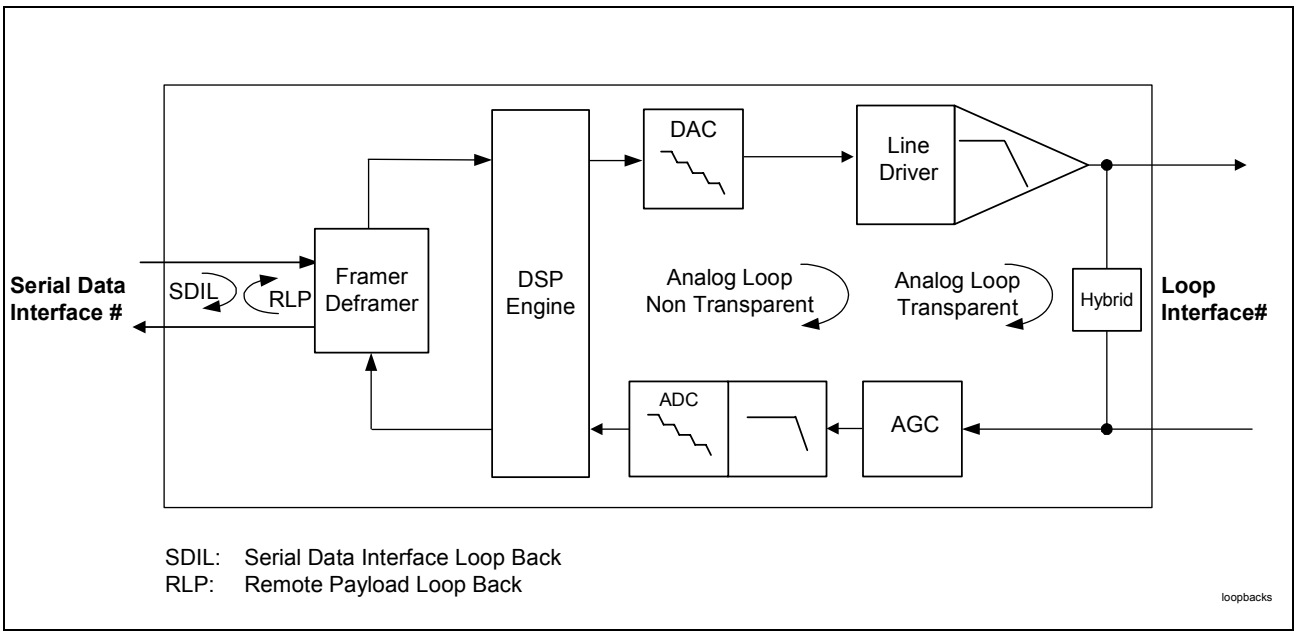


Figure 38 Loop Backs

4 Functional Description

4.1 symDSL Reference Model

Figure 39 shows the symDSL reference model according ITU-T G.991.2, ITU-T G.shdsl.bis and ETSI TS 101 524.

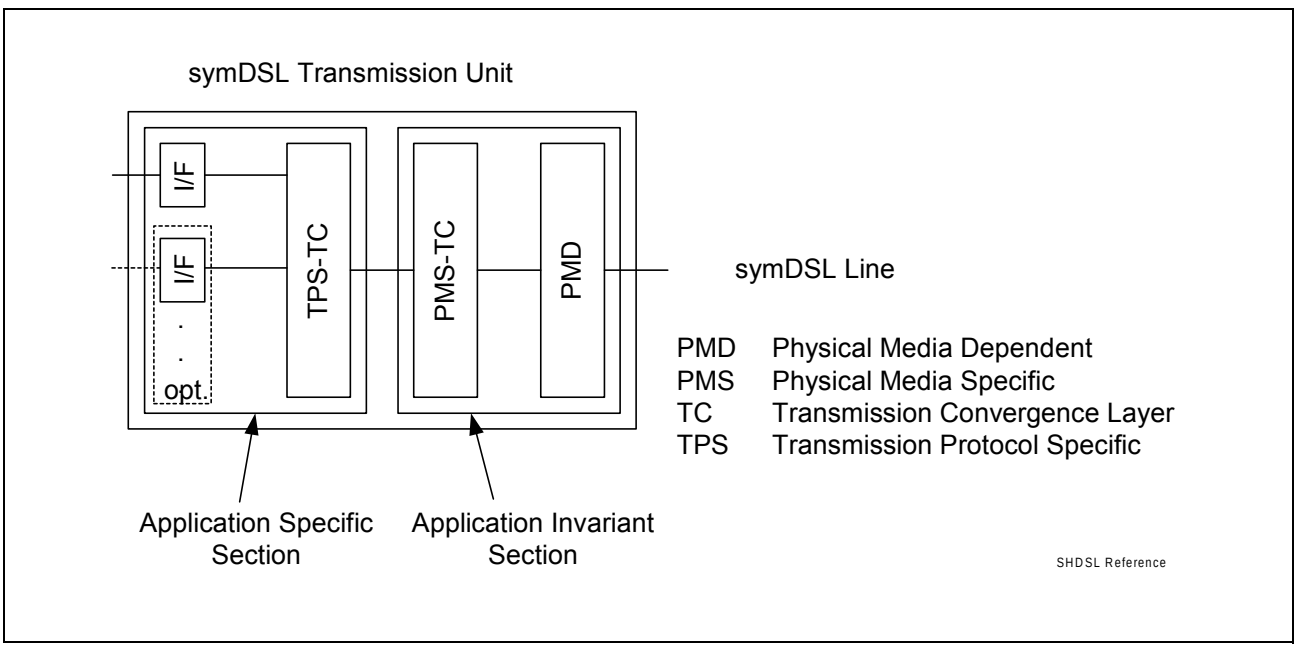


Figure 39 symDSL Reference Model

The SDFE-4 handles the PMS-TC functionality, the PMD functionality and the STM of the TPS-TC functionality including *M*-pair mode.

4.2 Functional Block Diagram

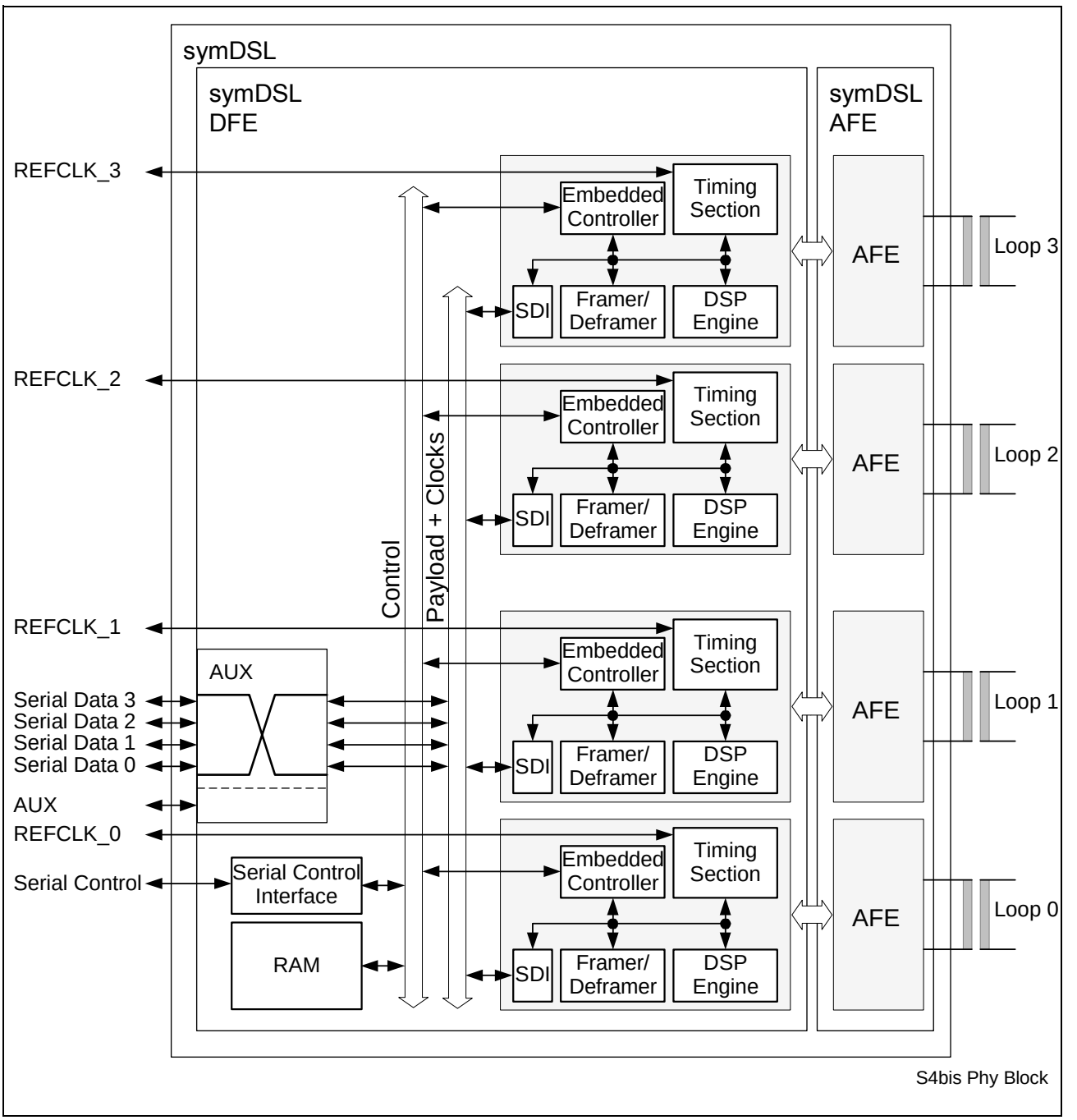


Figure 40 Functional Block Diagram

4.3 Functional Description, Digital Front End (DFE)

4.3.1 Memory (RAM)

Firmware for the 4 symDSL channels will be stored within the memory block (RAM). Firmware download is done via the Serial Control Interface.

4.3.2 Timing Section (Timing Recovery)

On the central office side (LTU, STU-C) and the regenerator unit COT side (SRU-C) the loop clock can be derived directly from the oscillator (internal timed) or the loop clock can be synchronized to any reference clock from the system side by means of a digital phase locked loop (external timed).

The network timing reference on the remote side (NTU, STU-R) is recovered from the received frame clock by means of a digital phase locked loop. This network timing reference is supplied as reference clock to the system for all data rates.

On the regenerator unit RT side (SRU-R) the reference clock is recovered from the receive baud clock by means of a digital phase locked loop.

The crystal to be used is the same for all modes and data rates.

4.3.3 Framer and Deframer

In transmit direction the framer puts the payload and the overhead bits in the defined order of a symDSL frame. In receive direction the deframer extracts the payload and overhead bits out of the frame.

4.3.4 DSP Engine

The DSP engine consists of various sub-blocks. These sub-bloks will be described in this chapter.

4.3.4.1 Trellis Encoding

The trellis encoder performs signal space coding based on a finite state machine (convolutional encoder). The rate 1/2 trellis encoder introduces redundancy and dependence of the successive symbols by its state memory. Coding gain is achieved by convolutional encoding and due to constellation design.

4.3.4.2 Viterbi Decoding

Viterbi decoders allow optimum decoding of convolutional codes in the receiver. The Viterbi algorithm is a sequential trellis search algorithm for performing maximum likelihood sequence detection.

4.3.4.3 Echo Cancellation

Echo cancellation enables bidirectional data transmission using the same frequency band. An echo is an undesired interference of the transmit data signal into the receiver through the hybrid. The adaptive echo canceller generates a replica of the echo which is subtracted from the receiver input to yield an echo-free signal.

4.3.4.4 Tomlinson Precoding

The trellis encoding and Viterbi decoding does not allow the use of a decision feedback equalizer in the receive path. Transmitter precoding (Tomlinson-Harashima coding) achieves a performance essentially identical to the decision feedback equalization by moving the feedback filter to the transmitter.

4.3.4.5 Scrambling/Descrambling

A maximum-length shift register is used on the input bit stream to “randomize” or “whiten” the statistics of the data, making it look more random. Scrambling of the transmitted signal is reversed by a descrambler at the receiver.

4.3.4.6 Decimation and Filtering

Decimation reduces the data rate of the highly oversampled bit stream provided from the Sigma-Delta Analog to Digital Converter. All of the out of band noise is eliminated within the filter stages.

4.3.4.7 Interpolation and Noise Shaping

The data rate is increased to get the oversampled data which is necessary for the digital to analog conversion.

4.3.4.8 HDLC Controller for EOC

This HDLC controller (for each channel separate) handles EOC messages in an HDLC-like format as defined in ITU-T G.997.1 paragraph 6.2 and standardized in ITU-T G.991.2, ITU-T G.shdsl.bis and ETSI TS 101 524.

It performs the following framing functions: flag generation/recognition, byte stuffing and CRC check.

One FIFO for the receive and one for the transmit direction are implemented to allow EOC messages of every length to be transported within one HDLC frame.

4.3.5 On-Chip Biterror Tester

An on-chip biterror tester is available for each channel.

In the biterror test mode scrambled ones or zeros are transmitted in the payload data stream.

The receiver counts the received zeros and ones of the payload data as failed bits within a counter period of *n**6 ms (BERT Counter), where *n* is any programmable integer value between 1 and 65536.
The counter stops if its maximum value is reached within one counter period.

For host access the BERT Counter value is stored in the BERT register at the end of the counter period and the BERT Counter is restarted.

While BERT is enabled ’1’ are transmitted to the Serial Data Interface.

The principle of the on-chip biterror tester is shown in **Figure 41**.

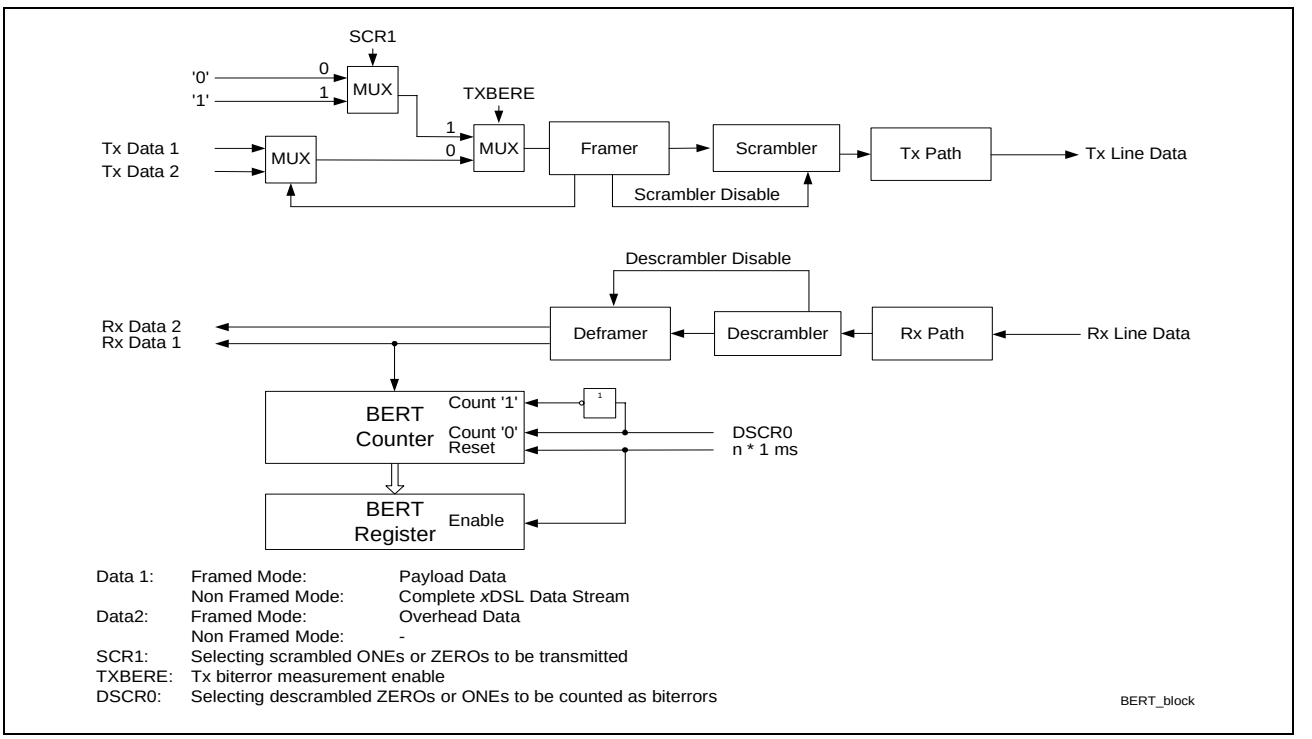


Figure 41 Block Diagram, Biterror Test

4.3.6 Embedded Microcontroller

For preactivation (G.hs), activation/deactivation and the HDLC handling of the EOC channel one controller for each symDSL channel is integrated.

Before activation the firmware for the microcontroller has to be downloaded from the host via SCI to the integrated memory.

4.4 Functional Description, Analog Front End (AFE)

4.4.1 Block Diagram of the AFE

Beside the 20.48 MHz clock the AFE is identical for each channel (see **Figure 43** and **Figure 44**). For channel 0 an oscillator is implemented in addition. The 20.48 MHz clock of channel 0 is supplied to all other channels and to pin CLKOUT (see **Figure 42**).

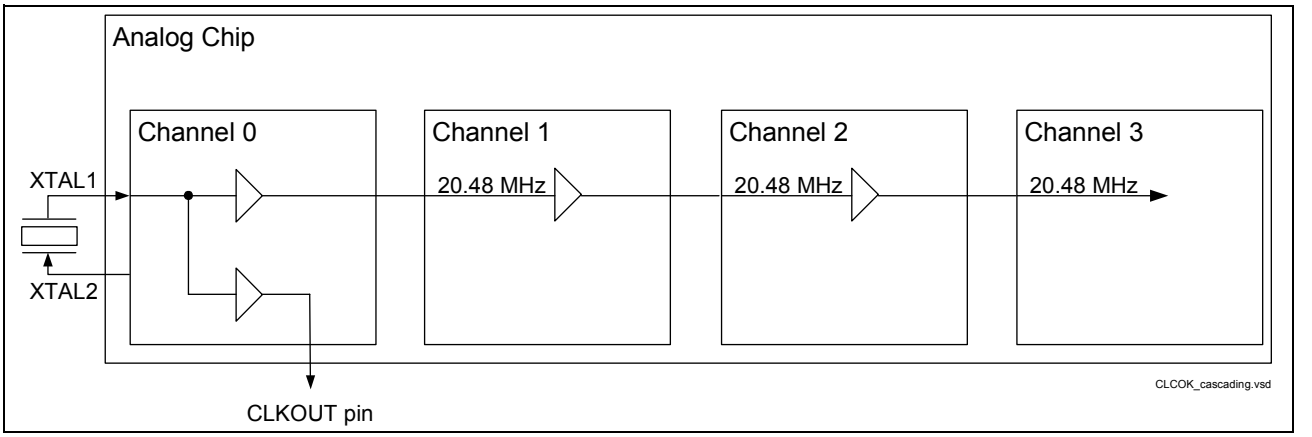


Figure 42 Clock Cascading of the 20.48 MHz Clock

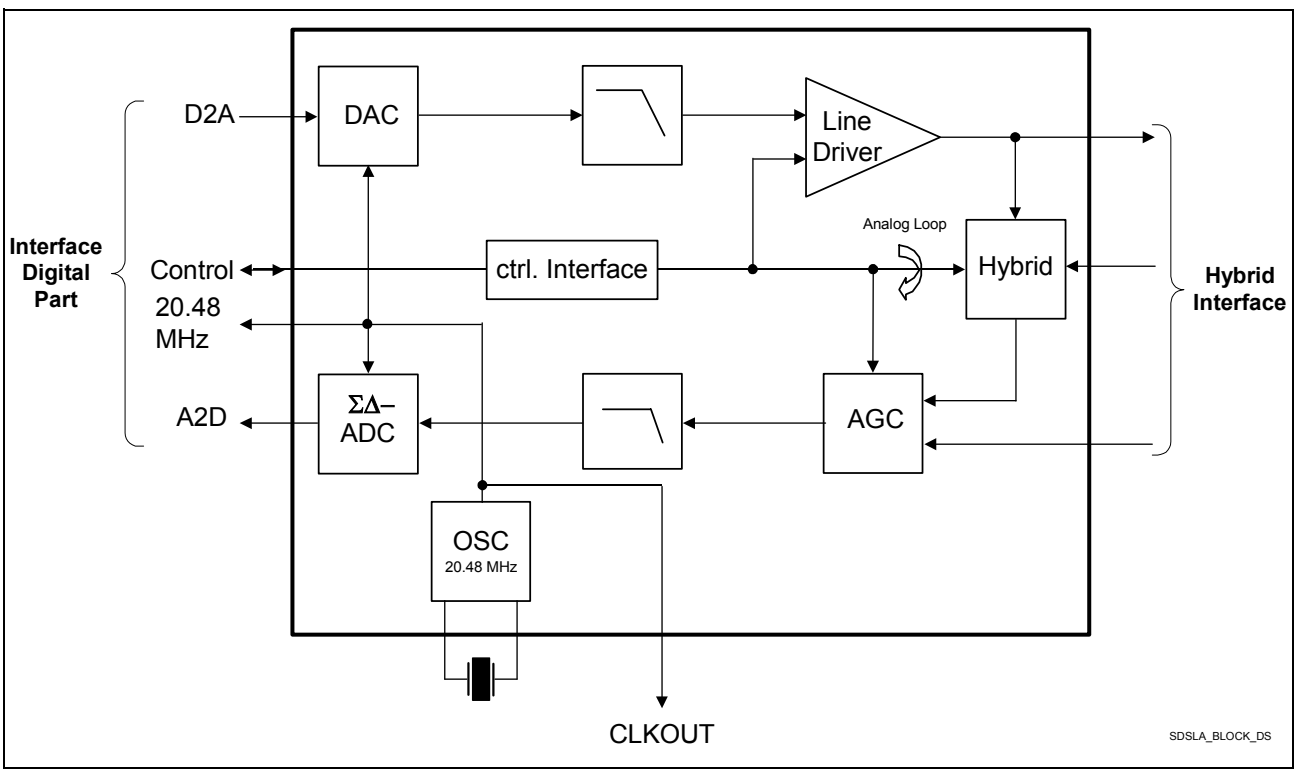


Figure 43 Block Diagram of the Analog Part of Channel 0

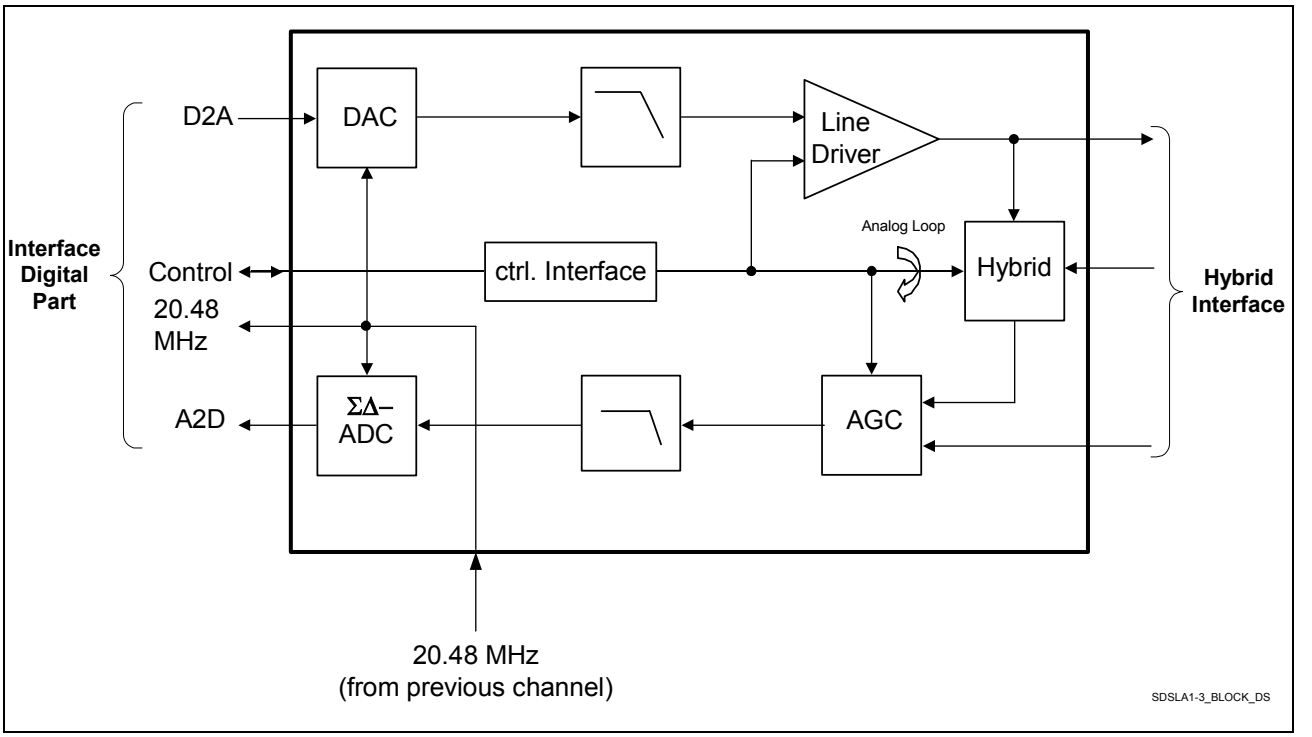


Figure 44 Block Diagram of the Analog Part of Channel 1, 2 and 3

4.4.2 Features

The integrated analog front end is designed for symDSL applications with data rates up to 2 MBaud/s. All symmetrical and asymmetrical PSDs are supported according to ITU-T G.991.2, ITU-T G.shdsl.bis and ETSI TS 101 524.

It integrates all receive and transmit functional blocks:

- Automatic Gain Control, AGC
- Filtering
- Analog to Digital Conversion, ADC
- Digital to Analog Conversion, DAC
- Crystal Oscillator, XOf = 20.48 MHz ± 60 ppm over temperature and aging[1)]
- Hybrid, automatically tuned to the real line conditions
- Line driver

4.4.3 Digital/Analog Converter DAC

The digital symbols are transformed to an analog symbol via a low power multi bit current steering DAC, which has high resolution and is highly linear in order to maximize the echo cancellation. A differential type of line driver with a high current driving capability and low distortion characteristics drives the subscriber lines.

1) For a detailed specification of the crystal refer to **Chapter 7.7**

4.4.4 Line Driver

A differential type of line driver with a high current driving capability and low distortion characteristics drives the subscriber lines. This line driver also supports HDSL (ETSI TS 101 135, ETSI TS 101 135) and HDSL2/HDSL4 (T1E1.4/2001-006R3).

4.4.5 Analog/Digital Converter ADC

The analog input from the Automatic Gain Control amplifier is converted into digital data by a third order sigma-delta modulator. The converter's sampling rate is 20.48 Mhz.

Oversampling reduces the amount of quantization noise power present in the signal band. Noise shaping further attenuates quantization noise in the signal band, thereby pushing noise power to out-of-band frequencies. The noise power, that is pushed outside the signal band can be attenuated by a digital filter such that it has no further effect on the signal.

4.4.6 Analog Echocanceller (HYBRID)

The dominant disturber in duplex data transmission over twisted-pair cables is the echo leaking from the transmitter into the receiver. Therefore a B-Filter (Balancing Filter, adaptive hybrid) is implemented in each analog part. Adaptivity is essential as the input impedance of the loop depends on the wire gauge, gauge changes and the presence/ absence of bridged taps. The adaptation algorithm is handled by the datapump at system startup.

4.5 External Circuitry (for Analog Part and Power Supply)

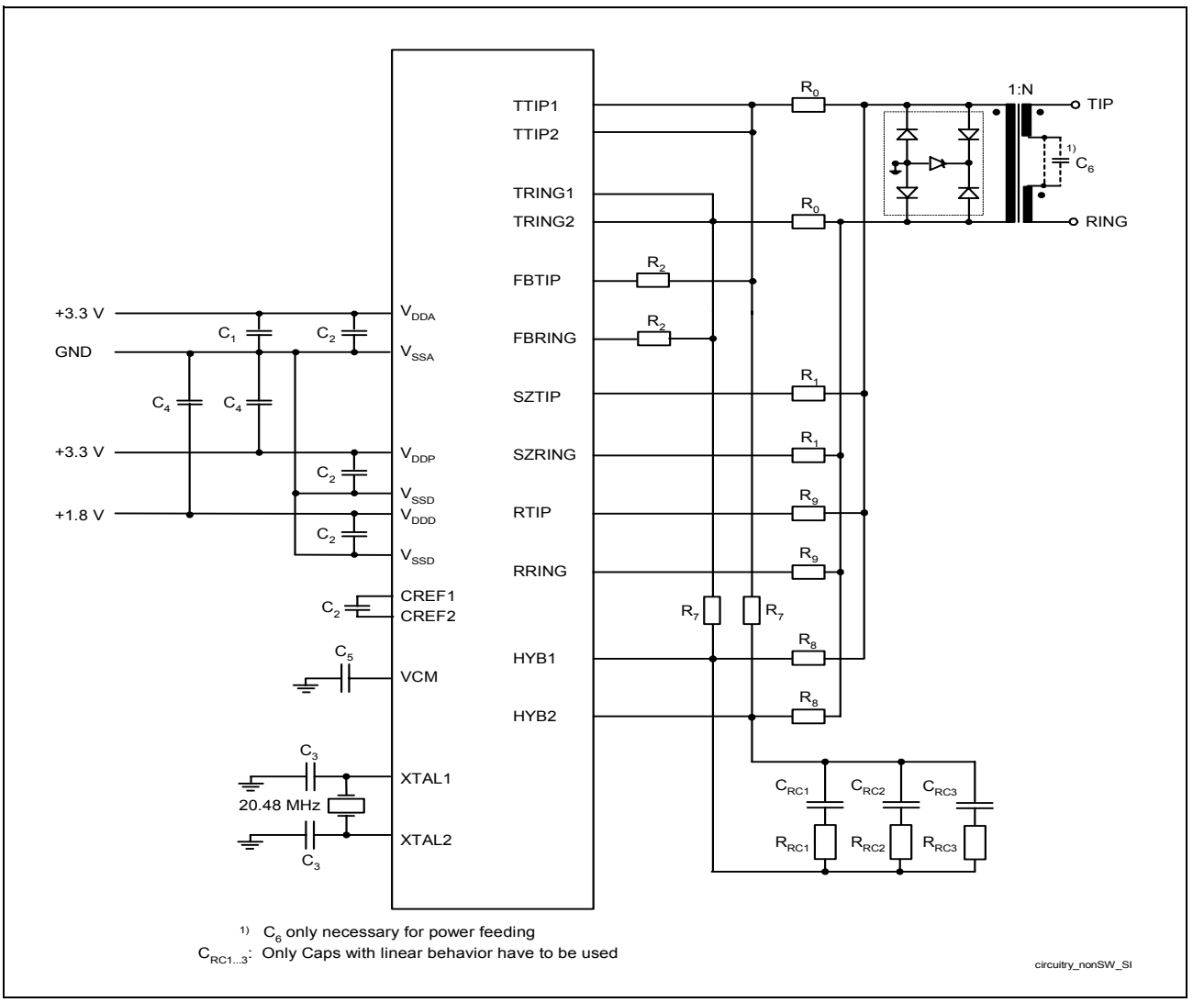


Figure 45 External Circuitry for one Channel

Note: Only passive components are necessary.

The values of **Table 17** are recommended for all applications using symmetrical PSDs.

Table 17 External Circuitry

Symbol	Value[1)]	Unit	Tolerance
N	4.5		+/- 1.5 %
R_0	2.3	W	+/- 1 %
R_1	43	W	+/- 1 %
R_2	T.B.D. (for future use. Do not mount in the meanwhile)	W	+/- 1 %
R_7	750	W	+/- 1 %
R_8	3.3	kΩ	+/- 1 %
R_9	787	W	+/- 1 %
R_{RC1}	3.3	kΩ	+/- 1 %
R_{RC2}	6.2	kΩ	+/- 1 %
R_{RC3}	14	kΩ	+/- 1 %
C1	220[2)]	µF	+/- 20 %
C2	100	nF	+/- 20 %
C3	6.8	pF	+/- 5 %
C4	4.7	µF	+/- 20 %
C5	100	nF	+/- 10 %
C6	1[3)]	µF	+/- 10 %
C_{RC1}	2.2	nF	+/- 5 %
C_{RC2}	1.2	nF	+/- 5 %
C_{RC3}	560	pF	+/- 5 %

1) $C_{RC1...3}$: Only capacitors with linear behavior have to be used

2) Recommended size, smaller values are possible

3) C_6: Required for span powering only

5 Interface Description

The interfaces provided by the SDFE-4 are described in this chapter.

5.1 Serial Control Interface (SCI)

One SCI exists for the 4-channel SDFE-4. Control information for the symDSL channels as well as data for the firmware download will be exchanged HDLC framed via this interface. The SDFE-4 is configured and maintained by appropriate messages which are described in the Programmer Reference which is provided by Infineon.

5.1.1 SCI Functionality

In some cases the internal controllers have to communicate with each other to exchange messages, for example in the *M*-pair mode. This communication beside the communication with the external host controller is performed via the external SCI. To avoid collisions the SCDI pin of the external SCI is combined by an logical AND with all outputs of the internal modules. This combined signal is transmitted via pin SCDO and fed back to the internal modules. The modules transmitting a logical ’1’ but receiving a logical ’0’ will stop transmission and will retry transmission after the next HDLC Stop Flag (see **Figure 46**).
This communication protocol is based on LAPD and according to ITU-T Recommendation I.430.

To ensure the message exchange between the host and the SDFE-4 the mechanism of collision detection and withdrawal from transmission in case of a collision have to be realized in the host controller as well. For collision detection the host controller has to use pin SCDO not only as the message direction from SDFE-4 to host but also as echo of the message transmitted by the host.

To connect more than one SDFE-4 to one SCI the pin SCDO of each SDFE-4 have to be combined by logical AND. Up to 15 SDFE-4 can be connected to one SCI. **Figure 47** shows an example with four SDFE-4 connected to one SCI.

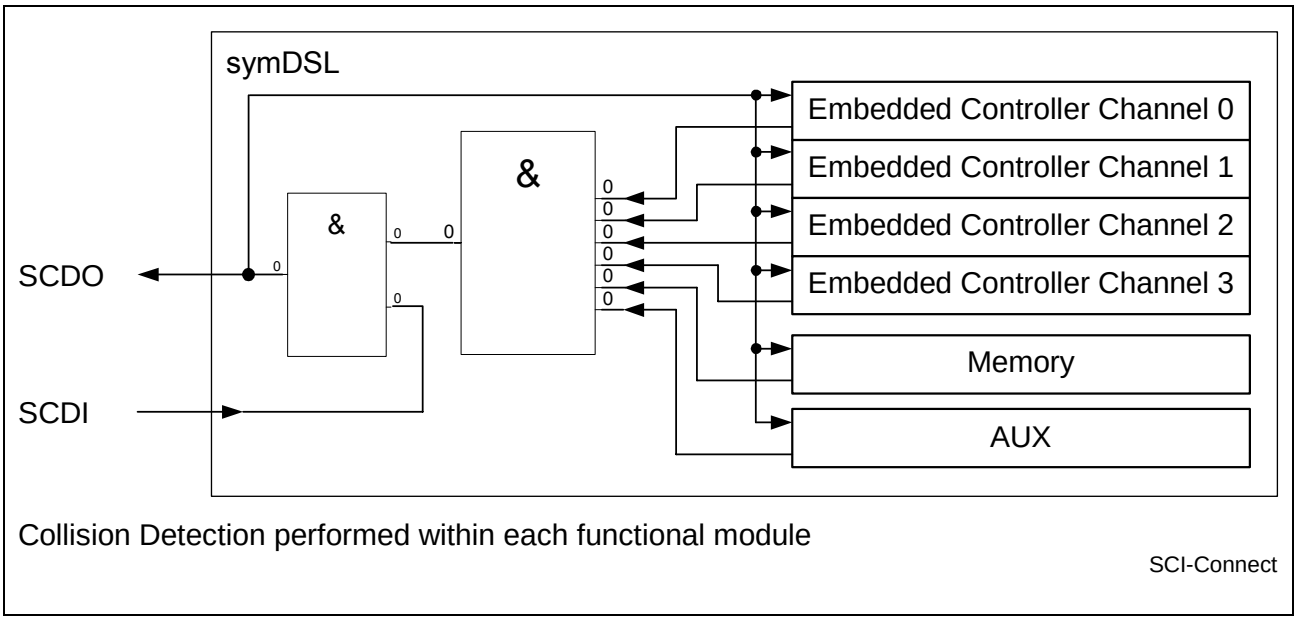


Figure 46 SCI Functionality

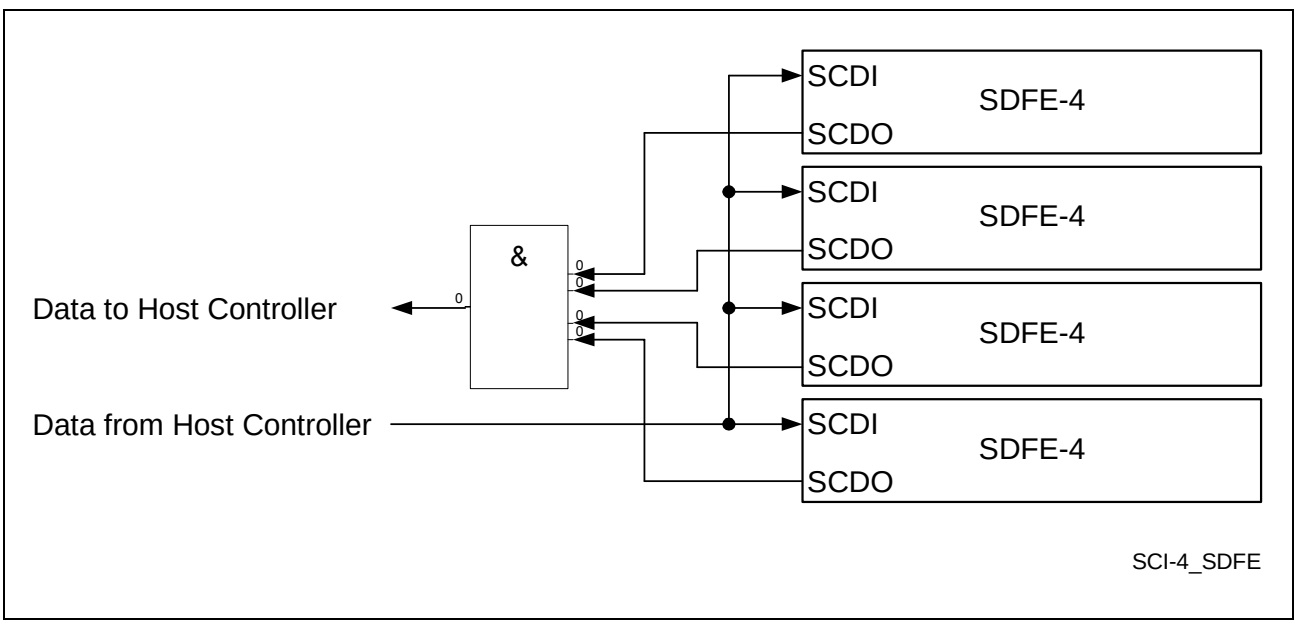


Figure 47 SCI with four SDFE-4

5.1.2 HDLC Protocol for SCI

The HDLC protocol used for SCI is according to ITU-T Recommendation Q.921. The header and payload bytes are transferred LSB first whereas the CRC is transferred MSB first. The HDLC frame is shown in **Figure 48**.

The address bytes are described in **Table 18**.

The entire receiver address field of the incoming HDLC frames is compared. Just frames whith DESTADDR which match the values of **Table 20** are accepted.

After transmission of the stop-flag continuous ONEs (at least nine ONEs) are used as inter-frame fill.

To decouple the SCI performance from the performance of the embedded controllers one 128 byte FIFO is implemented for the receive and one for the transmit direction for each controller. The FIFOs are implemented as cyclic buffers.

The AUX and RAM blocks are directly accessed.

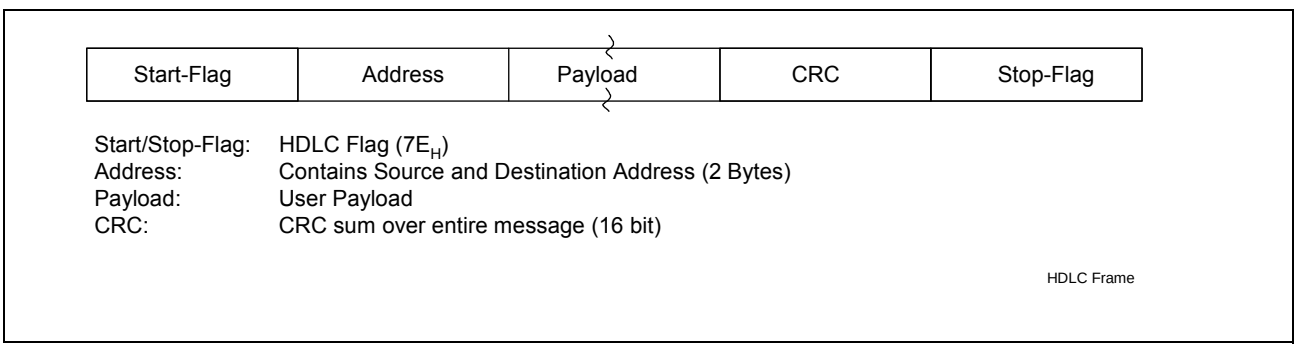


Figure 48 HDLC Frame

Table 18 Address Bytes

High Address Byte	Low Address Byte
SOURCEADDR	DESTADDR

SOURCEADDR Source Address (Address of Transmitter)

DESTADDR Destination Address (Address of Receiver)

5.1.3 Address Mapping

Each functional block of the SDFE-4 has its own address comprising the device address and the assigned block address.

The 4 bit device address allows the connection of up to 15 SDFE-4 to one SCI. The chip address is latched in from pins AUX_0_[5], AUX_1_[5], AUX_2_[5] and AUX_3_[5] during reset, i.e. the appropriate device address has to be set by external pull-ups and pull-downs to these AUX pins (see **Table 19**). Integrated pull-ups set the device address to F_H by default.

The device address F_H is the broadcast address which is for example useful for firmware download to all connected SDFE-4 in parallel.

Table 19 AUX Mapping to Device Address during Reset

AUX Pin	Device Address Bit
AUX_3_[5]	Bit 3 (MSB)
AUX_2_[5]	Bit 2
AUX_1_[5]	Bit 1
AUX_0_[5]	Bit 0 (LSB)

The addresses of the chip internal functional blocks are as follows:

Table 20 SCI Address Mapping

Modul	Address[1)]
Embedded Controller Channel 0	$x2_H$
Embedded Controller Channel 1	$x6_H$
Embedded Controller Channel 2	xA_H
Embedded Controller Channel 3	xE_H
Memory	$x5_H$
AUX	$x9_H$
External Controller (Host)	$x1_H$

1) *x* is the device address of the SDFE-4 which is determined by pins AUX_0_[5], AUX_1_[5], AUX_2_[5] and AUX_3_[5] during reset
The device address F_H is used as braodcast address, i.e. each SDFE-4 connected to the same SDI is accessed by the device address F_H.

5.2 Serial Data Interface (SDI)

One SDI exists for each symDSL channel. The configuration of the SDI are identical for all symDSL channels. The following configurations are selectable:

- TDM interface
- Bit Serial
- DSL3 interface (for regenerator applications)

The appropriate pin assignment for all TDM pins beside DIN_# and DOUT_#, i.e. the pins for TDM frame synchronization and symDSL synchronization is described in **Table 21**.

Two, three or four symDSL channels can be combined to one TDM interface to realize the 2-, 3- or 4-pair mode.

Two or four symDSL channels can be combined to one TDM interface to realize a TDM bus configuration.

5.2.1 Clock Multiplexing for Receive Direction

In *M*-pair or TDM bus mode the symDSL frames have to be synchronous to each other to avoid bit slips in case of symDSL frame wander.

To synchronize all symDSL channels which belong to the same *M*-pair or TDM bus group, only one receive clock for all group members has to be applied. The multiplexer structure for the receive clock is shown in **Figure 49**.

In transmit direction the clocks of the appropriate SDI blocks have to be connected together externally.

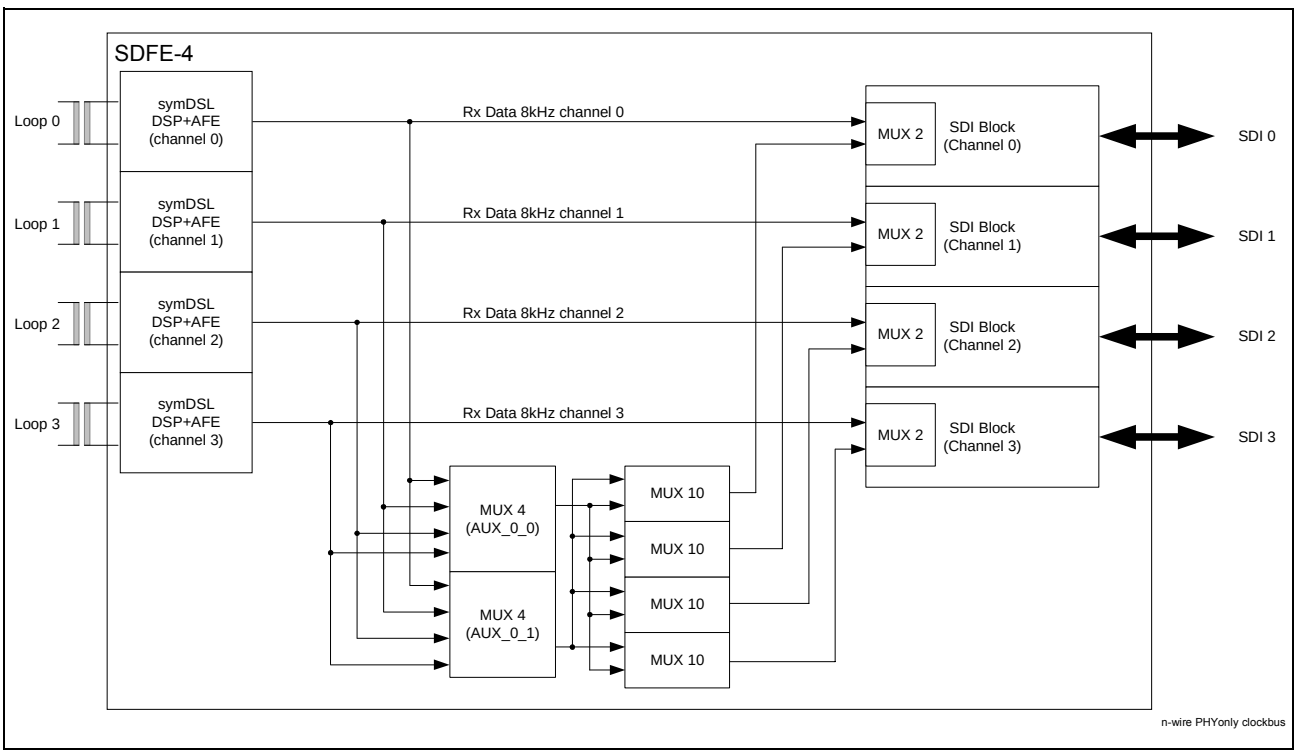


Figure 49 Receive Clock Multiplexing for *M*-Pair and TDM Bus

5.2.2 SDI in DSL3 Mode

The SDI in DSL3 mode is only supported for regenerator applications. In this mode pin DIN of the SRU-C can be connected directly to pin DOUT of the SRU-R and pin DOUT of the SRU-C can be connected directly to pin DIN of the SRU-R. Additionally to the payload data the clock and frame clock information is coded in the DSL3 data stream and therefore no additional clock or frame clock pins are necessary.

5.2.2.1 Clocking, SDI in DSL3 Mode

In DSL3 mode no clock pin is used. The clock, frame clock and symDSL frame clock are coded in the DSL3 data stream.

However for *M*-pair or TDM bus configuration the receive clock multiplexer described in **Chapter 5.2.1** has to be programmed for the internal receive clocks.

5.2.3 SDI in TDM or Bit Serial Mode

Functional List of TDM Interface Block

- One TDM interface for each loop interface.
- Interface ports can be configured for T1/J1 (1.544 MHz), PCM Highway -E1 (2.048, 4.086, 8.192, 16.384 MHz), bit serial mode (Data Rate TDM = symDSL payload data rate)
- Except in bit serial mode all interface ports provide 8 kHz TDM and/or 6 ms symDSL frame synchronization
- Serial data and synchronization pulses sampled/transmitted with rising or falling edge of clocks (programmable)
- Positive or negative polarity of data clocks and frame synchronization pulses (programmable)
- Programmable DIN_#/DOUT_# bitshift of +3/-4-bits relative to the TDM synchronization pulse
- Prgrammable payload shift when working in fractional or channelized mode (bus modes, payload interleaved, byte interleaved)
- symDSL alignment of the loop interface
- programmable Z-Bit position
- SDI and remote payload loop back per port

5.2.3.1 Clocking, SDI in TDM or Bit Serial Mode

In general the clock and frame clocks for transmit are inputs and for receive outputs.

For all framing modes but Bit Serial Mode the following frame synchronization modes are supported:

- Use of the 8 kHz TDM frame synchronization pulses for payload synchronization (pin RFSC_# and TFSC_#) and the 6 ms symDSL frame synchronization pulses (pin RSFSC_# and TSFSC_#)
- Use of the 8 kHz TDM frames synchronization pulses for payload synchronization only (pin RFSC_# and TFSC_#)
  The symDSL frame is not synchronized to any TDM frame
- Use of the 6 ms symDSL frame synchronization pulses only (pin RSFSC_# and TSFSC_#)

The following TDM clock frequencies are supported:

- 1.544 MHz clock, 193 bits / 125 µs frame
- 2.048 MHz clock, 256 bits / 125 µs frame
- 2.312 MHz clock, 289 bits / 125 µs frame
- 4.096 MHz clock, 512 bits / 125 µs frame
- 8.192 MHz clock, 1024 bits / 125 µs frame
- 16.384 MHz clock, 2048 bits / 125 µs frame

5.2.3.2 Framing Modes

The following formats are supported:

- T1 mode (TDM framed or symDSL framed mode - 48 T1 frames per symDSL frame)
- PCM Highway (E1 mode, TDM framed or symDSL framed mode - 48 E1 frames per symDSL frame)
- Bit Serial Mode (no framing information provided in this mode)

The data transmission format of the TDM interface in T1 operation is shown in **Figure 50**. TDM interface in E1 operation is shown in **Figure 51**.

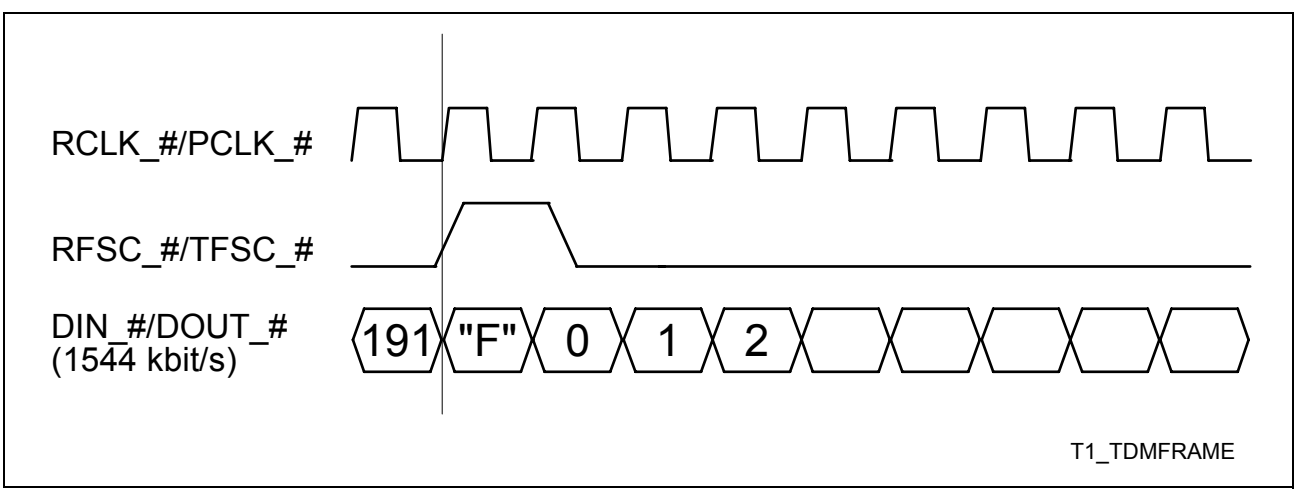


Figure 50 T1 Framing

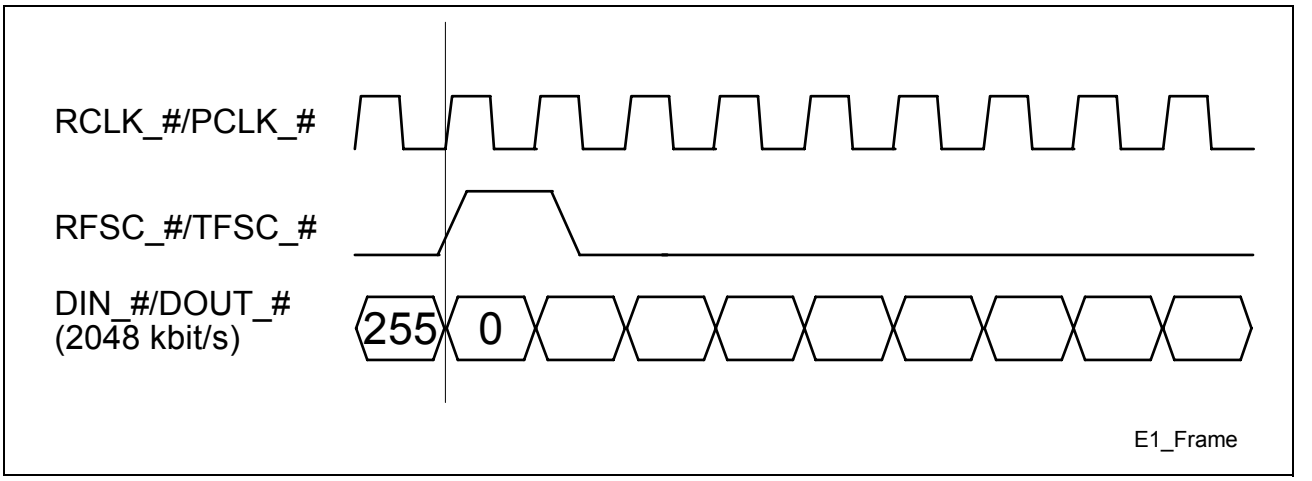


Figure 51 E1 Framing

The following figures shows the use of bit shift, byte offset and Z-bit alignment. Byte offset and therefore different bus modes can be adjusted with physical channels.

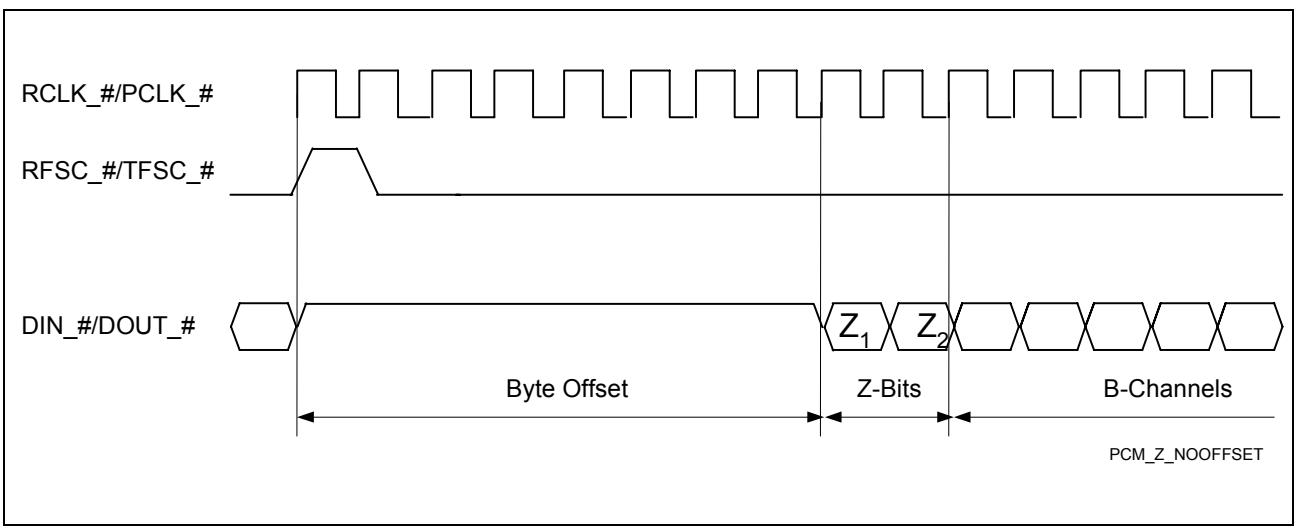


Figure 52 Example for Byte Offset, Z Bits Not Octet Aligned

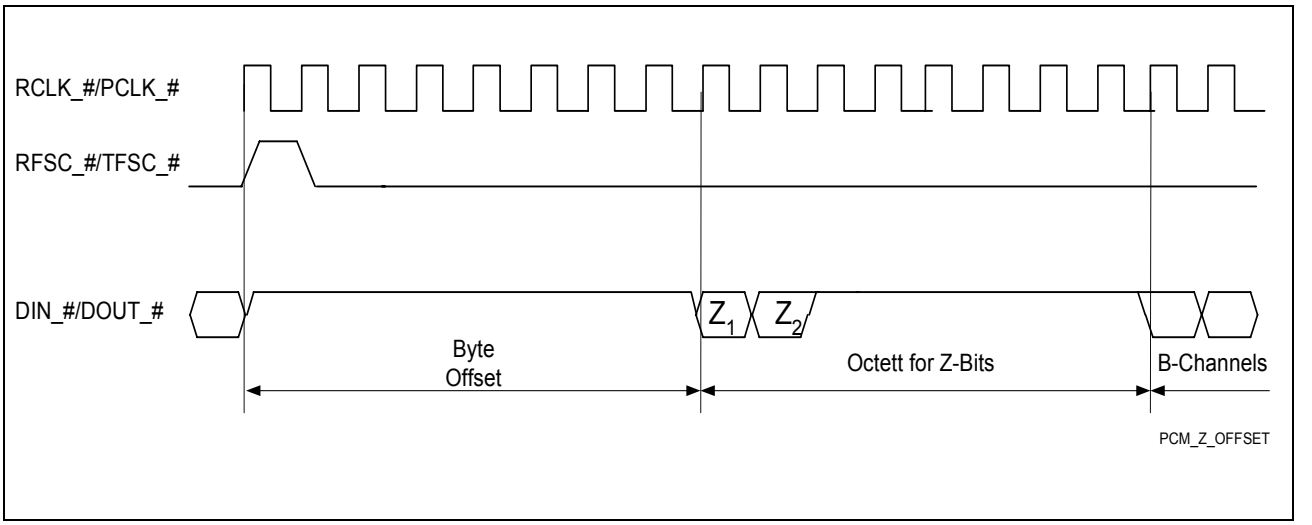


Figure 53 Example for Byte Offset, Z Bits Octet Aligned

In Bit Serial Mode no framing information is necessary. Therefore provided frame synchronization pulses will be ignored. Bit shift and byte offset are ignored, all bits are driven/sampled. The bit clock frequency is equal to the symDSL payload bit rate. **Figure 54** shows the Bit Serial Mode with a data rate of 1024 kBit/s.

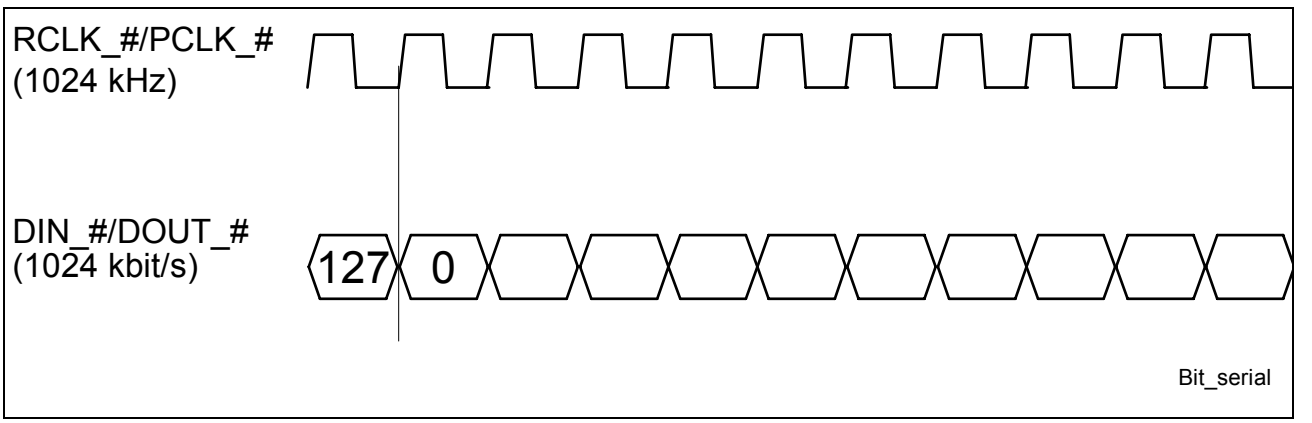
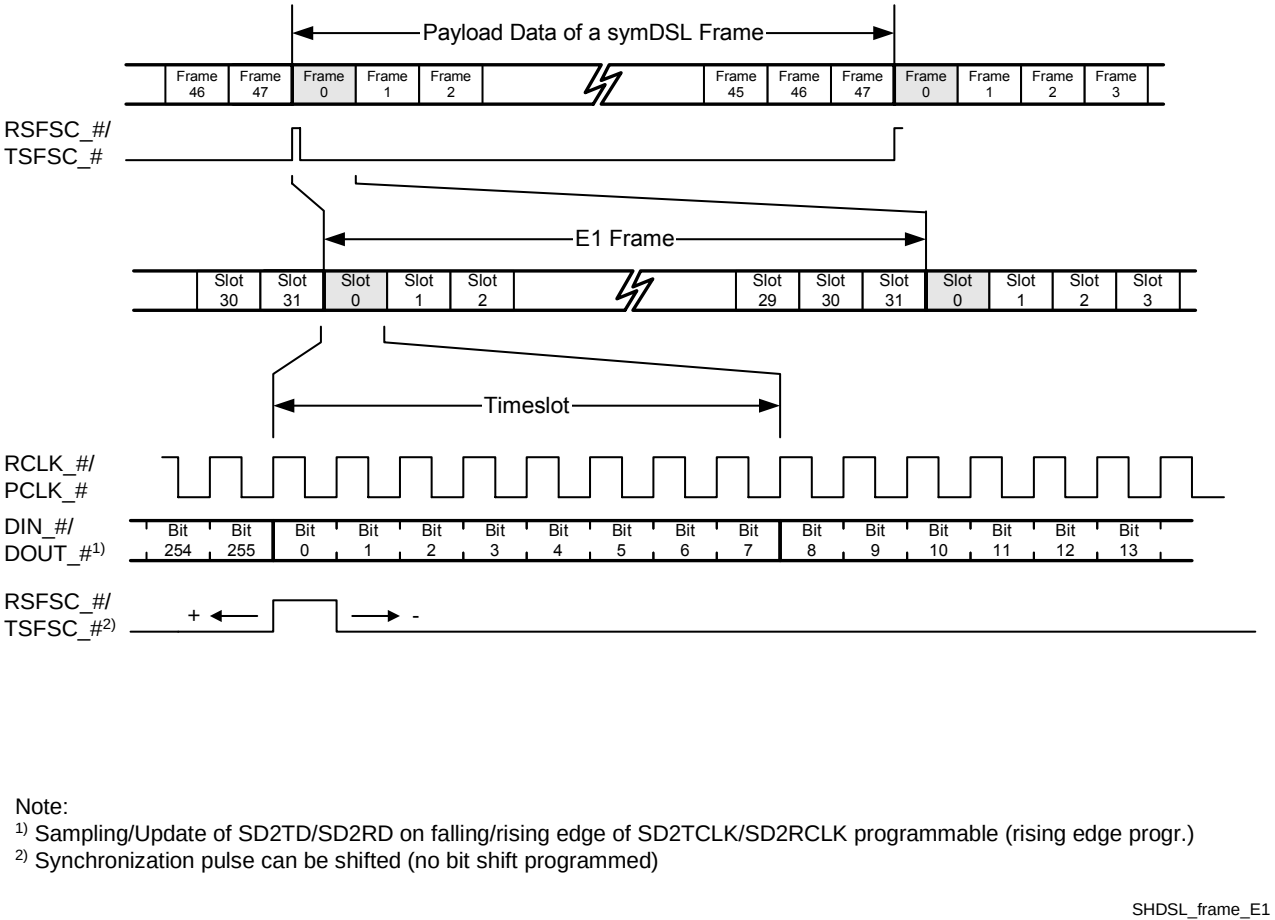


Figure 54 Bit Serial Mode

5.2.3.3 symDSL Framing Mode

Instead of applying the 8 kHz TDM frame synchronization pulse and the 6 ms symDSL frame synchronization pulse in addition, it is possible to apply the 6 ms symDSL frame synchronization pulse only.

A symDSL frame contains payload data of 48 TDM frames. Therefore the symDSL Frame Mode consists of 48 TDM frames. The following figures show the TDM frame data mapping from/to the symDSL frame.



Note:
1) Sampling/Update of SD2TD/SD2RD on falling/rising edge of SD2TCLK/SD2RCLK programmable (rising edge progr.)
2) Synchronization pulse can be shifted (no bit shift programmed)

SHDSL_frame_E1

Figure 55 symDSL Frame Mode, E1 over symDSL

Figure 56 shows a configuration where the external TDM interface works with f = 4.096 MHz, but only 36 timelsots are driven/sampled. This corresponds to a payload of 2.304 MBit/s. This 2.304 MBit/s data stream can be shifted within this 4.096 Mbit frame with bit granularity.

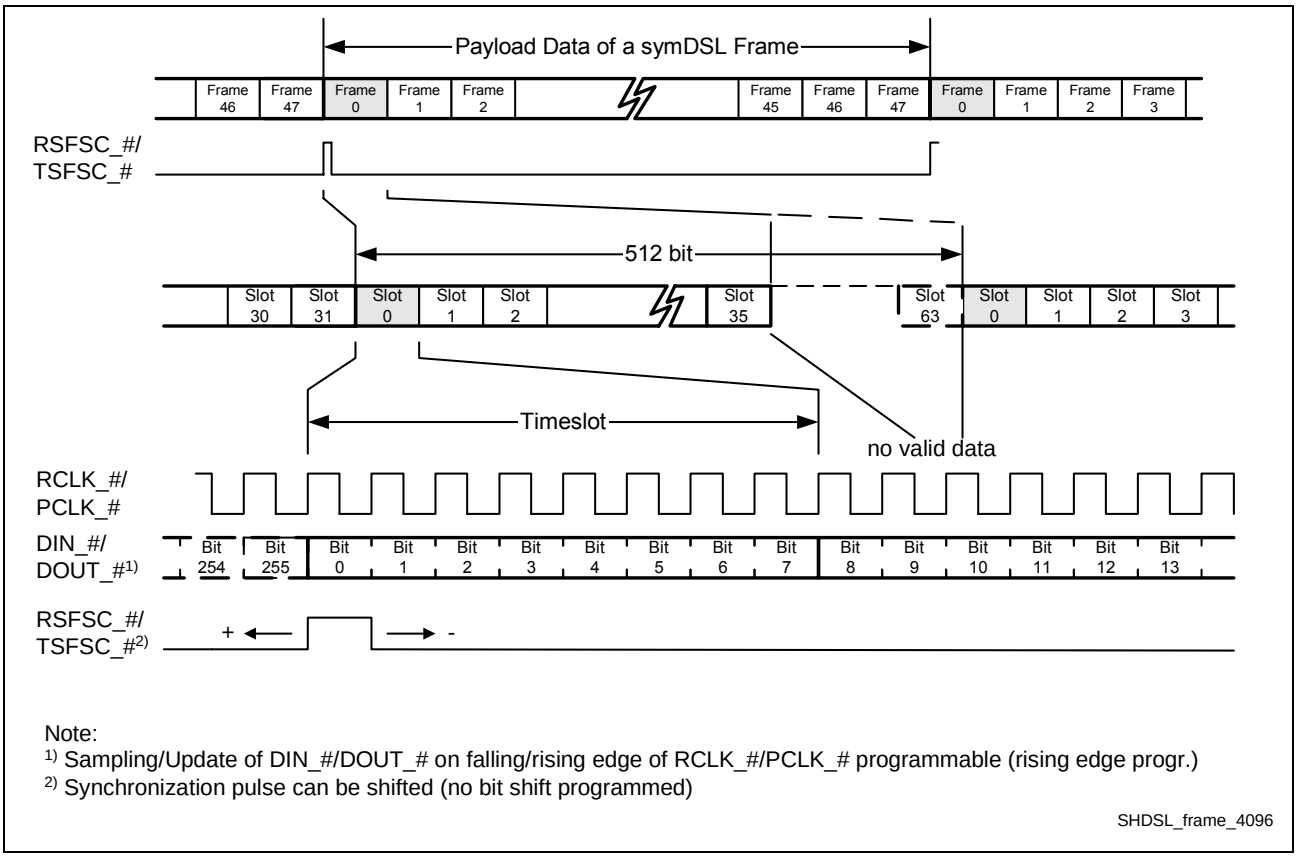


Figure 56 symDSL Frame Mode, TDM Frequency 4.096 MHz

5.2.3.4 TDM Bus Configuration

For normal TDM bus application (not *M*-pair mode) byte interleaved, bit interleaved and bitstream interleaved is supported according to **Table 24**.

Either two or four channels can be combined to one TDM bus.
In case of combining two TDM interfaces to one TDM bus, channel 0 and 1 use TDM interface 0 as their TDM bus interface and channel 2 and 3 use TDM interface 2 as their TDM bus interface.
If all four channels are combined to one TDM bus, TDM interface 0 is used as TDM bus interface.

In applications using the receive clocks synchronized to the loop interface for the TDM interface, e.g. NTU (STU-R) or plesiochronous mode, the receive clock of each master channel of the TDM bus groups supplies the appropriate complete TDM bus group.

5.3 Auxiliary Interface (AUX)

When the SDI is in DSL3 mode (only useful for regenerators) the AUX interface is accessible by the host via SCI.

When the SDI is in TDM or Bit Serial mode no host access to the AUX interface is possible. The appropriate pin assignment is according to **Table 21**.

Table 21 AUX Pin Assignment for the supported SDI Modes

SDI Interface Mode	Pins	Dir.[1)]	Description
DSL3	AUX_#_0	I/O	Host Access
	AUX_#_1	I/O	Host Access
	AUX_#_2	I/O	Host Access
	AUX_#_3	I/O	Host Access
	AUX_#_4	I/O	Host Access
	AUX_#_5	I/O	Host Access
TDM and Bit Serial	AUX_#_0	I	TSFSC_#, Tx symDSL 6 ms frame synchronization pulse
	AUX_#_1	I	TFSC_#, Tx TDM 8 kHz frame synchronization pulse
	AUX_#_2	I	PCLK_#, Tx data clock
	AUX_#_3	O	RSFSC_#, Rx symDSL 6 ms frame synchronization pulse
	AUX_#_4	O	RFSC_#, Rx TDM 8 kHz frame synchronization pulse
	AUX_#_5	O	RCLK_#, Rx data clock

1) I stands for input, O for output and I/O for input or output

5.4 JTAG Interface

The boundary scan functionality is implemented according to IEEE 1149.1, using a 5-pin test access port. The necessary signals are described in **Table 22**

Table 22 Boundary Scan Interface

Symbol	Name	Function
TRST	Test Reset	TAP Controller with instruction, bypass and identification register
TCK	Test Clock	
TMS	Test Mode Select	

Table 22 Boundary Scan Interface (cont'd)

Symbol	Name	Function
TDI	Test Data IN	Boundary scan chain
TDO	Test Data Out	

5.4.1 Boundary Scan Test Mode

The desired test mode is selected by serially loading a 4 bit instruction code into the instruction register via JTEST2 (TDI) (LSB first)

Table 23 Boundary Scan Test Modes

Code	Instruction	
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code register
0100	CLAMP	
0101	HIGHZ	
1111		Bypass operation
others		*For test purposes only, not accessible to customers*

5.4.2 Boundary Scan Identification Register

The identification register than can be serially read out via pin TDO contains the following value:

Version	Device Code	Manufacture Code		Output
0001	00000000 10101101	0000100 0001	1	-> TDO

5.5 Loop Interface

The following Loop Interface modes are supported:

- SHDSL (synchronous and plesiochronous) according to ITU-T G.991.2 and ITU-T G.shdsl.bis
- ETSI SDSL according to ETSI TS 101 524
- ANSI HDSL2/HDSL4 according to T1E1.4/2001-006R3
- HDSL according to ETSI TS 101 135, ITU-T G.991.1
- 2B1Q-SDSL
- Transparent (without any framing)

5.5.1 Loop Interface in *M*-Pair Configuration

The supported framing modes for the *M*-pair application are summarized in **Table 24**.

Table 24 TPS-TC Framing Modes for *M*-pair Applications

TPS-TC Framing	Interleaving Mode	Figure
TDM, Clear Channel Byte-Oriented Data	Byte interleaved	**Figure 57**
TDM, HDSL4 Replacement	1st bit[1] (Framing bit): identical[2] Data:Bit interleaved	**Figure 58**
TDM, Clear Channel Data	Bitstream interleaved	**Figure 59**
TDM, Unaligned DS1[3] Transport	*Not supported in M-pair mode according to ITU-T G.shdsl.bis*	
TDM, Aligned / Fractional DS1 Transport (*n*T1)	1st bit[1] (Framing bit): identical[2] Data: byte interleaved	**Figure 60**
TDM, 2048 kbit/s Digital Unstructured Leased Line (D2048U)	Bitstream interleaved (same as for "TDM, Clear Channel Data")	
TDM, Unaligned 2048 kbit/s Digital Structured Leased Line (D2048S)	*Not supported in M-pair mode according to ITU-T G.shdsl.bis*	
TDM, Aligned 2048 kbit/s Digital Structured Leased line (D2048S)	Byte interleaved (same as for "TDM, Clear Channel Byte-Oriented Data")	

1) Equivalent to Z-bit(s)

2) 1st bit received on wire Pair 1 is the relevant one

3) DS1 also known as T1

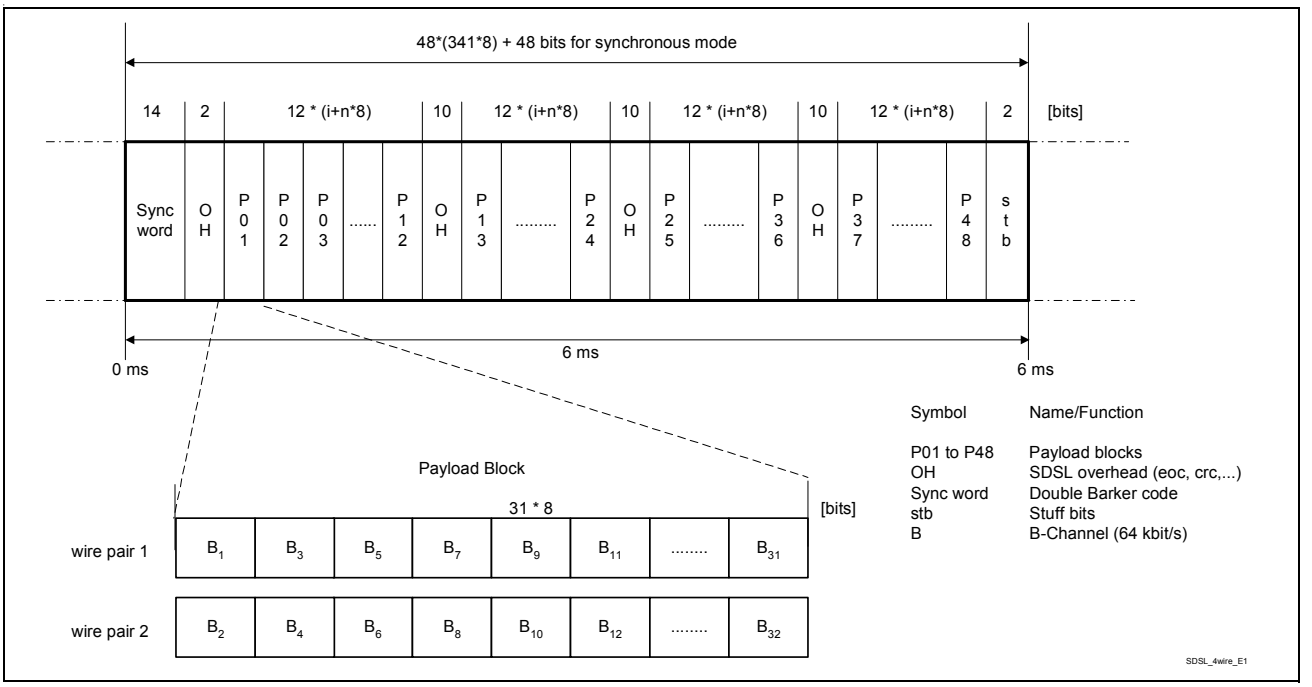


Figure 57 Clear Channel Byte-Oriented, S(H)DSL framed, 4-Wire

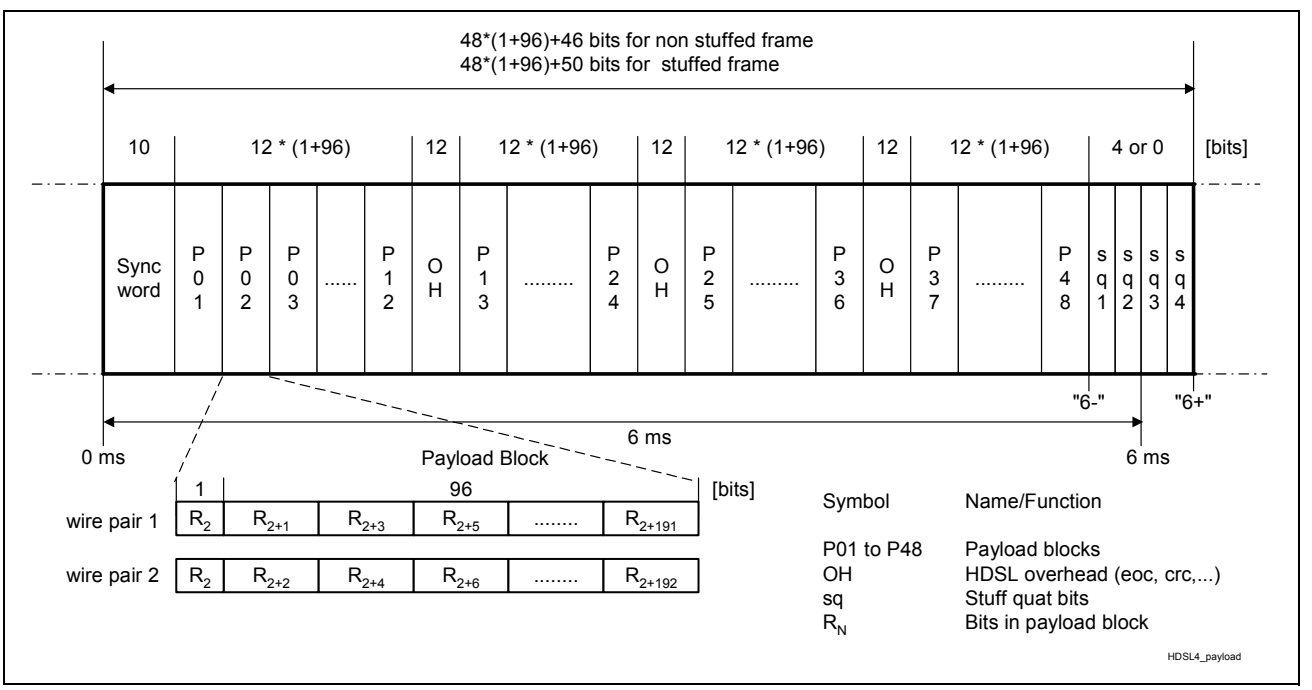


Figure 58 HDSL4 Replacement, HDSL2 Framed

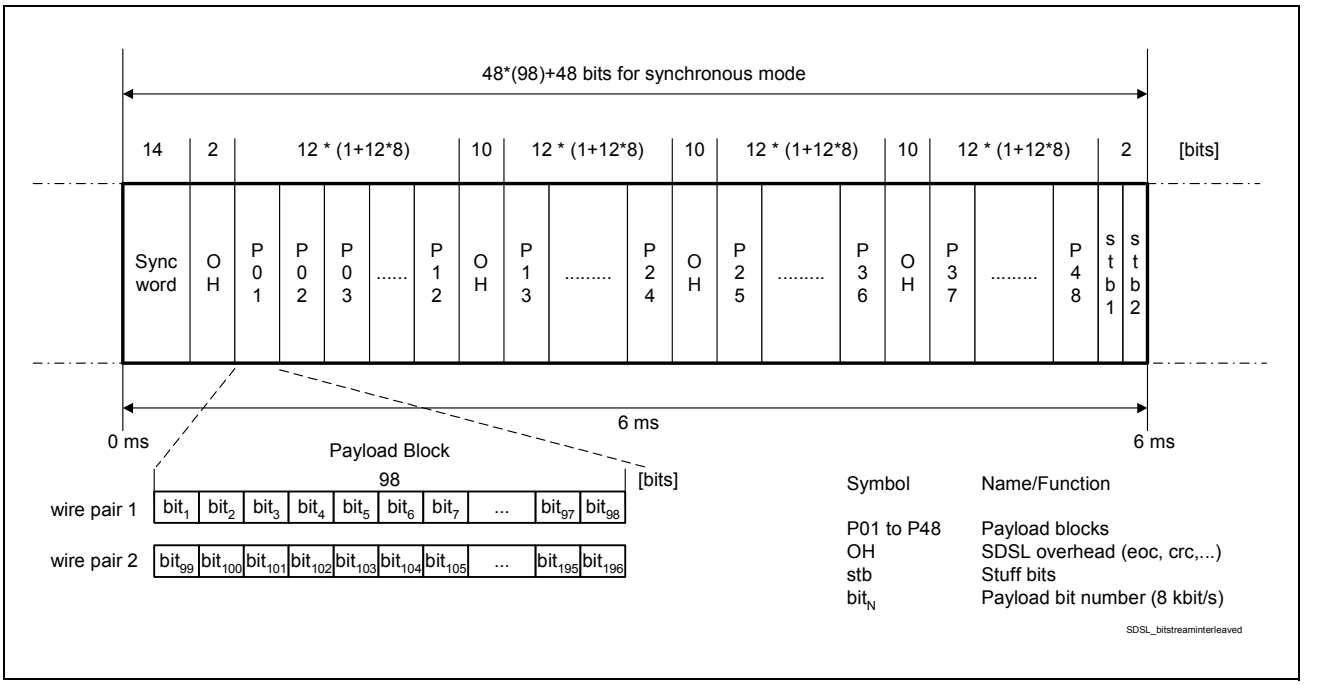


Figure 59 Clear Channel Data, S(H)DSL Framed, 4-Wire

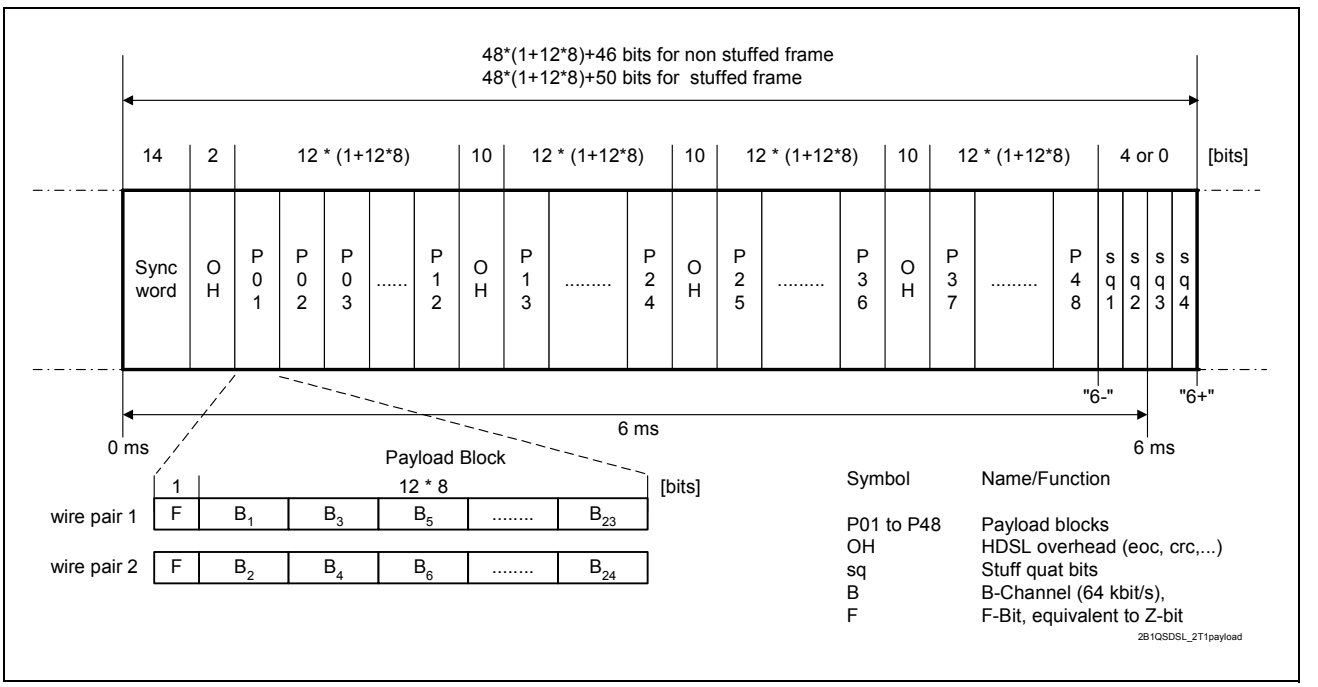


Figure 60 Fractional DS1 Transport (2T1), 2B1Q-SDSL Framed

6 Operational Description

The SDFE-4 is a chip which realizes the described functionality with hardware and firmware. The hardware of the SDFE-4 consists of interface blocks, functional building blocks and on-chip microprocessor core subsystems (embedded controllers). “Firmware” references code that is run on the embedded controllers.

To operate the SDFE-4 it is necessary to configure and maintain the device through the Serial Control Interface (SCI). Data to and from the SCI is HDLC framed (see **Chapter 5.1**). The SCI is a message based interface and allows an easy and efficient programming of the device via high level messages.

To support the system recovery mechanism for higher software layers a “Read-Back” functionality is realized which provides configuration parameters stored in the device.

A detailed description of the device control interface, all messages and application examples is given in the User’s Manual - Programmer’s Reference of SDFE-4.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 25 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min	max		
Max. Junction Temperature	T_J	-55	150	°C	-
Core supply voltage	V_{DD}	-0.3	2.4	V	-
I/O supply voltage	V_{DDP}/ V_{DDA}	-0.5	4.8	V	V
Voltage on any pin	V_{max}	-0.5	4.8	V	
Maximum DC current on any pin		-10	10	mA	
ESD robustness HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$		2000	V	According to EIA/JESD22-A114-B
ESD robustness	$V_{ESD,SDM}$		500	V	According to ESD Association Standard DS5.3.1 - 1999

Note: The maximum voltage difference must not exceed 4.8 V in any case (for example Supply voltage = 4.8 V and Input Voltage = -0.5 V is NOT allowed!)

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 Operating Range

Table 26 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias PEF	T_A	-40	85	°C
Core supply voltage	V_{DD}	1.71	1.89	V
I/O supply voltage	V_{DDP} V_{DDA}	3.13 3.13	3.47 3.47	V V
Ground	V_{SS}	0	0	V

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.2.1 Recommended Operation Conditions

The SDFE-4 meets all standards for operation in indoor and outdoor environments in communication systems.

7.3 Power Up

To avoid damage of the SDFE-4 during power up an external Schottky diode has to be applied beween the 3.3 V and 1.8 V power supplies (see **Figure 61**).

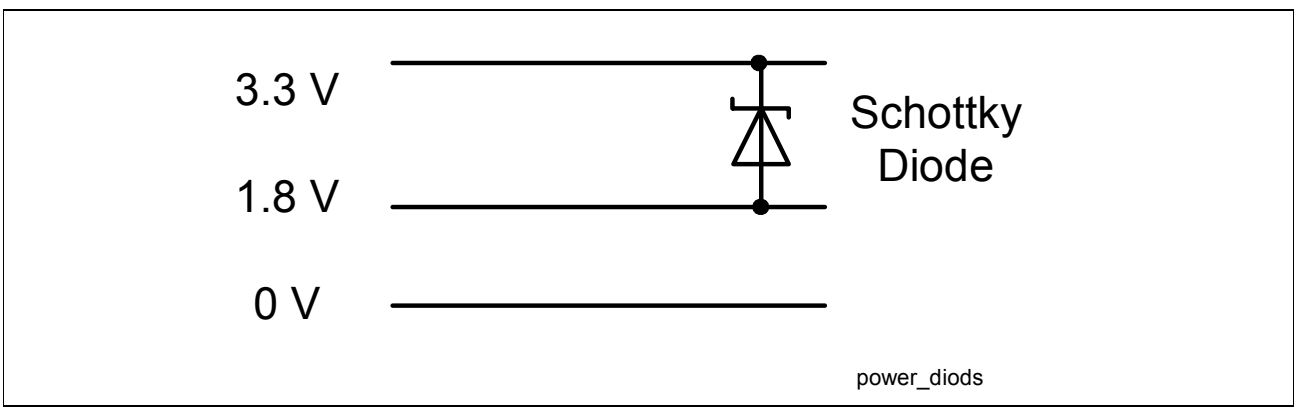


Figure 61 Circuit for Power Up

7.4 Line Overload Protection

The maximum input current for the loop interface (under over-voltage conditions) for the loop interface is given as a function of the width of a rectangular input current pulse. For the destruction current limits refer to **Figure 62**.

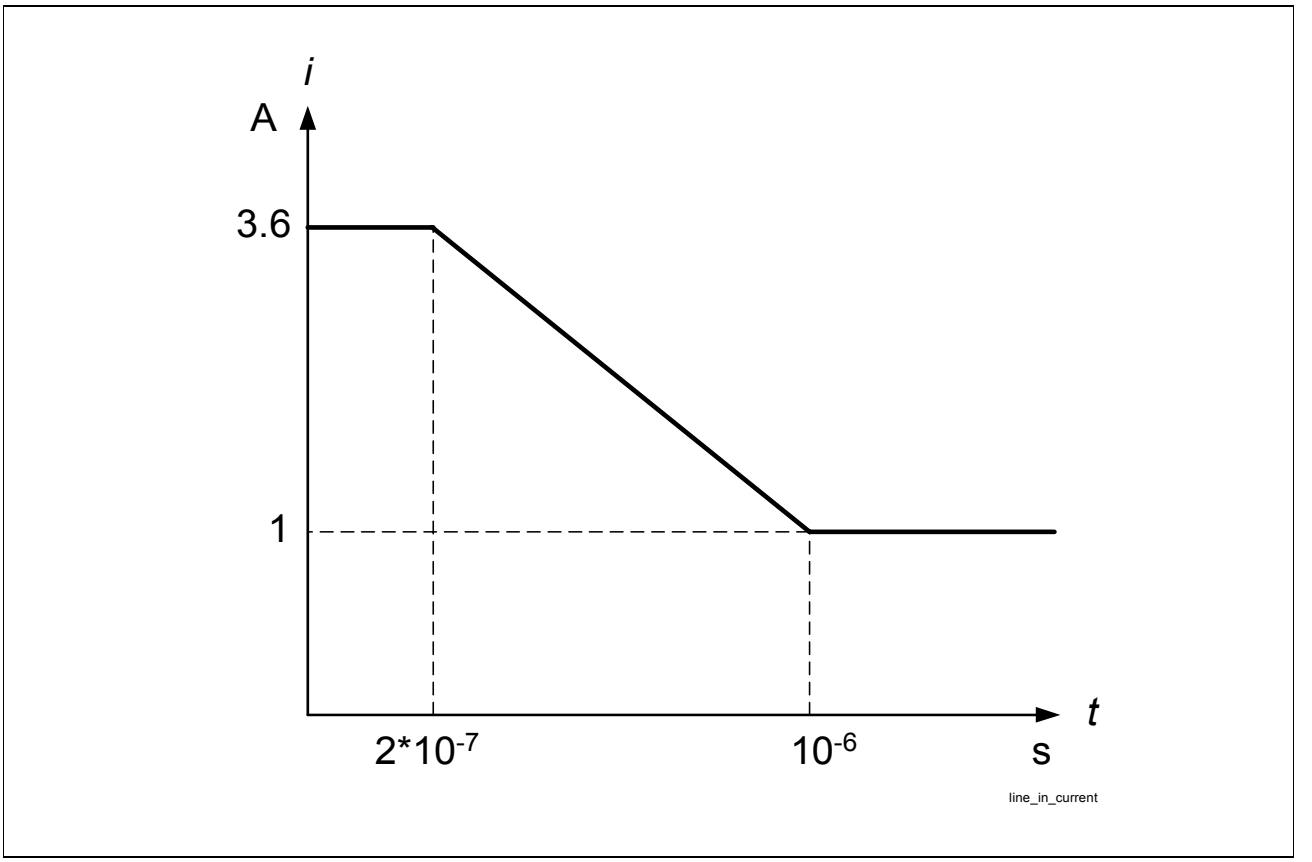


Figure 62 Maximum Line Input Current

7.5 DC Characteristics

Table 27 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	-0.4	0.8	V	
Input high voltage	V_{IH}	2	3.6	V	
Output low voltage	V_{OL}		0.4	V	I_{OL} [1)] = 5 mA $I_{OL, DOUT}$ = 8 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} [1)] = 5 mA $I_{OH, DOUT}$ = -8 mA

Table 27 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Avg. power supply current V_{DD} supply: 90-260 kbaud 260-515 kbaud 515-773 kbaud 3.3V (V_{DDP}/V_{DDA})supply:	I_{CC} (AV)		 T.B.D. T.B.D. T.B.D. T.B.D.	mA	V_{DD} = 1.8 V, $V_{DDP/DDA}$ = 3.3 V, T_A = 25°C Typical Values T.B.D. T.B.D. T.B.D. T.B.D
Input leakage current	I_{IL}		1.0[2)]	µA	Test condition 3.6 V
Output leakage current	I_{OL}		1.0[2)]	µA	Test condition 3.6 V
Pull Up Current	I_{PUR}	11	34	µA	Test condition 0 V

1) All pins except DOUT

2) Pull up resistors (100 kΩ) are not taken into account.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread.

7.6 Capacitances

T_A = 25 °C, 3.3 V ± 5% and 1.8 V ± 5% , f_C = 1 MHz, unmeasured pins grounded.

Table 28 Capacitances

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input Capacitance I/O Capacitance	C_{IN} $C_{I/O}$		5	pF pF	All pins except XTAL1
Output Capacitance against V_{SS}	C_{OUT}		5	pF	All pins except XTAL2
Input Capacitance	C_{IN}		7	pF	XTAL1
Output Capacitance against V_{SS}	C_{OUT}		7	pF	XTAL2

7.7 Specification of the Crystal

A crystal (parallel resonance) has to be connected to XTAL1 and XTAL2 which shall meet the following specification:

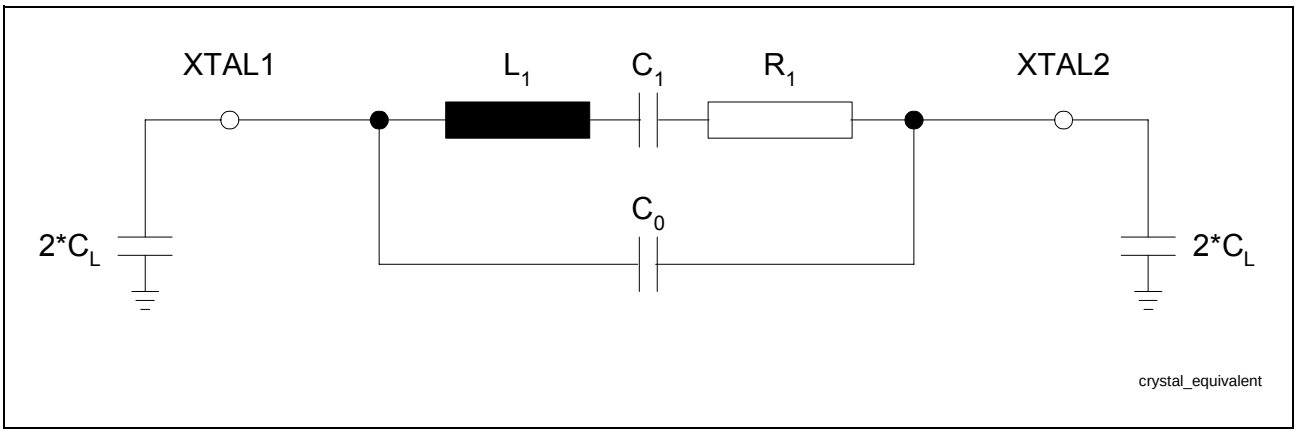


Figure 63 Equivalent Circuit for Crystal Specification[1)]

Table 29 Specification of the Crystal

Parameter	Abr.	Min	Typ	Max	Units
Nominal Frequency			20.48		MHz
Temperature Range		-40		+85	°C
Total Frequency Stability[1)]		-60		+60[2)]	ppm
Load Capacitance	C_L		18 pF		pF
Shunt Capacitance	C_0		7		pF
ESR	R_1		30	40	Ω
Drive Level		1			mW

1) This stability refers to the sum of all tolerances (general, temperature, aging)

2) ± 32 ppm are required for Internal Timed mode (see **Chapter 3.3**), ± 60 ppm are required for Loop Timed and External Timed mode (see **Chapter 3.3**) in order to meet the standards (ITU-T G.991.2, ITU-T G.shdsl.bis and ETSI TS 101 524)

The crystal specifications shall meet the requirements given in **Table 29**.

1) $2*C_L$ includes board and pin capacitance

7.8 Specification of the Transformer

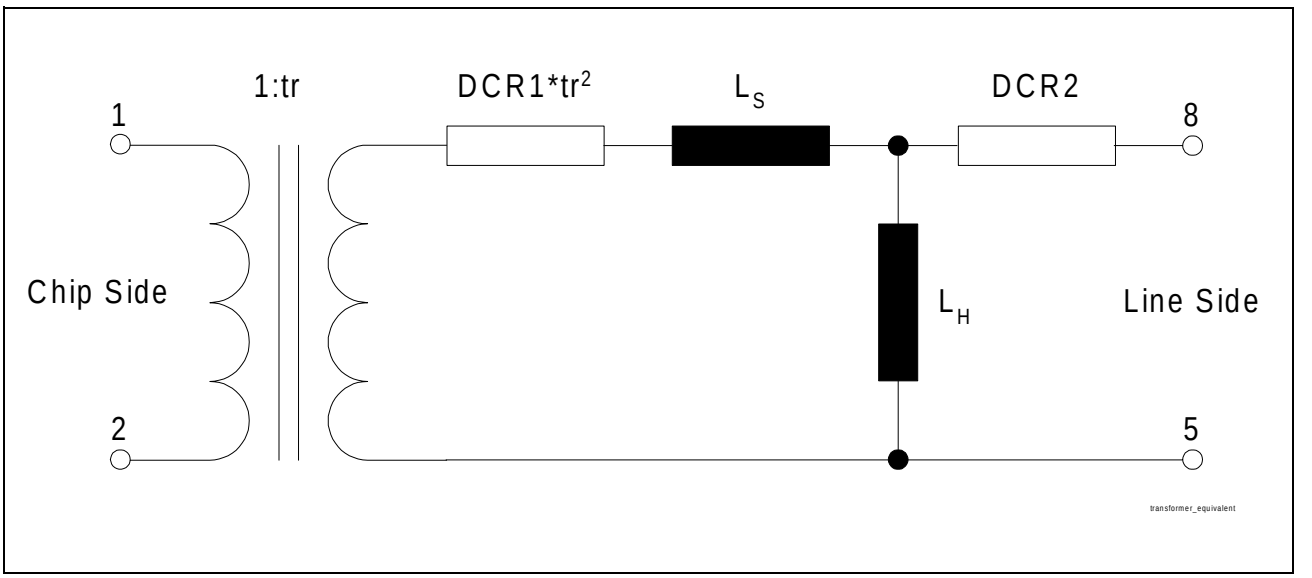


Figure 64 Equivalent Circuit for Transformer Specification

Table 30 Electrical Transformer Specification[1)]

Parameter	Abr.	Min	Typ	Max	Units
line side inductance:	L_H	2.7	3	3.3	mH
turns ratio cable to chip side:	tr	4.4325	4.5:1	4.5675:1	
winding resistance chip side (1-2):	DCR1			0.66	Ω
winding resistance line side:	DCR2			3.3	Ω
interwinding capacitance at 10 kHz				150	pF
primary to secondary breakdown voltage:		2000			Vrms
primary to secondary longitudinal balance:		50 at 5 kHz to 400 kHz			dB
leakage inductance (line side refered):	L_S			22[2)]	µH
THD at 35 mA DC line side osc. freq: 3 kHz (chip side) 1 V RMS (line side)		2nd harmonic -76 dB 3rd harmonic -84 dB			

1) Specified values guarentee optimum performance

2) Short pins 1 and 2 as well as 4 and 5. Measure leakage inductance from pin 3 to pin 6.

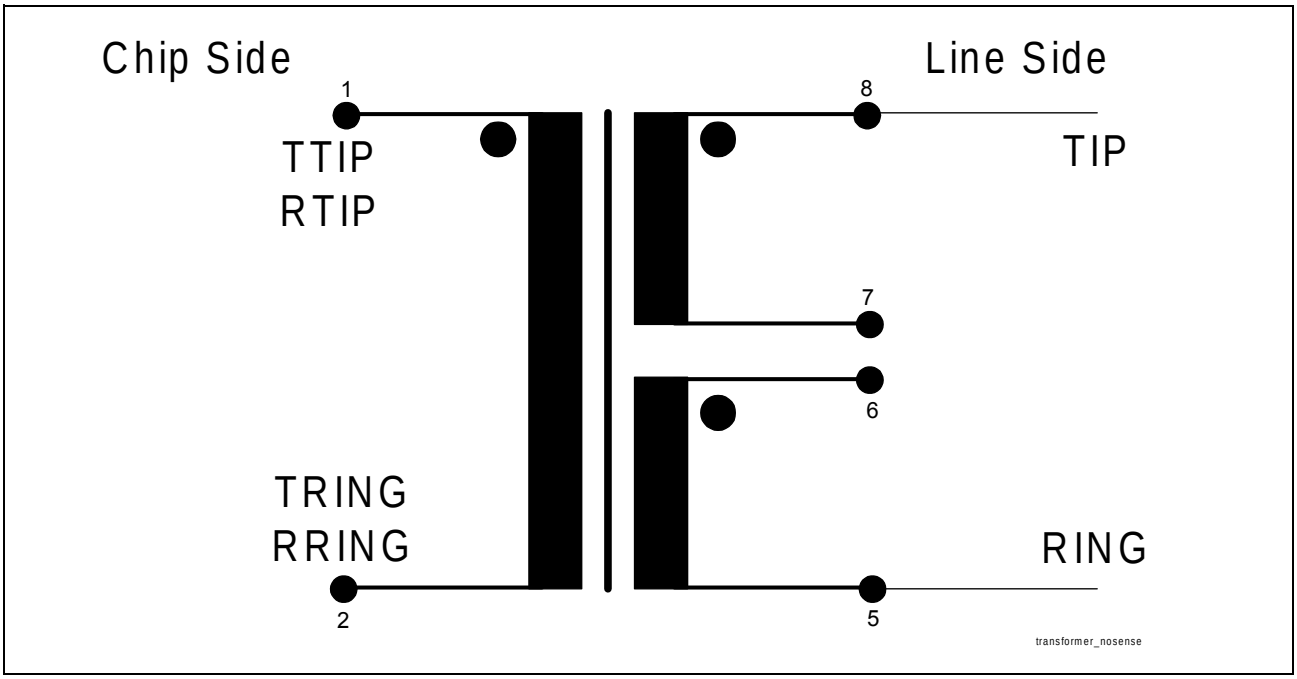


Figure 65 Transformer

7.8.1 THD Test

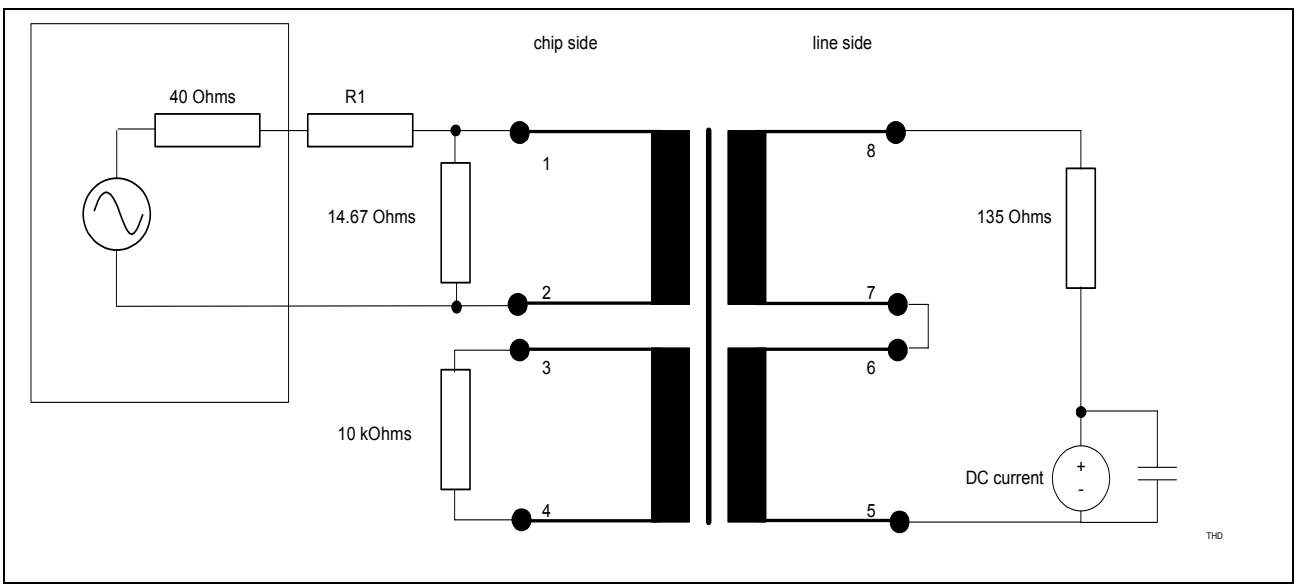


Figure 66 Test Circuit

Test Equipment

Audio Precision Measurement system or equivalent.

Lab Quality DC power supply capable of 5-10 V at 35 mA.

Set output impedance for 40 Ω, balanced output. Externally ground one end of output. Set input impedance for 100 kΩ, balanced. The test circuit is as described in Figure **Figure 66**.

Adjust oscillator amplitude so that U 5-8 is 1 V RMS. Oscillator frequency is 3 kHz. All resistors have 1% tolerance. Set DC current supply such that a current of 35 ±0.5 mA flows in winding 3-4-5-6.

Requirements

At U3-6:

1. 2nd harmonic (6 kHz) shall be at least 80 dB (objective) or 76 dB (requirement) below the fundamental.

2. 3rd harmonic (9 kHz) shall be at least 84 dB below the fundamental.

7.9 Reset Behavior

To reset the SDFE-4 properly, a reset pulse with a minimum pulse width as defined in **Table 31** has to be applied. Spikes on the reset line of up to 10 ns are ignored.

The 20.48 MHz clock has to be provided for pin XTAL1 of the SDFE-4 during reset.

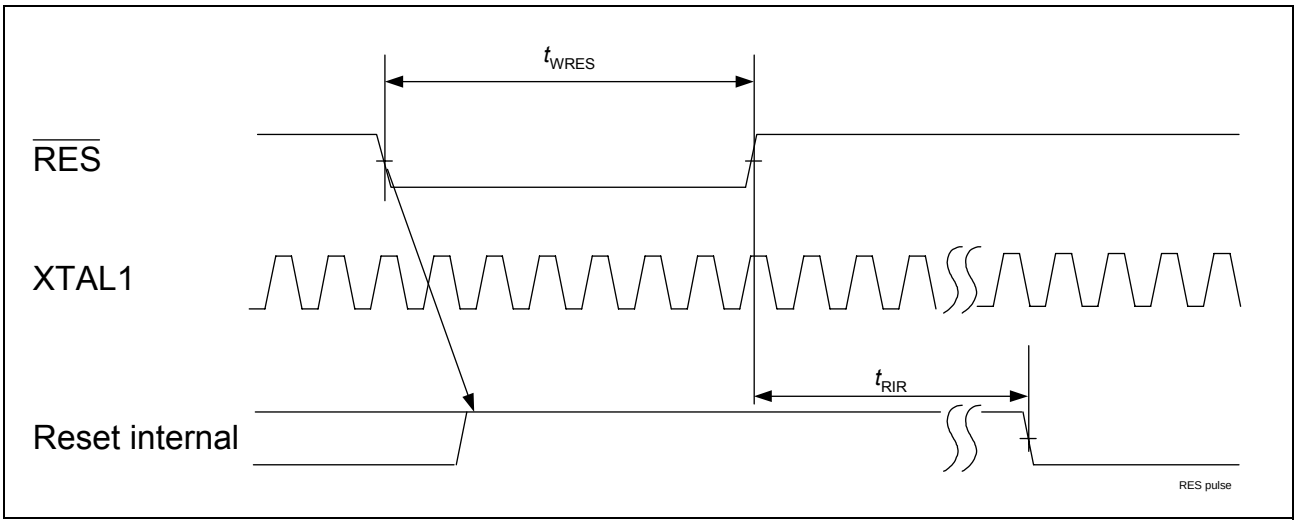


Figure 67 Reset Behavior

Table 31 Reset Behavior

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Pulse Width	t_{WRES}	150	-	-	ns
Internal Reset Release	t_{RIR}	-	-	200	µs

7.10 AC Characteristics

T_A = - 40 to 85 °C; V_{DDA} / V_{DDP}= 3.3 V ± 5% V_{DD} = 1.8 V ± 5%

Inputs are driven to V_{IH} = 2.4 V for a logical "1" and to V_{IL} = 0.4 V for a logical "0". Timing measurements are made at V_{TH} = 2.0 V for a logical "1" and V_{TL} = 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 68**.

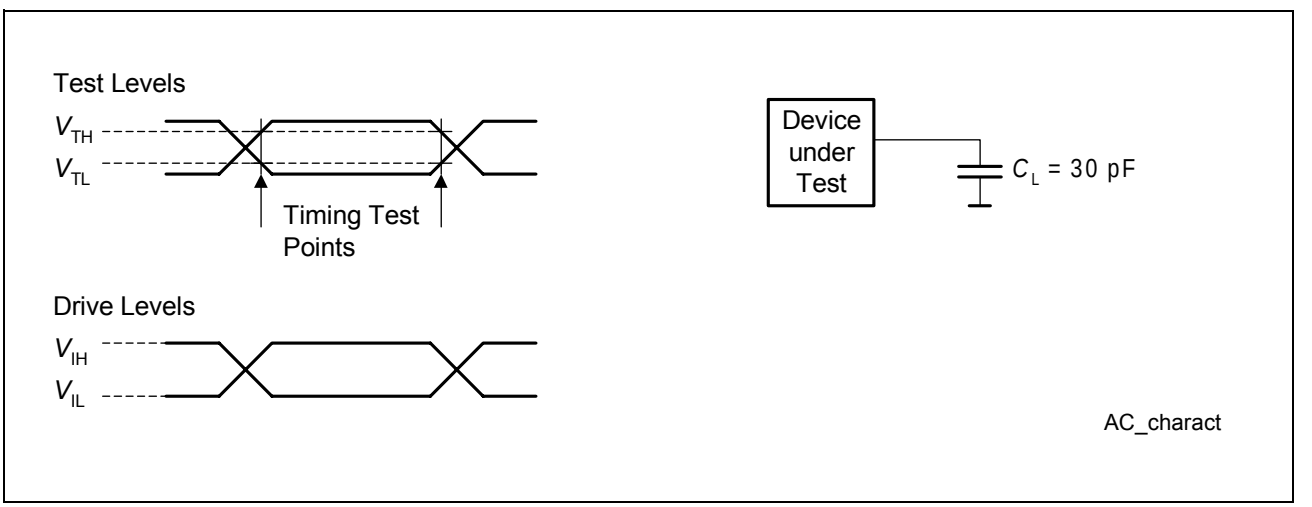
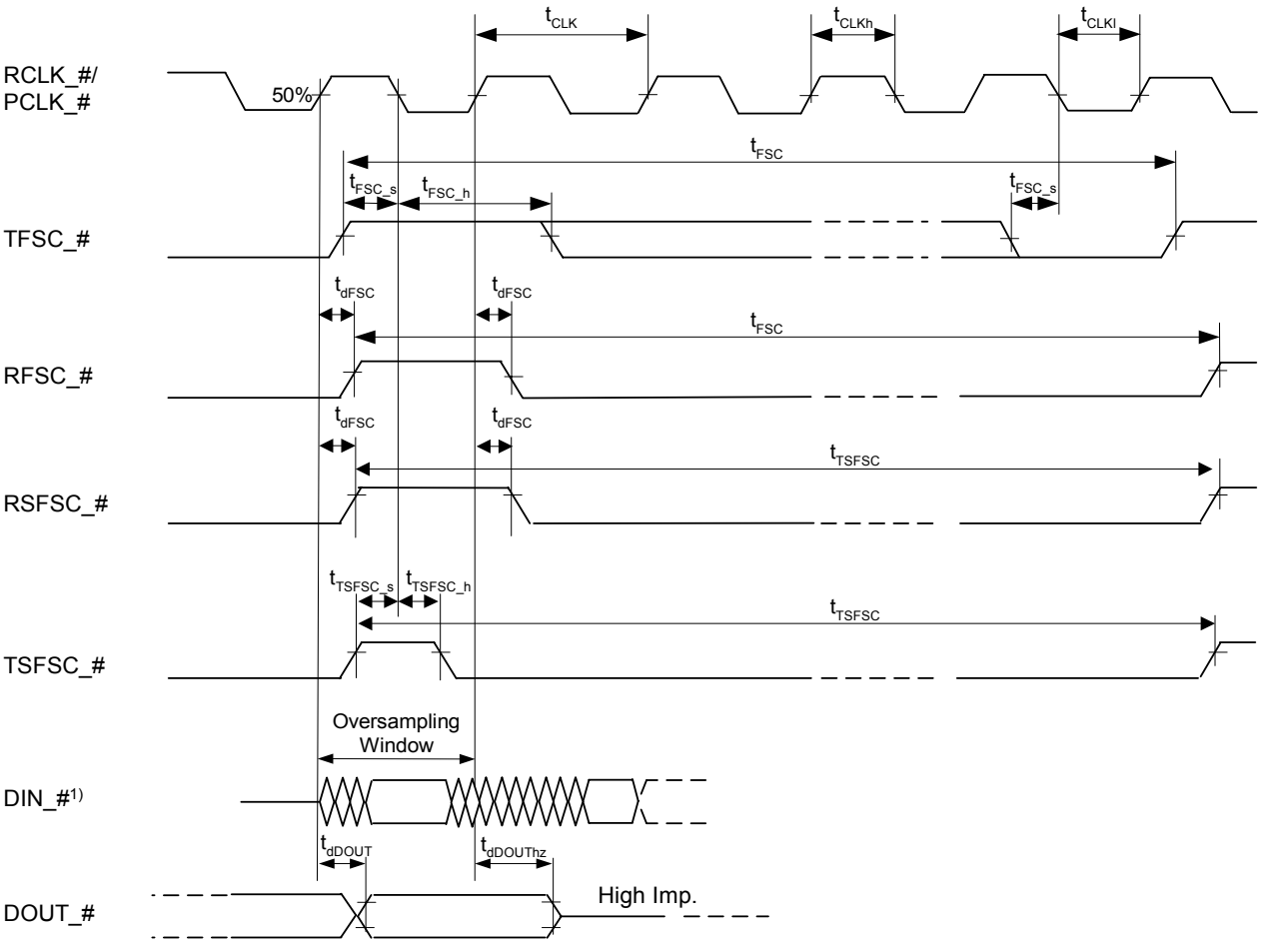


Figure 68 Input/Output Waveform for AC Tests

7.10.1 Serial Data Interface (TDM Interface Timing)



1) DIN_# is oversampled with the internal system clock.
The data is evaluated according to majority decision, i.e. the data which is valid for at least 20 ns plus 50% of the oversampling window is sampled.
This means for example for a clock frequency of 16.384 kHz the data delay of the counter part must not exceed 10 ns.

PCM_TIM

Figure 69 TDM Interface Timing

Table 32 TDM Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of RCLK_# / PCLK_#[1]	t_{CLK}	61[2]		5200[3]	ns
RCLK_# / PCLK_# high time[1]	t_{CLKh}	24	$t_{CLK/2}$		ns
RCLK_# / PCLK_# low time[1]	t_{CLKl}	24	$t_{CLK/2}$		ns
Period of RFSC_#(x) / TFSC_#(x)	t_{FSC}		125		µs
Period of RSFSC_# / TSFSC_#	t_{SFSC}		6		ms
TFSC_# setup time	t_{FSC_s}	16			ns
TFSC_# hold time	t_{FSC_h}	16			ns
TSFSC_# setup time	t_{SFSC_s}	16			ns
TSFSC_# hold time	t_{SFSC_h}	16			ns
RFSC_# /RSFSC_# delay	t_{dFSC}			10	ns
DOUT_# delay time	t_{dDOUT}			10	ns
DOUT_# delay time to high Z	$t_{dDOUThz}$			20	ns

1) RCLK_# / PCLK_# is programmable. Timing is the same for either edge or either polarity used.

2) In case of selecting 16.384 MHz as TDM data clock

3) In case of selecting 192 kHz as TDM data clock

7.10.2 Serial Control Interface Timing

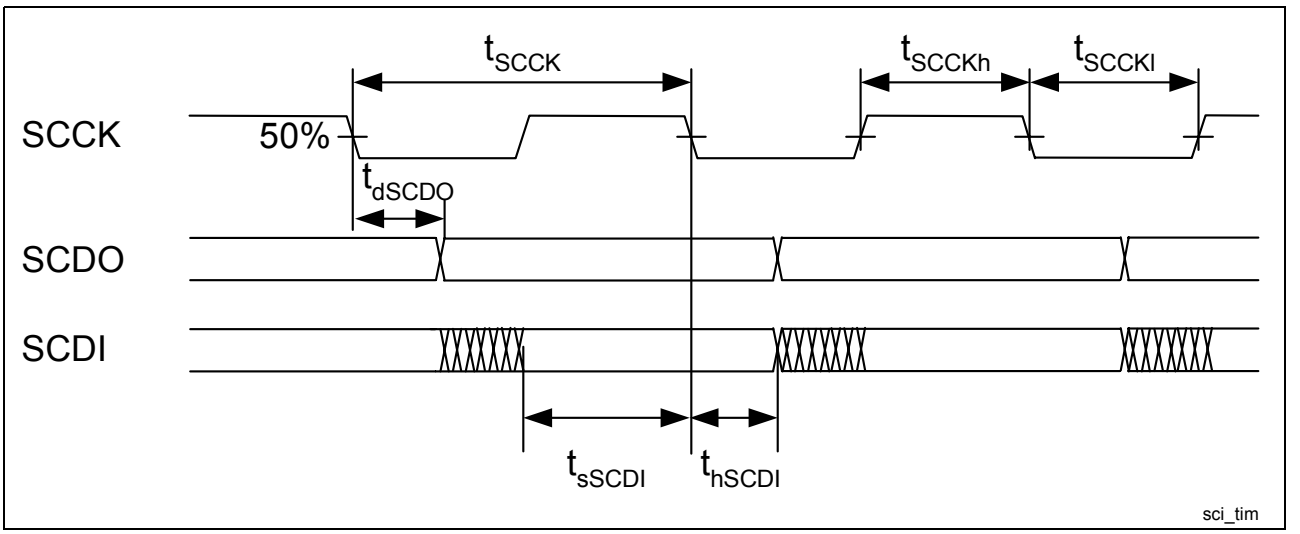


Figure 70 SCI Timing

Table 33 SCI Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of SCCK[1)]	t_{SCCK}	67		536	ns
SCCK high time[1)]	t_{SCCKh}	33	$t_{SCCK}/2$		ns
SCCK low time[1)]	t_{SCCKl}	33	$t_{SCCK}/2$		ns
SCDI setup time to SCCK	t_{sSCDI}	t_{SCCKh}			ns
SCDI hold time to SCCK	t_{hSCDI}	0			ns
SCDO delay time	t_{dSCDO}	5		13	ns

1) SCCK polarity is programmable. Timing is the same for either edge used
Clock frequencies in the range from 3.75 to 15 MHz can be applied

7.10.3 JTAG Interface

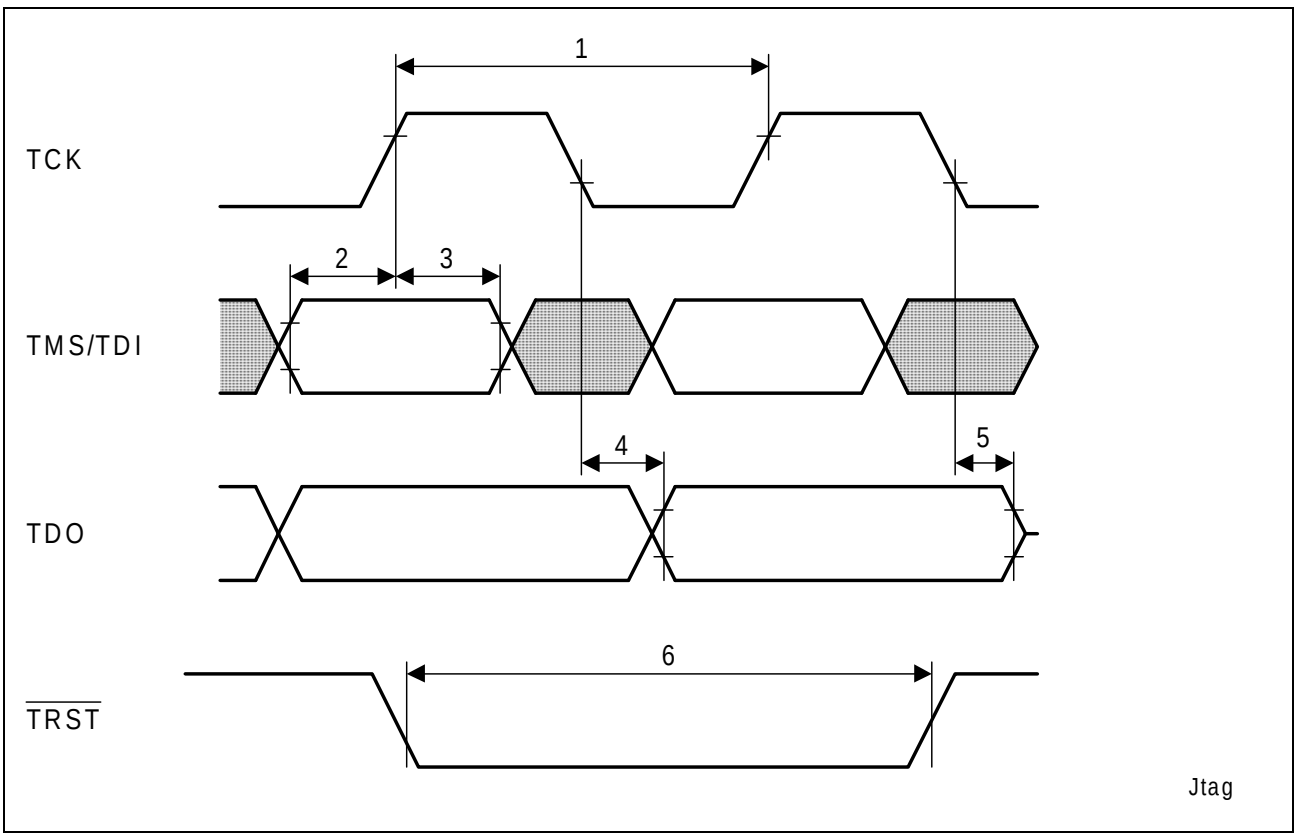


Figure 71 Boundary Scan Interface Timing

Table 34 Timing for Boundary Scan

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	T_{TCK}: Period TCK	160	–	–	ns
1A	F_{TCK}: Frequency TCK	–	–	6.25	MHz
2	Setup time TMS, TDI before TCK rising	10	–	–	ns
3	Hold time TMS, TDI after TCK rising	10	–	–	ns
4	Delay TCK falling to TDO valid	0	–	30	ns
5	Delay TCK falling to TDO high impedance	0	–	30	ns
6	Pulse width $\overline{TRST}$ low	$2 \times T_{TCK}$	–	–	ns

8 Package Outlines

P-LBGA-324-2
(Plastic Low Profile Ball Grid Array)

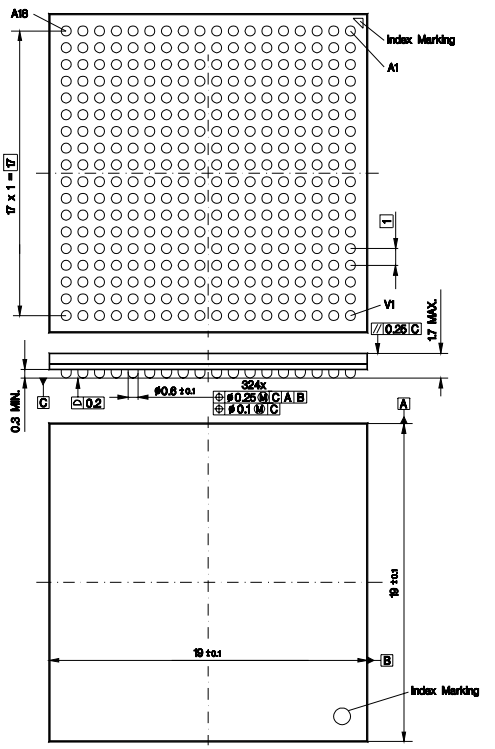


Figure 72 Package Outline (P-LBGA-324-2)

You can find all of the current packages, types of packing, and others on the Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

9 Terminology

API	Application Programming Interface
ANSI	American National Standards Institute
P-LBGA	Plastic Low Profile Ball Grid Array
B-ISDN	Broadband - Integrated Services Digital Network
BSC	Base Station Controller
BTS	Base Transceiver Station
CO	Central Office
CPE	Customer Premises Equipment
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DLC	Digital Loop Carrier
DSL	Digital Subscriber Line
DSLAM	Digital Subscriber Line Access Multiplexer
ETSI	European Telecommunications Standards Institute
FCS	Frame Check Sequence
FIFO	First In, First Out
FW	Firmware
HDLC	High-level Data Link Control
HW	Hardware
IEEE	Institute of Electrical & Electronic Engineers
I/O	Input/Output
ITU	International Telecommunications Union
ITU-T	International Telecommunications Union - Telecommunications Standardization Sector
JTAG	Joint Test Action Group
LAN	Local Area Network
LBGA	Low Profile BGA
LSB	Least Significant Bit
LTU	Line Termination Unit
MIB	Management Information Base
µP	Microprocessor

MPI	Micro Processor Interface
MSB	Most Significant Bit
MUX	Multiplexer
NTU	Network Termination Unit
OAM	Operation, Administration, and Maintenance
PAM	Pulse Amplitude Modulation
PBX	Private Branch Exchange
PCM	Pulse Code Modulation
PDH	Plesiochronous Digital Hierarchy
PHY	Physical Layer Device
POTS	Plain Old Telephone Service
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RAM	Random Access Memory
RITL	Radio In The Loop
RNC	Radio Network Controller
Rx	Receive
SCI	Serial Control Interface
SDI	Serial Data Interface
SRU	SymDSL Regenerator Unit
SRU-C	SRU Central Office Functionality (Customer Side)
SRU-R	SRU Remote Functionality (Network Side)
STM	Synchronous Transport Module
STU	SymDSL Transceiver Unit
STU-C	STU at the Central Office
STU-R	STU at the Remote End
SW	Software
symDSL	Symmetrical DSL (according to ITU-T G.991.2 (SHDSL), ETSI TS 101 524 (SDSL), ITU-T G.shdsl.bis (SHDSL bis), ITU-T G.991.1 (HDSL), ETSI TS 101 135 (HDSL), T1E1.4/2001-006R3 (HDSL2/HDSL4) and 2B1Q-SDSL)
TAP	Test Access Port
TDM	Time Division Mutiplex

Tx	Transmit
WLL	Wireless Local Loop

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Dr. Ulrich Schumacher

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