Bt8960

Hardware User's Guide

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Bt8960EVM Hardware User's Guide

Introduction

Welcome to the Bt8960 Evaluation System from Brooktree Corporation. You can use the Bt8960 Evaluation System to evaluate the performance of the Bt8960 device, to develop software for your Digital Subscriber Line (DSL) system, and for many other applications. Brooktree has created this development platform to help its customers get their communication system products to market as quickly as possible.

Important Information

Bt8960EVM Contents

The Bt8960 Evaluation System Hardware User's Guide is one part of the Bt8960EVM package. If you have ordered the Bt8960EVM, please review the Bt8960EVM Contents List to ensure that you have received all of the items on the list.

Software

This user's guide covers the operation and design of the Bt8960EVM. It does not describe the software contained in the PROMs that are shipped with this system. For a description of this software, please sign and return the Software License agreement shipped as part of the Bt8960EVM package. In return, Brooktree will send the source code (in C) of the software that resides in the PROM.

User Interface Program

A user interface program (UIP) is also provided by Brooktree to perform for more advanced monitoring and testing of the Bt8960EVM. This program runs on a standard IBM compatible personal computer (PC) and interfaces from the PC to the Bt8960EVM through two RS-232 serial communication ports. Please see the User Interface Program (UIP) User's Guide (UGHDSL_1A) for additional information.

Data Rate

The Bt8960EVM has been designed to operate at a data rate of 288 Kbits per second. It can be modified to run at other data rates supported by the Bt8960 device. Please see the Bt8960 datasheet or the Interconnection Information application note for more information on how to modify the line card for different data rates. Each line card in the system also contains a line card ID which is set by five 0 ohm resistors, R39 to R43 (see the 8960EVM line card schematic in appendix A). These resistors may need to be modified so the EVM software is configured for the correct data rate. The line card ID is defined according to Table 1.

Table 1 Line Card ID Definition

R39 to R43 (binary)	Data Rate (kbps)	
	Center	Range of Operation
00000 (default)	288	220 to 352
00001	416	352 and up
00010	160	Up to 220
All Others	Reserved	Reserved

Ordering Information

Order Code Bt8960EVM

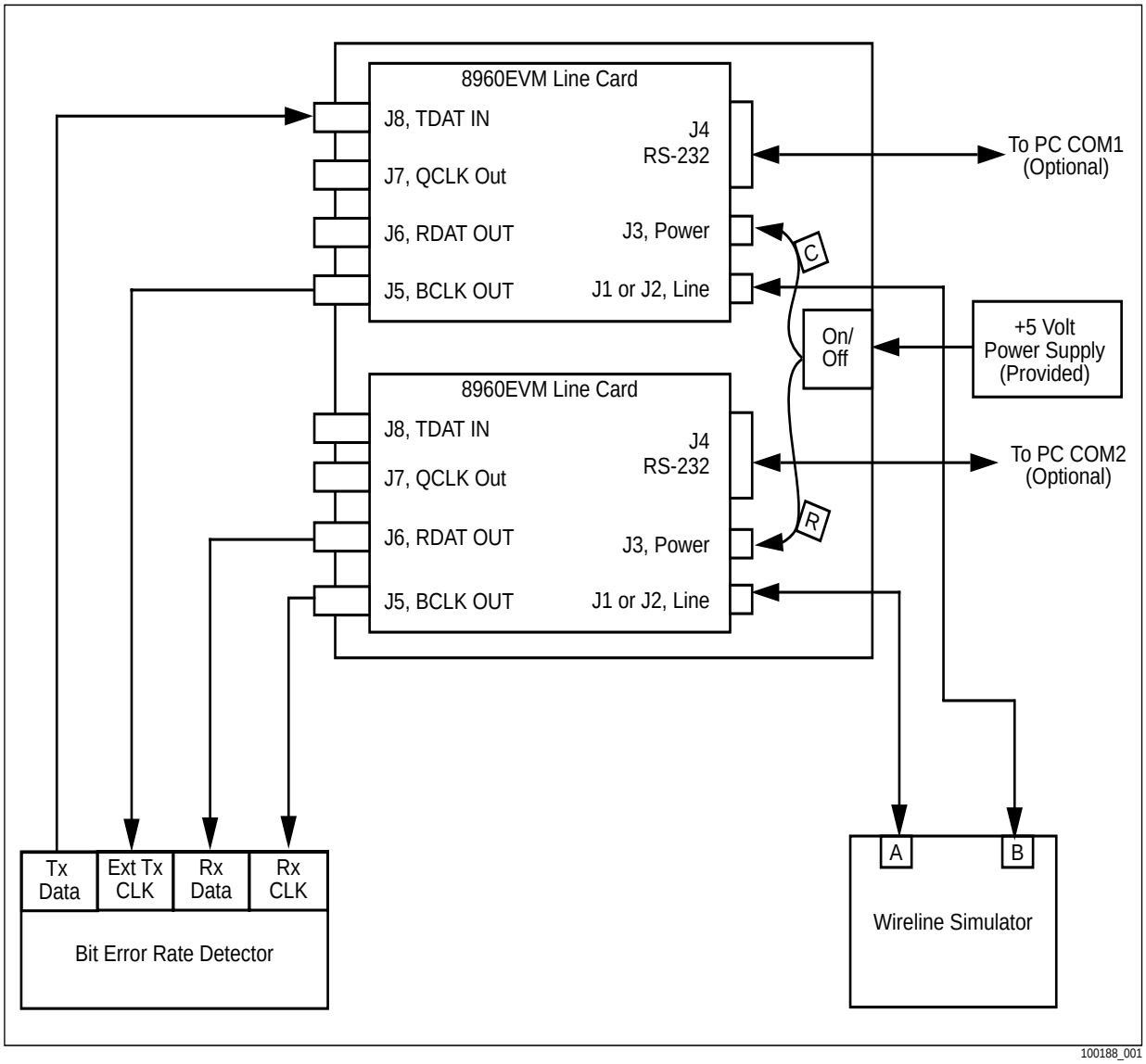
Description The Bt8960 evaluation system can be ordered using the order code listed above. This order includes both the local (HTU-C/LTU) and remote (HTU-R/NTU) units needed to perform full-duplex data transmission over a twisted pair of wire. A power supply is also included for your convenience. For a full list of the items shipped with the Bt8960EVM order, please see the Bt8960EVM Contents List.

Setup Instructions

Basic Setup

In Figure 1, "C" designates the line interface card as being the central unit, also referred to as the local unit, HTU-C, or LTU. The "R" designates the remote unit line interface card. It is also referred to as the HTU-R or NTU.

Figure 1 Loop Performance Test Remote Unit Setup (C to R)



Follow the steps below to set up the EVM for loop performance evaluation.

1. Connect all cables as shown in the Figure 1, Loop Performance Test Setup (C to R).
    a. Bit Error Rate Detector Connection—The FIREBERD 6000 (w/ lab interface) is recommended (see "Recommended Equipment" section herein). If it is used, the lab interface should be set up as follows (selected on rear panel):
        1 Mode: Unipolar Unbalanced
        2 Input Impedance: 8 Kohms
        3 Clock Phasing: TX and RX falling edges

The FIREBERD should also be configured as follows using the front panel selections:

        4 Data: 2^23-1
        5 GEN CLK: INTF
        6 TIMING MODE: SYNC
        7 ANALYSIS MODE: CONTINUOUS
        8 MENU: INTF SETUP: LAB
        9 AUXILIARY: default settings ("AUX FUNC IN USE" will illuminate if default is not used)

    b. Wireline Simulator Connection—Connectors J1 (RJ-45) or J2 (screw tightened terminal strips) on the line interface cards should be connected to points "A" and "B" on the wireline simulator. If either of the J2 connectors are used, be sure the polarity is the same at each line interface card. If the polarity is reversed (i.e., tip/ring reversal), the 8960EVM will start up, but the Bit Error Rate Detector may not synchronize. The wireline simulator can also be bypassed by connecting J1 or J2 on the "C" line interface card directly to J1 or J2 on the "R" line interface card
    c. Power Supply Connection—Connect the power supply as shown. Make sure the power switch is in the "OFF" position.
    d. PC Connection (optional)—If a PC is connected to the EVM through the RS-232 COM1 and COM2 serial communication ports, the User Interface Program (UIP) can be used to monitor the status of the EVM during startup and normal operation. The UIP can also be used to exercise a variety of other test modes and functions of the EVM. Instructions for running the UIP are listed below in the UIP Quick Start section. Please see the UIP User's Guide for more details.
2. Turn the power switch to the "ON" position.
3. After power is applied, both line cards in the EVM will perform self-test. During self-test, the START-UP and ERROR LEDs will illuminate. If the self-test fails, they will remain illuminated and the EVM will go into the idle state. If both line cards pass self-test, the EVM will automatically try to startup on the loop connected between the line terminals on the EVM

line cards (J1 or J2). Startup will take approximately 30 seconds to complete (for 228 kbps operation only). During startup, the green START-UP LED will blink to indicate that start-up is in process.

4. If startup fails, the red ERROR LED will illuminate momentarily and startup will begin over again. If startup is successful, the green START-UP LED will stop blinking and become steadily illuminated, and the EVM will begin transmitting and receiving external data through the BNC connectors on the line cards (J5, J6, J7 and J8). This state is referred to as the Normal Operation state.
5. If during the Normal Operation state, one of the line cards detects an error condition (i.e., Loss of Signal (LOS) or low noise margin), the line card will deactivate and the red ERROR LED will blink for approximately 2 seconds. The line card will then attempt to re-startup on the given loop.

UIP Quick Start

1. Verify the RS-232 connectors on the EVM line cards (J4) are connected to COM1 for the central unit and COM2 for the remote unit on the PC. Also verify the UIP is installed on the PC according to the instructions on the UIP installation disk and in the UIP User's Guide.
2. In the UIP directory, type "8960EVM" and press enter.
3. The UIP will default to the "EVM Configuration" form. "BT8960" should be displayed in column #1 of the "Bitpump Type" field for both the HTU-C and HTU-R. Press escape to exit.
4. In the main menu, select "Startup". In the "Custom Startup Options" form, select "Global Activate". Startup should begin (verify the green START-UP LEDs on the line cards are blinking). The UIP will indicate the status of the EVM as it attempts to startup.
5. If startup is successful, the UIP will display the "Startup Successful" message. Now the Bit Error Rate Detector should begin passing data (On the FIREBERD the "sync" indicator will illuminate).

Recommended Equipment

Line Simulator

- Manufacturer: Consultronics
- Model: DLS 200
- Phone: (800) 267-7235

NOTE: Several versions of DLS 200 models are available to simulate ANSI and ETSI ISDN and CSA loops. The model should be chosen according to the application and data rate. Brooktree used the DLS 200 ISDN ANSI and ETSI models to evaluate the 288 kbps loop performance of the Bt8960.

Communications Analyzer Bit Error Rate Detector

- Manufacturer: Telecommunications Techniques Corporation
- Model: FIREBERD 6000 with Lab Interface Adapter
- Phone: (800) 638-2049

Personal Computer (optional)

- See the UIP User's Guide

Functional Description

The 8960 EVM consists of two 8960 line cards, a power supply assembly, and a mounting plate.

8960 Line Cards	The 8960 line cards are described in detail in the Interface Descriptions section.
Power Supply Assembly	The power supply assembly consists of a universal +5 volt power supply and the associated cabling. In addition to providing +5 volt power and ground, the power supply assembly also provides a signal to each 8960 line card which determines if the line card will be configured as a local unit (HTU-C/LTU), or a remote unit (HTU-R/NTU). The power connectors to each line card are labeled as C, as in HTU-C, and R, as in HTU-R, to indicate how the line card it is connected to will be configured. See the "Power Supply/Line Card Configuration Interface (J3)" section for more details on this interface.
Mounting Plate	The mounting plate simply provides a mounting surface for the line cards and power supply assembly.

Interface Descriptions

Line Interface (J1, J2)

Connectors

Two connectors are included on the 8960 line card to provide connections to the line. J1 is an RJ-45 style connector common to telecommunication equipment. Only pins 4 (tip) and 5 (ring) are utilized on the connector. Pins 1, 2, 3, 6, 7 and 8 of J1 are left unconnected. J2, an all-purpose terminal strip connector, can also be used to connect to the line tip and ring signals.

Prototyping Provisions

Test points and prototype space are included on the line card to facilitate the testing of remote line powering and lightning protection circuits. See Table 2 to determine which test points are provided for these purposes. In most cases, a 0 ohm resistor must be removed prior to adding the circuitry to be tested.

Power Supply/Line Card Configuration Interface (J3)

Power Supply (pins 1 and 2):

Power is provided to the line card through the J3 connector. Two test points are provided so that power can be measured and/or supplied by an alternative source if desired. *If power is supplied though these test points, be sure to remove the mating connector from J3 because the cable connected to J3 will create a short between power and ground when the power switch on the power box is in the OFF position.* Two large capacitors (C11, C12) and a transorb (CR4) provide a steady 5 volt power rail and protect circuits on the line card from dangerous transient power spikes. The POWER LED (CR1) indicates when power is applied to the line card.

Remote/Local Unit Configuration (pin 3)

In addition to supplying the line card with 5 volts and ground, the 3-pin connector also contains a control pin used by the 8032 microprocessor to indicate if the line card is to be configured as the local (HTU-C/LTU) or remote (HTU-R/NTU) unit. If pin three of J3 (J3-3) is connected to ground, the line card will be configured as the local unit. Conversely, if J3 is left open, the line card will be configured as the remote unit. Control of the local/remote configuration function can be removed from the J3 connector and given to jumper J12 by removing the 0 ohm resistor, R44, and installing jumper J12. Note that the 8032 microprocessor PORT1B7 signal (pin 9) contains an internal pull-up resistor that is connected to J3-3 so that no external pull-up resistor is required.

RS-232 Interface (J4)

Connector J4 provides an RS-232 connection to the 80C32 microprocessor. The TX, RX and GND are the only RS-232 signals utilized for this connection. TX and RX are labeled on the line card PCB silk-screen.

Digital Data Interface (J5, J6, J7, J8)

Four BNC connectors are provided to connect the raw digital data and clocks to be transmitted and received over the line to the Bt8960. These connectors are buffered through an HCT244 buffer to protect the Bt8960 from improper connections and to provide extra drive strength for coax cables. All outputs include a source resistance of 50 ohms to prevent ringing. The TDATA IN input (J8) is pulled up to 1 Kohm to prevent ringing while also providing a high enough input impedance so it can be driven by a typical CMOS driver. After these signals are buffered, they connect to the channel unit interface section of the Bt8960. See the Bt8960 datasheet for details on the channel unit interface timing and functionality. Test points are provided for all of the Bt8960 channel unit interface signals so that the signals can be connected to a customized framer if desired. Prototype space is also available on the line card for this purpose.

Test Points

A variety of test points are included on the Bt8960 to accommodate test measurements and to provide solder points for prototyping. Table 2 lists all of the test points on the Bt8960 line card along with their associated signal names. These test points have been numbered in an orderly fashion on the 8960 line card so that they are easy to locate.

Table 2 8960 Line Card Test Point

Test Point Name	Signal Name
TXP	Transmit (positive)
TXN	Transmit (negative)
TP1	SMON
TP2	RST*
TP3	HCLK
TP4	XOUT
TP5	TIP / R46
TP6	TIP (line side)
TP7	TIP (circuit side)
TP8	Split Transformer / TIP
TP9	BCLK (buffered)
TP10	Split Transformer / RING
TP11	RING / R45
TP12	RING

Table 2 8960 Line Card Test Point

Test Point Name	Signal Name
TP13	RING (circuit side)
TP14	GND
TP15	RDAT (buffered)
TP16	TCK (JTAG)
TP17	TMS (JTAG)
TP18	TDI (JTAG)
TP19	TDO (JTAG)
TP20	TBCLK
TP21	RBCLK
TP22	TQ0 (buffered)
TP23	+5V
TP24	QCLK (buffered)
TP25	TDAT (buffered)

80C32 Processor Circuitry

RESET

The RESET button provides an active-high reset signal to the 80C32 processor. The 80C32 processor contains an internal pull-down resistor so that an external pull-down resistor is not needed. The length of the reset pulse is controlled with capacitor C34.

Memory

A 64 Kbyte PROM (27C512) provides program memory to the 80C32. The 80C32 contains 256 bytes of internal RAM. No external RAM is provided. The upper address line of the 80C32 processor (ADDR15) is used as chip select for the Bt8960 device. The memory is mapped according to Table 3.

Table 3 Memory Mapping

Memory Type	Address Range	R/W	Size (bytes)	Description
Internal RAM	0x00–0xFF	R/W	256	80C32 Internal Memory
Program	0x0000–0xFFFF	R	64 K	ROM
Data	0x0000–0x00FF	R/W	256	Bt8960
Data	0x0100–0x7FFF	-	32 K–256	Phantom Bt8960
Data	0x8000–0xFFFF	-	32 K	Unused

Status LEDs

In addition to the power LED, two LEDs labeled ERROR and START-UP are included to provide status to the Bt8960EVM user. They are connected to Port 1 on the 80C32 and are controlled via the Bt8960EVM software.

Line Card ID

Five signals are provided to the 80C32 to indicate the ID of the line card to the EVM software. They are connect to Port 1 of the 80C32. See Table 1 for a description of the line card ID values.

Layout Considerations

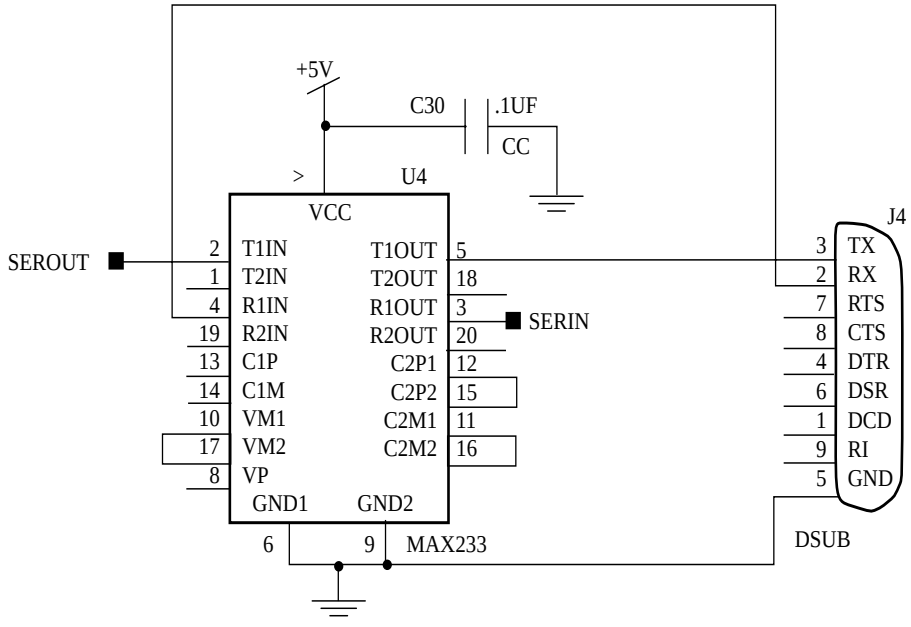
The Bt8960 line card analog and digital power and ground planes are isolated from each other. The analog and digital planes are connected at a single point under the Bt8960 device. Voltage bypass and compensation capacitors are located as close to their associated devices as possible. In addition, capacitors C5 and C6 are located as close to the Bt8960 device as possible to minimize noise at the Bt8960 analog inputs.

Appendix A

Schematics, Layout Drawings and BOMs

The schematic, layout drawing and BOM for the 8960 line card are presented on the following pages.

Figure 2. Detail "A" for Page 1 of the Bt8960 Schematic



NOTE(S):
Please note above changes for your design.

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