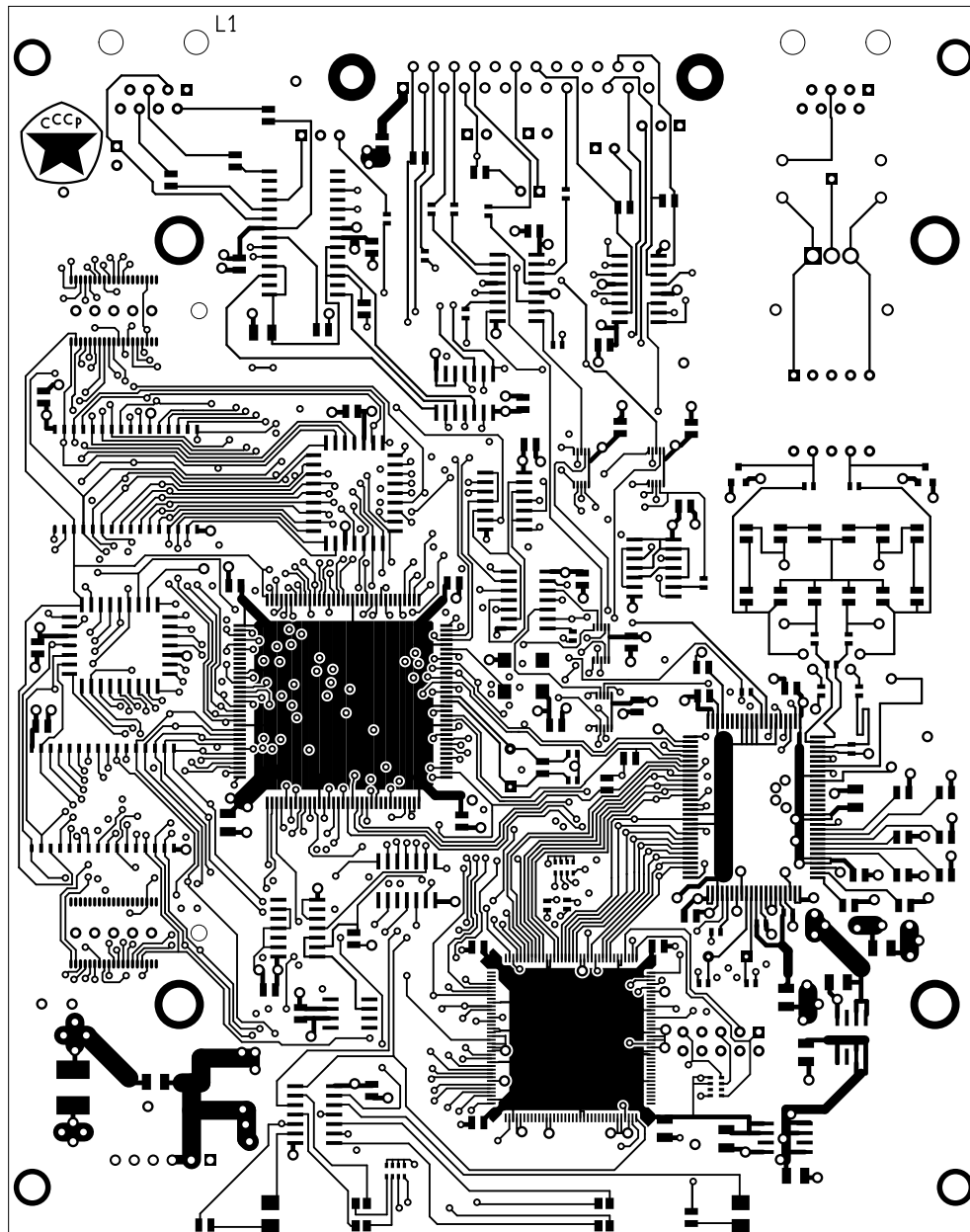
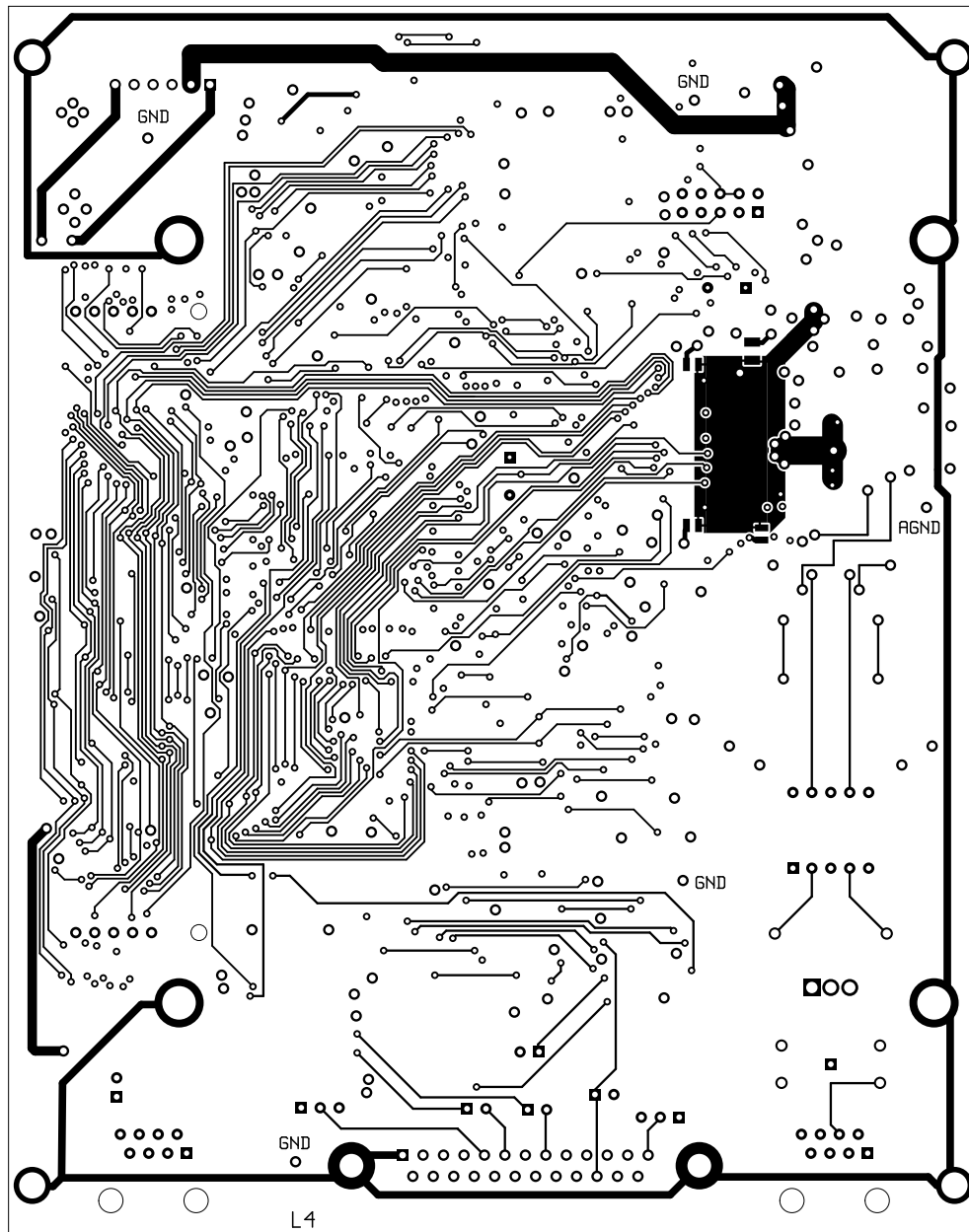
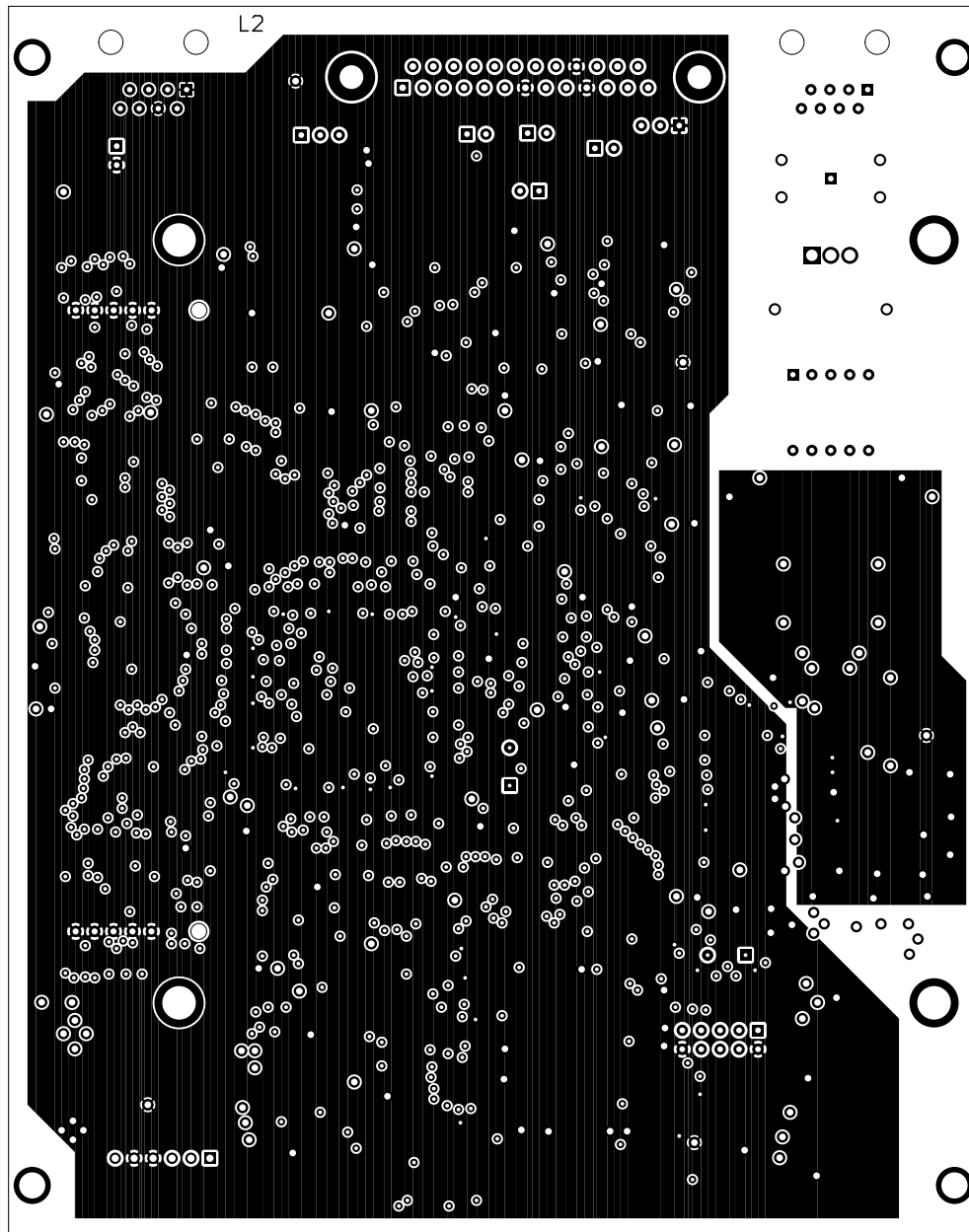
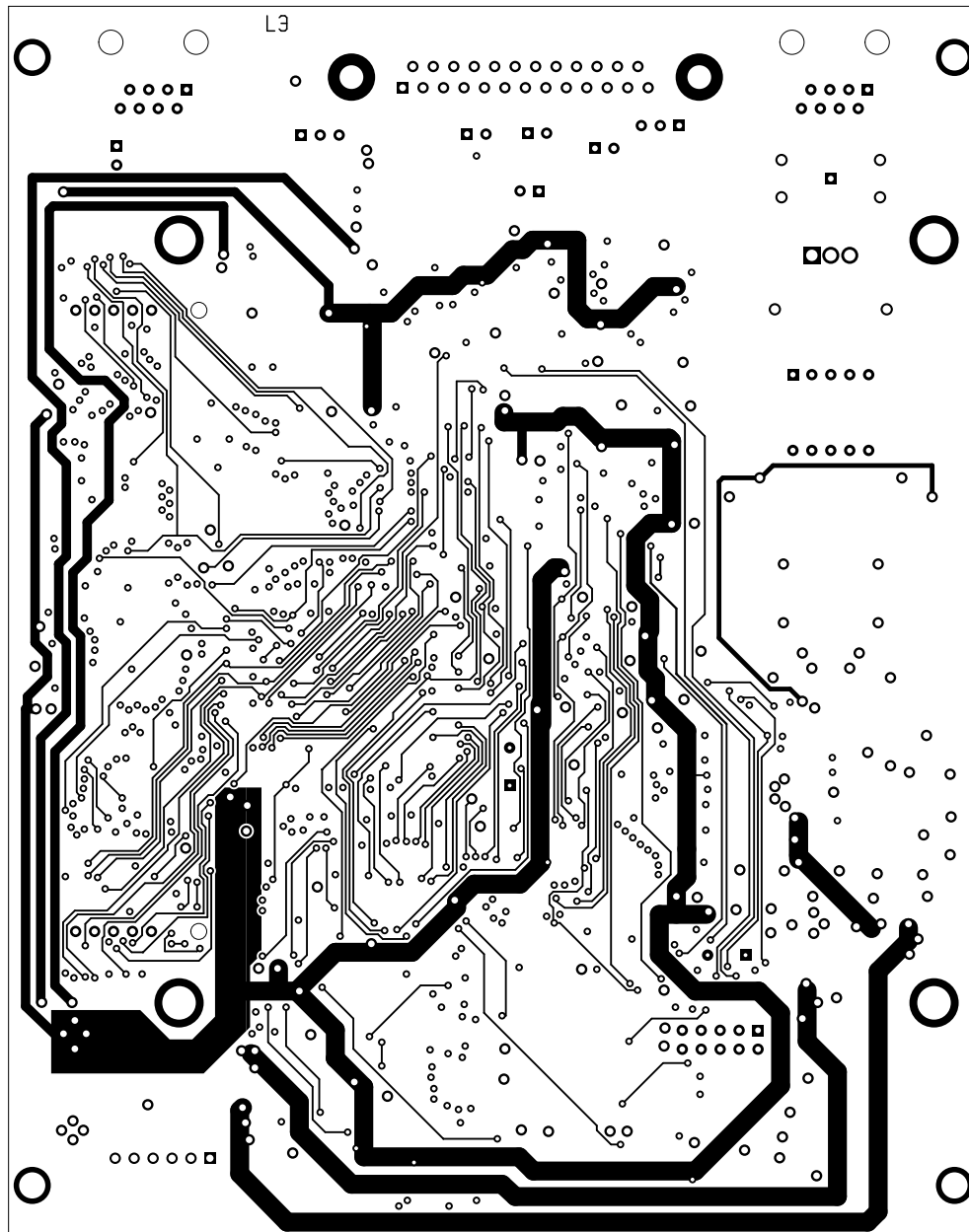


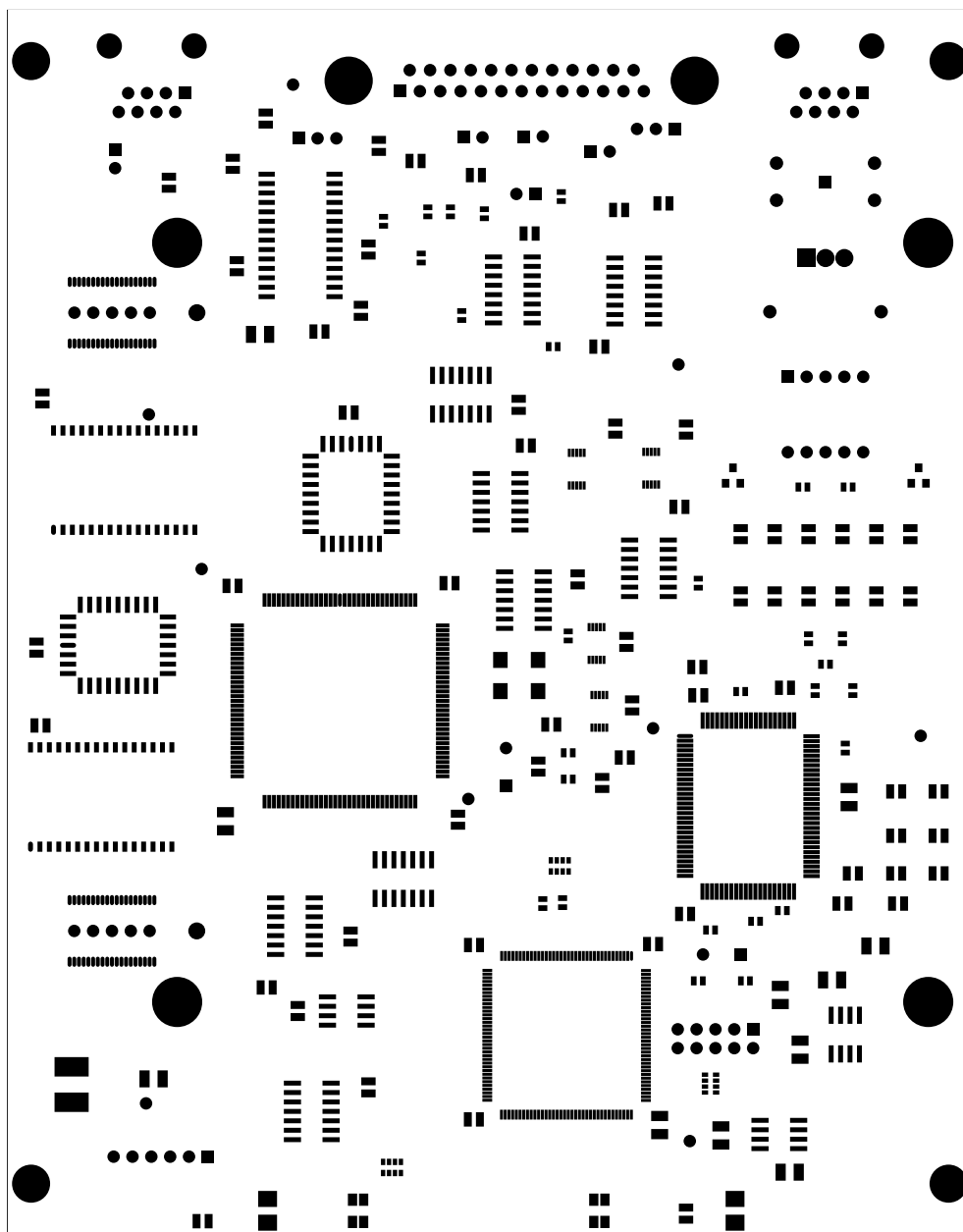
2. component
3. solder
4. GNDplane
5. middle1
6. componentmask
7. soldermask
8. plated-drill
9. unplated-drill
10. topsilk
11. bottomsilk
12. bottompaste
13. toppaste
14. topassembly
15. bottomassembly
16. fab

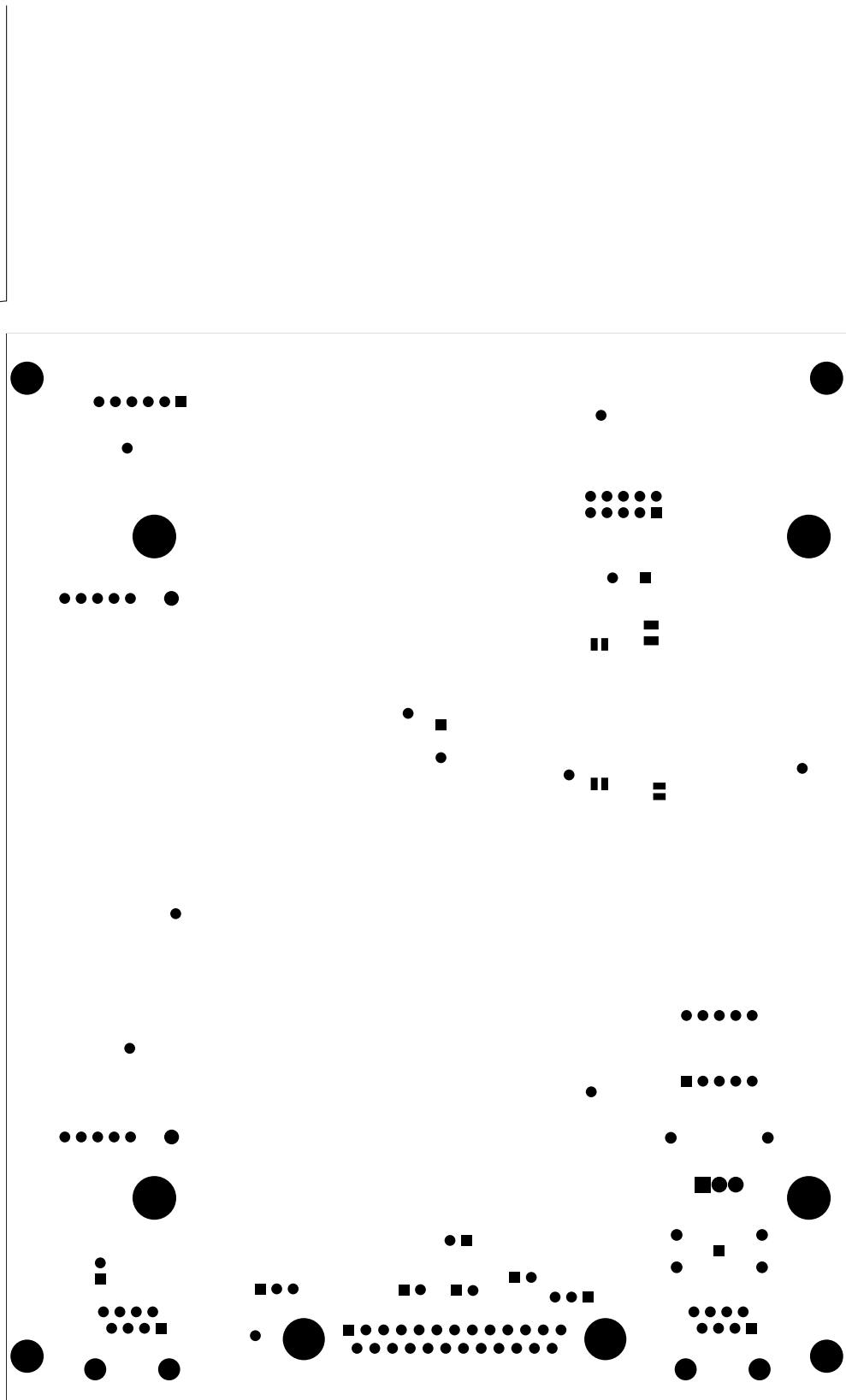




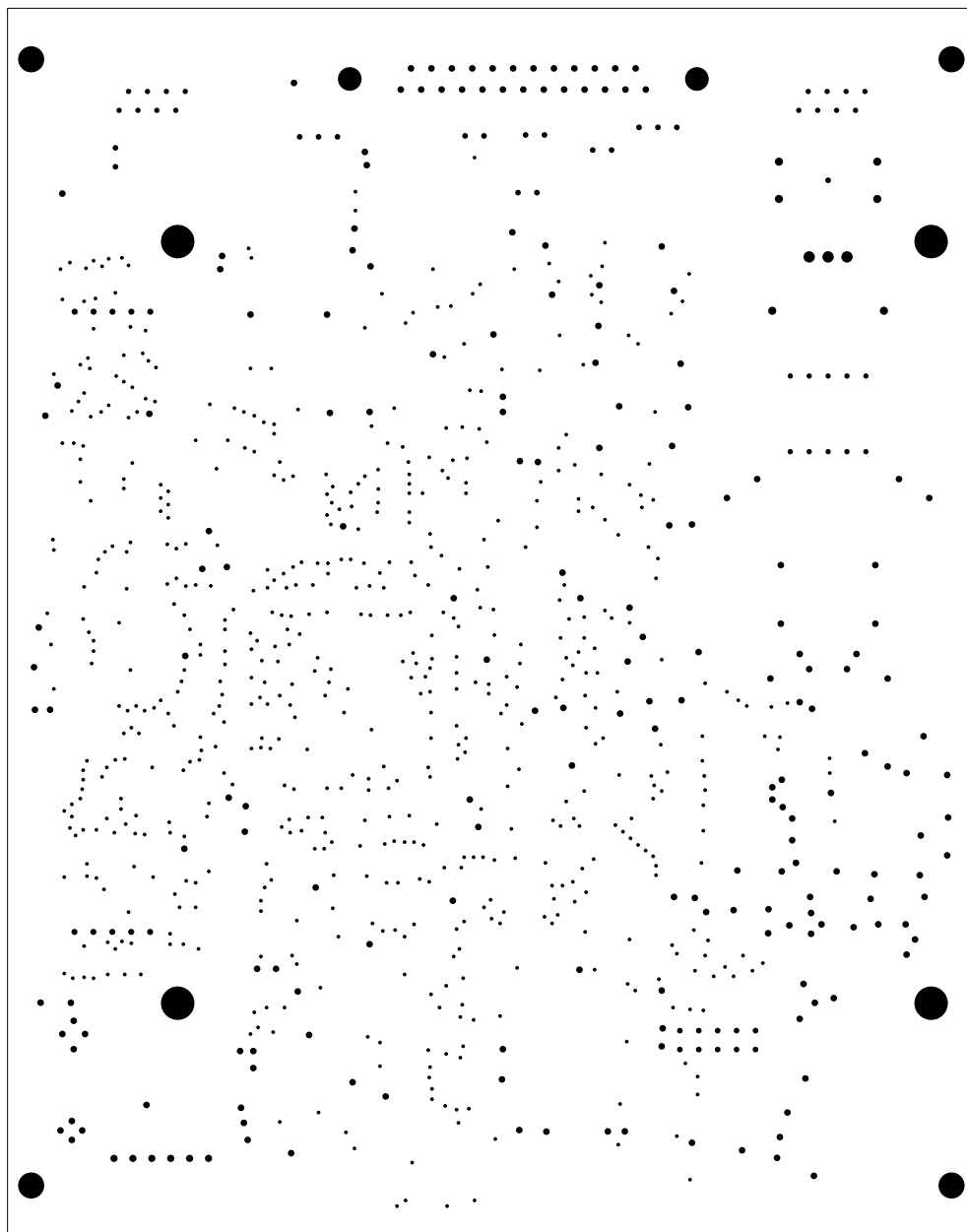


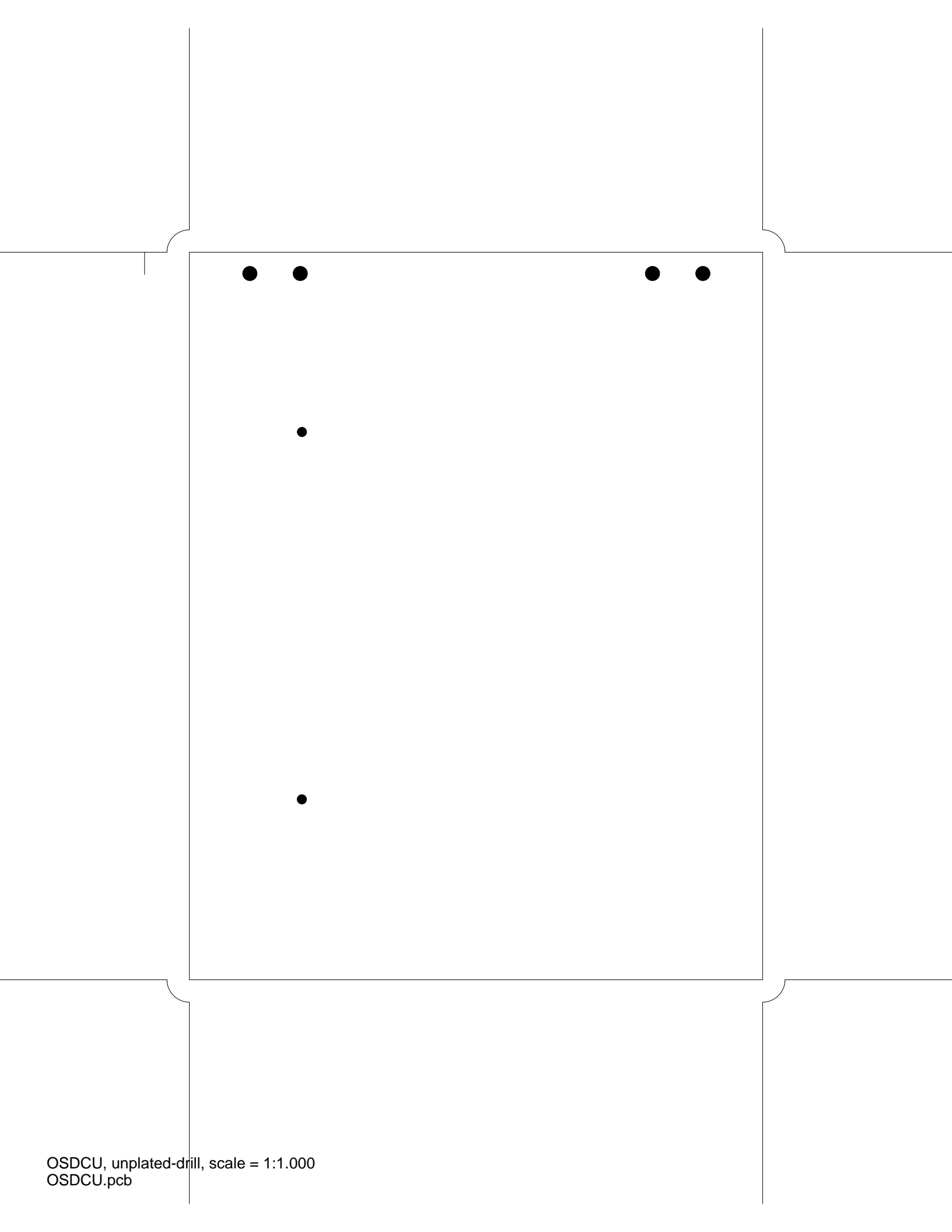


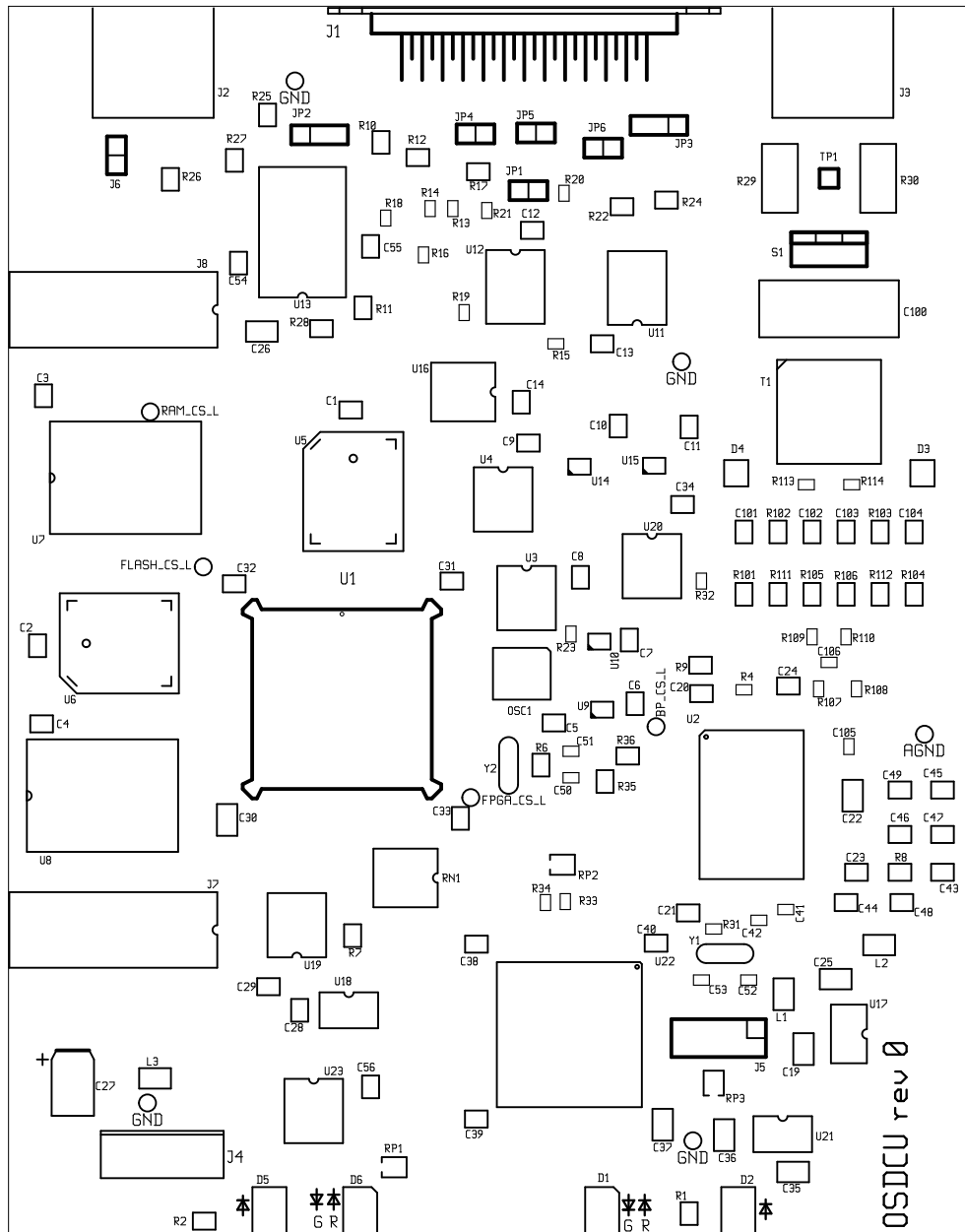




OSDCU, backmask (mirrored), scale = 1:1.000
OSDCU.pcb







○ Harhan Engineering Co. ○
SDSL Physical I/F
Design by Michael Sokolov
Layout by Ineiev

C16 C15

FPGA_CS_L ○

BP_CS_L ○ C17 C18 ○

FLASH_CS_L ○

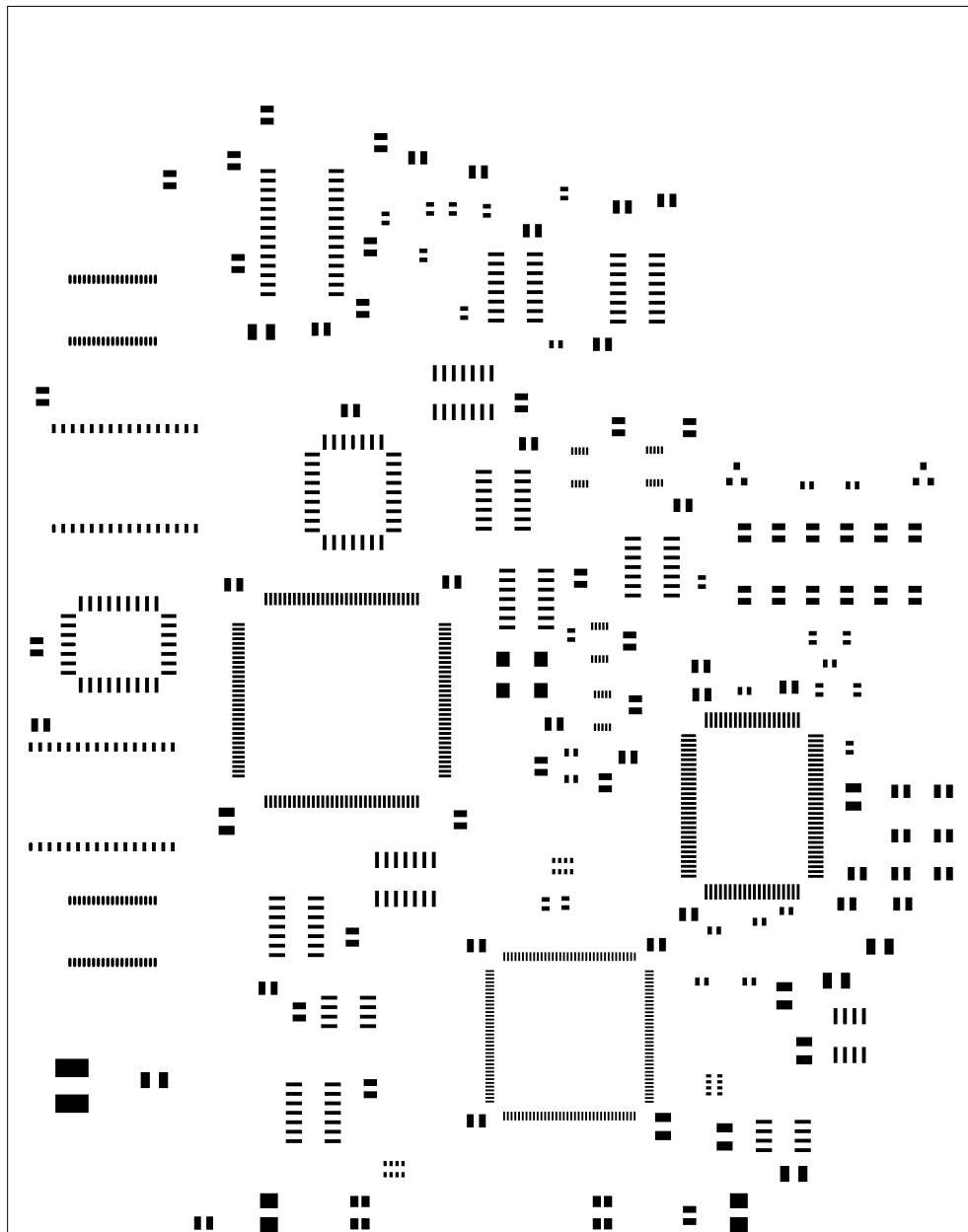
○ RAM_CS_L

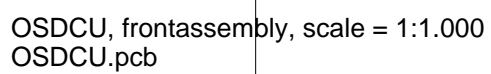
○

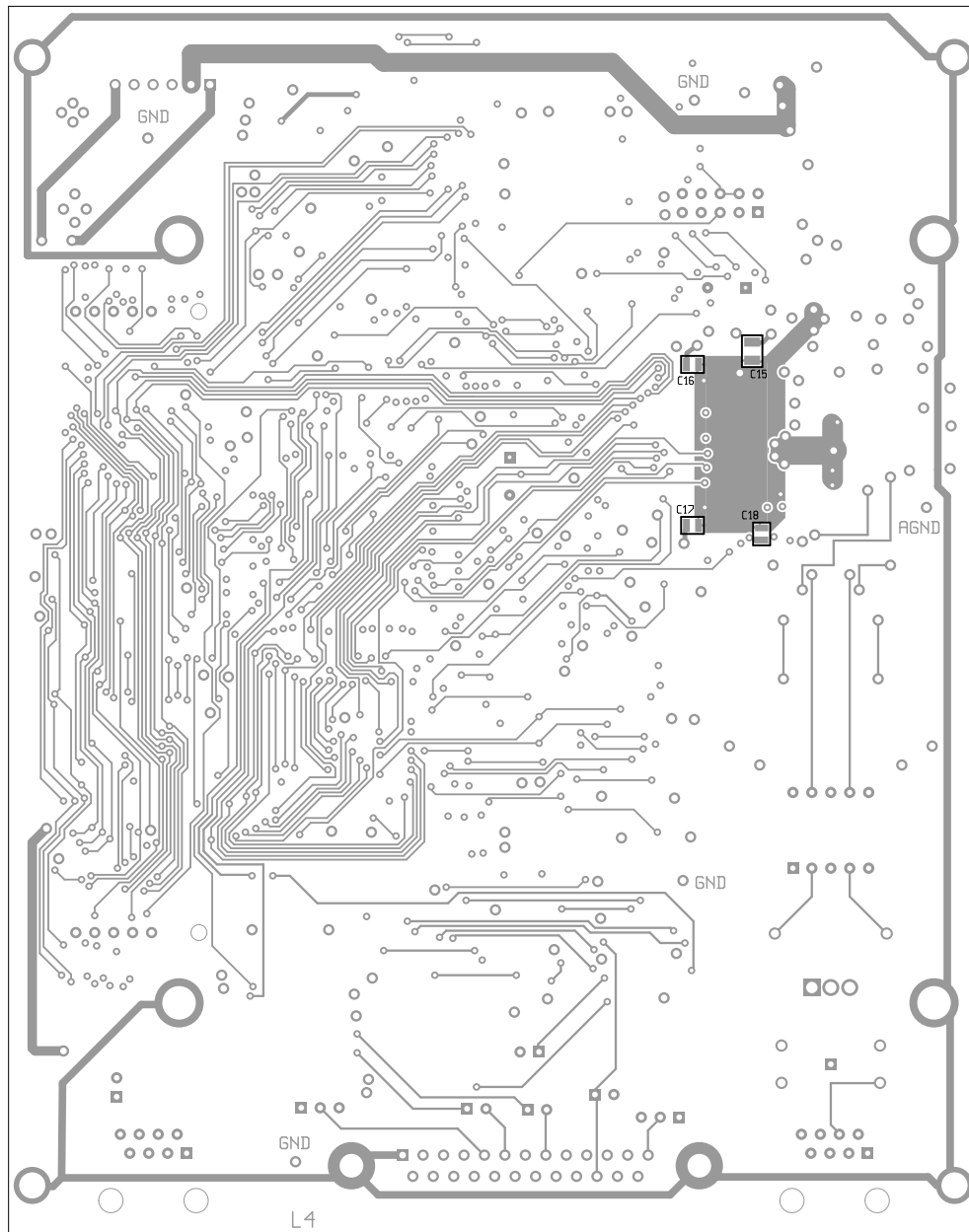
○

" "

" "







There are 13 different drill sizes used in this layout, 914 holes total

Symbol	Diam. (Inch)	Count	Plated?
Y	0.020	625	YES
+	0.028	26	YES
x	0.030	27	YES
•	0.032	10	YES
□	0.035	195	YES
▽	0.038	6	YES
⊕	0.043	6	YES
⊗	0.060	3	YES
⊙	0.084	2	NO
⊠	0.125	2	YES
⊕	0.128	4	NO
⊗	0.138	4	YES
⊠	0.177	4	YES

Title: OSDCU - Fabrication Drawing
Author: Michael Sokolov
Date: Thu Sep 17 18:33:28 2009 UTC
Maximum Dimensions: 5118 mils wide, 6496 mils high



Board outline is the centerline of this 10 mil rectangle - 0,0 to 5118,6496 mils