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Marvell Socket-7 CPU Modules

User Guide

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Section 1. Introduction

The DB-64340/60 and DB-96340/60 Marvell® development boards incorporate a CPU socket compatible to the Socket-7 mechanism, which can accommodate various CPU modules.

This document describes following Socket-7 CPU modules:

- DB-MPC7455DDR-L3-S7 Section 2
- DB-SR71010-S7 Section 3
- DB-IBM750CXe-S7 Section 4
- DB-IBM750FX-S7 Section 5
- DB-RM7000A/B-S7 Section 6
- DB-RM7000C Section 7
- DB-RM9000 Section 8

Each module has its own configuration settings when connected to the various Marvell development boards (backplanes).

Note

These modules are equipped with a I^2C 256 Byte General Purpose EEPROM for future use.

1.1 Documentation Updates and Technical Support

Marvell may have updated the documentation or software (if any) that was shipped with these modules. See the Marvell website at http://www.marvell.com for the following information:

- Assembly map drawings
- Block diagrams
- Module schematics
- BOM
- Gerber files
- PLD equations

Section 2. DB-MPC7455DDR-L3-S7

2.1 Overview

The DB-MPC7455DDR-L3-S7 is a CPU and L3 cache module. This module enables Marvell devices to operate with Motorola's MPC7455 CPU. The module plugs into the Socket-7 connector designed for it.

Note

Due to instability of the HVREF power source, which is used as a reference voltage for the L3 clock, the DB-MPC7455DDR-L3-S7 module supports an **L3 cache** frequency of 166 MHz. This instability will be corrected in rev 2.0 of the board.

Warnings

- Make sure the CPU fan is connected to the power.
- If the fan does not work, the CPU may burn out and the system must be turned off.

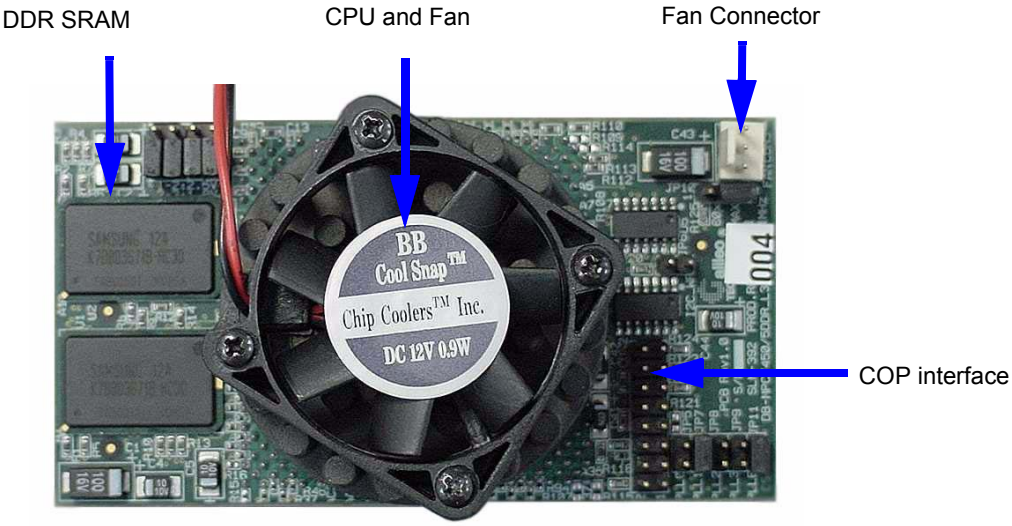
The DB-MPC7455DDR-L3-S7 includes the following features:

- Up to 133 MHz CPU bus frequency
- Optional CPUs (Motorola's MPC7455)
- Onboard L3 cache (supports 2 MB of DDR SRAM L3 cache)
- Debug port (COP interface with standard 16-pin header)

2.2 Description

The DB-MPC7455DDR-L3-S7 module components are illustrated in Figure 1.

Figure 1: DB-MPC7455DDR-L3-S7 Module Components



2.3 DB-MPC7455DDR-L3-S7 Module Jumpers

Table 1 details the DB-MPC7455DDR-L3-S7 module jumpers.

Table 1: DB-MPC7455DDR-L3-S7 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1, JP2, JP3, JP4 (Vcc IO)	1-2, 1-2 1-2, 1-2	CPU's Vcc I/O = 2.5V	The jumpers select the Vcc I/O that is supplied to the module. All four jumpers must be set to the same position. 1-2: Vcc I/O = 2.5V 2-3: Vcc I/O = 1.8V
JP5, JP7, JP8, JP9, JP11 (PLL0-3, PLL_EXT),	**NOTE:** PLL[0..3] and PLL_EXT (JP11) are set according to the CPU's maximum frequency.	According to the CPU's maximum frequency.	For each jumper: In: 0 Out: 1 The frequency setting table can be found in Motorola's specs.
JP10	2-3	MPX bus mode	The jumper selects the CPU's bus mode: 1-2: 60x mode 2-3: MPX mode
JP6 (I^2C_WP)	Out	I^2C memory is not write protected.	When this jumper is In, the I^2C memory on the CPU module is write protected.

Table 2: DB-MPC7455DDR-L3-S7 Module Resistors and DPRs

Resistor	Shipping Configuration	Assignment	Description
DPR4	1-2	Single MV64360	Selects multi-controller configuration: 1-2: Single-MV 2-3: Multi-MV
DPR3	1-2	CPU bus voltage (2.5V)	Selects the CPU bus voltage configuration: 1-2: 2.5V 2-3: 1.8V
R109, R106, R114, R113, R112	**NOTE:** Depends on the CPU's model.	CPU core voltage	Selects the CPU core voltage supply: 1.3V: Out, Out, Out, Out, In 1.6V: Out, In, In, Out, In 1.8V: Out, In, Out, In, In 1.9V: Out, Out, In, In, In **NOTE:** The configuration must be according to the datasheet of the CPU being used.
R110, R104, R56, R29, R51,R45	**NOTE:** Depends on the CPU's model.	CPU core voltage.	Selects CPU core low voltage supply (currently not used): 1.9V: In, Out, In, In, In, In 1.8V: In, In, Out, In, In, In 1.6V: In, In, In, Out, In, In 1.3V: In, Out, Out, Out, In, In
DPR2, DPR7	1-2, 1-2	No PAL present	
R32, R121,R55, R34, R35	Out, Out, Out, Out, Out	JTAG chain connection	When inserted, the JTAG mechanism is available.
DPR6	1-2	COP_TRST pulled up	Selects if the COP_TRST is pulled high or low. 1-2: Pulled high 2-3: Pulled low.
DPR1	1-2	BMODE0 = HRESET	Selects if BMODE0 is connected to GND or HRESET. See Motorola's MPC7455 user manual for more details.

Section 3. DB-SR71010-S7

3.1 Overview

The DB-SR71010-S7 is a CPU and L3 cache module. This module enables Marvell devices to operate with SandCraft's SR71010 CPU. The module plugs into the Socket-7 connector designed for it.

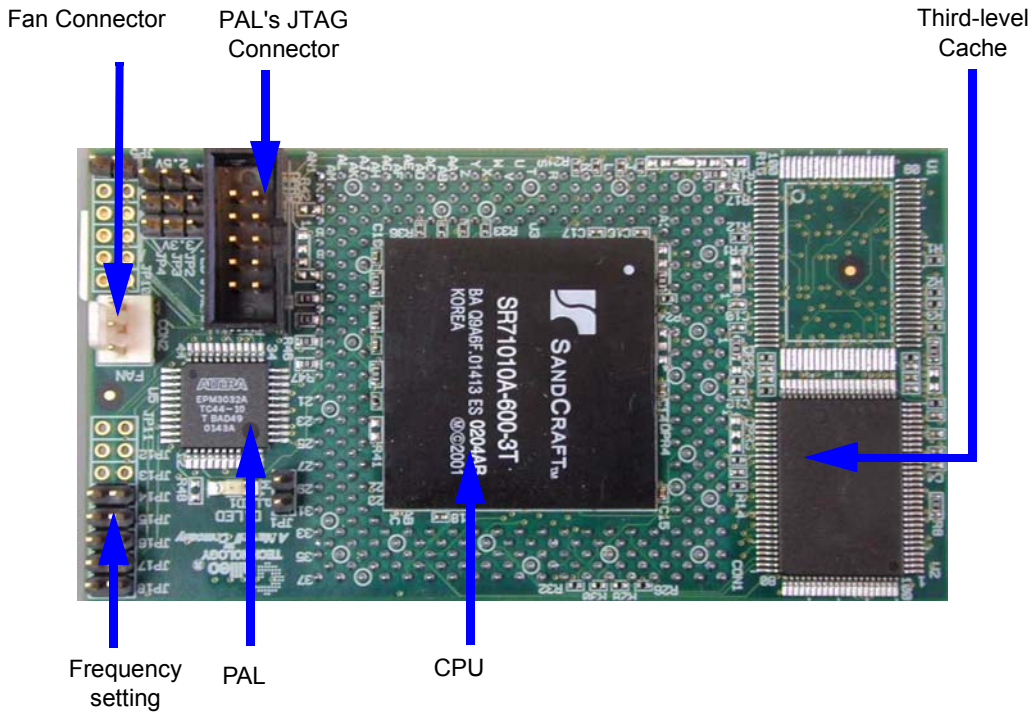
The DB-SR71010-S7 includes the following features:

- Up to 133 MHz CPU bus frequency
- CPU (SandCraft's SR71010 CPU)
- Onboard L3 cache (Supports 2 MB or 4 MB of L3 cache)
- Configurable jumpers for logic reset, I^2C write protect and Vcc I/O voltage
- Configurable DPR for logic reset, L3 cache SRAM size
- Configurable resistor for Linear or Interleave Burst mode, Vcc INT voltage
- Reference power supply circuit (supports various CPU voltages)

3.2 Description

The DB-SR71010-S7 module components are illustrated in Figure 2.

Figure 2: DB-SR71010-S7 Module Components



3.3 DB-SR71010-S7 Module Jumpers

Table 3 details the DB-SR71010-S7 module jumpers.

Table 3: DB-SR71010-S7 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1	In	Write protect	Serial EEPROM Write protect: In - Write protect Out - Write enable
JP2-JP4	1-2	Configure Vcc I/O	Configure Vcc I/O to 2.5V/3.3V: 1-2: Vcc I/O 2.5V 2-3: Vcc I/O 3.3V
JP5	Out		Reserved input to PAL
JP14 (Multi-4)	Depends on the CPU's maximum frequency	CPU's bus frequency multiplied by 4	The CPU's bus frequency multiplied by 4. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP15 (Multi-4.5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 4.5	The CPU internal frequency multiplied by 4.5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP16 (Multi-5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 5	The CPU internal frequency multiplied by 5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP17 (Multi-5.5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 5.5	The CPU internal frequency multiplied by 5.5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP18 (Multi-6)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 6	The CPU internal frequency multiplied by 6. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.

Table 4 details the DB-SR71010-S7 module resistor configuration.

Table 4: DB-SR71010-S7 Module Configuration Resistor

Resistor	Shipping Configuration	Assignment	Description
R6	Not connected	Interleave Burst	Linear or Interleave Burst mode: Connected - Linear Burst Not connected - Interleave Burst

Section 4. DB-IBM750CXe-S7

4.1 Overview

The DB-IBM750CXe-S7 is a CPU module that enables Marvell devices to operate with IBM's 750CXe CPU. The module plugs into the Socket-7 connector designed for it.

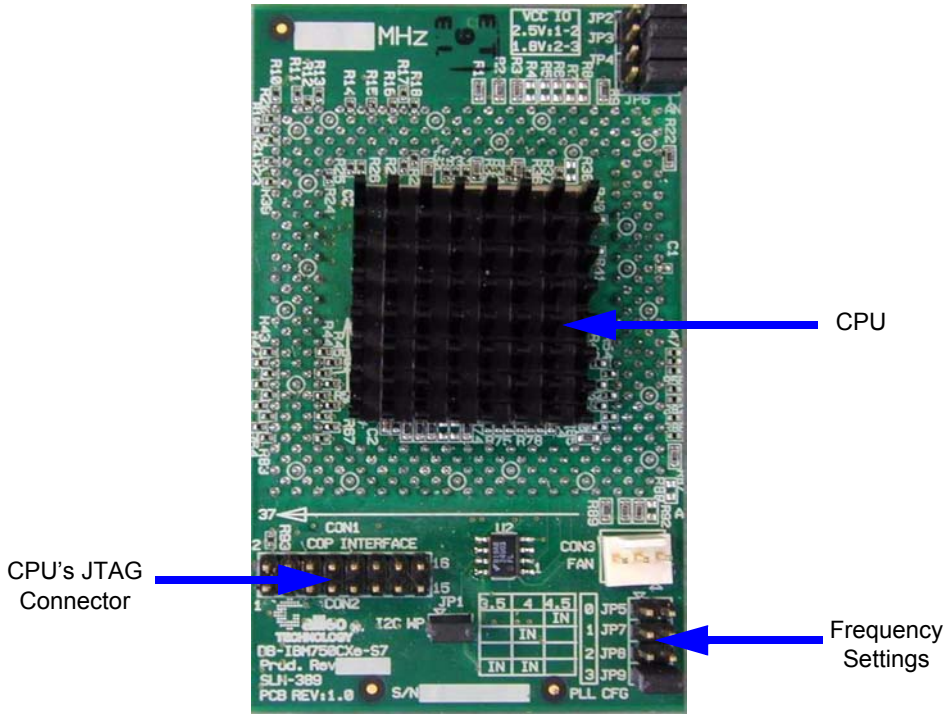
The DB-IBM750CXe-S7 includes the following features:

- Up to 133 MHz CPU bus frequency
- 60x bus arbiter (supports Marvell's internal 60x bus arbiter, or any other arbiter placed on the backplane)
- Debug interface (COP interface, standard 16-bit header)
- Reference power supply circuit (supports various CPU voltages)

4.2 Description

The DB-IBM750CXe-S7 module components are illustrated in Figure 3.

Figure 3: DB-IBM750CXe-S7 Module Components



4.3 DB-IBM750CXe-S7 Module Jumpers

Table 5 details the DB-IBM750CXe-S7 module jumpers.

Table 5: DB-IBM750CXe-S7 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP2, JP3, JP4, JP6 (Vcc IO)	1-2, 1-2 1-2, 1-2	CPU's Vcc I/O = 2.5V	The jumpers select the Vcc I/O that is supplied to the module. All four jumpers must be set to the same position. 1-2: Vcc I/O = 2.5V 2-3: Vcc I/O = 1.8V
JP5, JP7, JP8, JP9 (PLL_CF)	Depends on the CPU's maximum frequency		**JP 5 JP7 JP8 JP9** **x3.5** Out Out Out In **x4** Out In Out In **x4.5** In Out Out Out
JP1 (I^2C_WP)	Out	I^2C memory not write protected.	When this jumper is In, the I^2C memory is write protected.

Table 6: DB-IBM750CXe-S7 Module Resistors and DPRs

Resistor	Shipping Configuration	Assignment	Description
DPR5	1-2	Single MV64360	Selects multi-controller configuration: 1-2: Single controller 2-3: Multi-controller
DPR2	1-2	CPU bus voltage	Selects CPU bus voltage configuration: 1-2: 2.5V 2-3: 1.8V
R88, R87, R92, R91, R90	Depends on CPU's model.		Selects CPU core voltage supply: 1.65V: In, In, In, Out, in 1.80V: Out, In, Out, In, in 1.90V: Out, Out, In, In, in
R85, R89, R8, R33, R29	Depends on CPU's model.	CPU core voltage	Selects CPU Core Low Voltage Supply (currently not used): 1.9V: In, Out, In, In, In, In 1.8V: In, In, Out, In, In, In 1.6V: In, In, In, Out, In, In 1.3V: In, Out, Out, Out, In, In
DPR3, DPR4	1-2, 1-2	No PAL present	
R4, R5, R6, R7, R38	Out, Out, Out, Out, Out	No JTAG connection	When resistors inserted, the JTAG mechanism is available

Table 6: DB-IBM750CXe-S7 Module Resistors and DPRs (Continued)

Resistor	Shipping Configuration	Assignment	Description
DPR1	1-2	COP_TRST pulled up	Selects if COP_TRST is pulled high or low.

Section 5. DB-IBM750FX-S7

5.1 Overview

The DB-IBM750FX-S7 is a CPU module compatible with the Socket-7 mechanism. It provides the interface between the CPU and main board, enabling the Marvell device to operate with IBM's 750FX CPU.

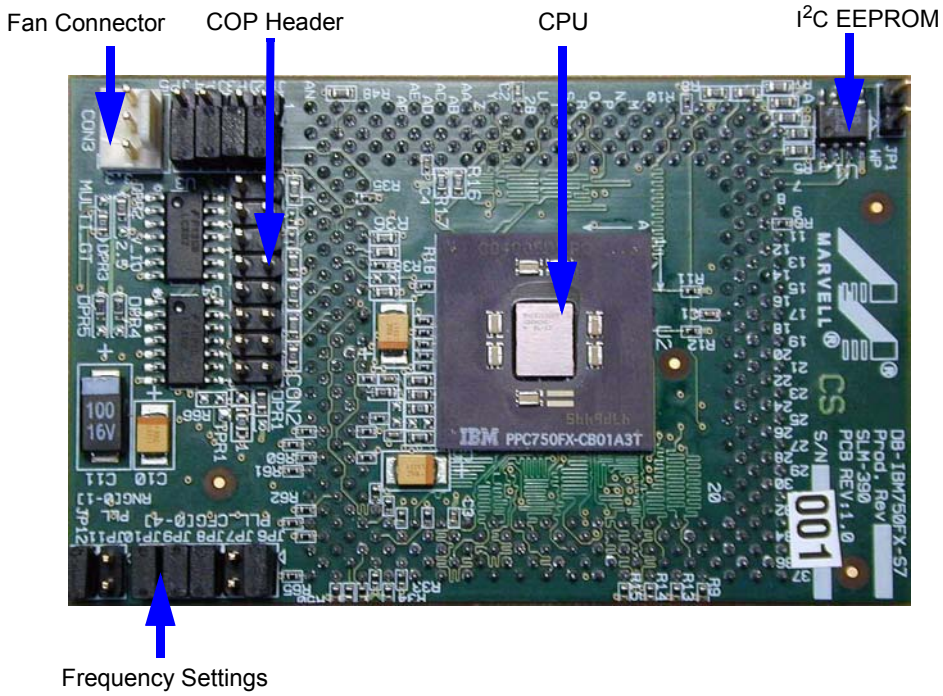
The DB-IBM750FX-S7 includes the following features:

- Up to 133 MHz CPU bus frequency.
- 60x bus arbiter (Supports Marvell's internal 60x bus arbiter, or any other arbiter placed on the backplane.)
- Debug interface (COP interface (standard 16-bit header)
- Reference power supply circuit (supports various CPU voltages)

5.2 Description

The DB-IBM750FX-S7 module components are illustrated in Figure 4.

Figure 4: DB-IBM750FX-S7 Module Components



5.3 DB-IBM750FX-S7 Module Jumpers

Table 7 details the DB-IBM750FX-S7 module jumpers.

Table 7: DB-IBM750FX-S7 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP2, JP3, JP4, JP5 (Vcc IO)	2-3, 2-3 2-3, 2-3	CPU's Vcc I/O =	These jumpers select the Vcc I/O that is supplied to the module. All four jumpers must be set to the same position (either all left or all right). 1-2: Vcc I/O = 1.8V 2-3: Vcc I/O = 2.5V
JP6, JP7, JP8, JP9, JP10 (PLL_CF)	System dependent		The CPU's PLL configuration for the internal frequency multiplication. The following details the most common configuration assuming the system's clock (sysclock) is 133 MHz. **Frequency (MHz) JP6 JP7 JP8 JP9 JP10** **533 In Out In In In** **600 In Out In In Out** **666 In Out In Out In**
JP11, JP12	System dependent		The CPU's PLL range configuration for internal frequency range: **Frequency (MHz) JP11 JP12** **500-750 In In**
JP1 (I^2C_WP)	Out	I^2C EEPROM's write protect disabled.	This jumper controls the I^2C EEPROM write protect mode. Inserting this jumper sets the I^2C EEPROM's write protect mode to enable, thus the EEPROM cannot be written.

Table 8: DB-IBM750FX-S7 Module Resistors and DPRs

Resistor	Shipping Configuration	Assignment	Description
DPR3	1-2	Single MV64360	This DPR selects between multi or single controller: 1-2: Single controller 2-3: Multi-controller
DPR1, TPR1	1-2, 1-2	CPU bus voltage	Selects CPU bus voltage configuration: 1.2, 1.5 or 1.8V: DPR1 2-3, TPR1 1-2 2.5V: DPR1 1-2, TPR1 1-2 3.3V: DPR1 1-2, TPR1 2-4

Table 8: DB-IBM750FX-S7 Module Resistors and DPRs (Continued)

Resistor	Shipping Configuration	Assignment	Description
R1, R8, R2, R4, R3	System dependant	CPU core voltage	Selects CPU core voltage supply (VccInt): 1.2V: Out, Out, Out, Out, Out 1.3V: Out, Out, Out, Out, In 1.4V: Out, In, Out, Out, In
R55, R37, R36, R54, R35	Out, Out, Out, Out, Out	No JTAG connection	When resistors inserted, the JTAG mechanism is available

Section 6. DB-RM7000A/B-S7 Module

The DB-RM7000A/B-S7 is a CPU and L3 cache module. This module enables Marvell devices to operate with QED's RM7000A/B CPUs. The module plugs into the Socket-7 connector designed for it.

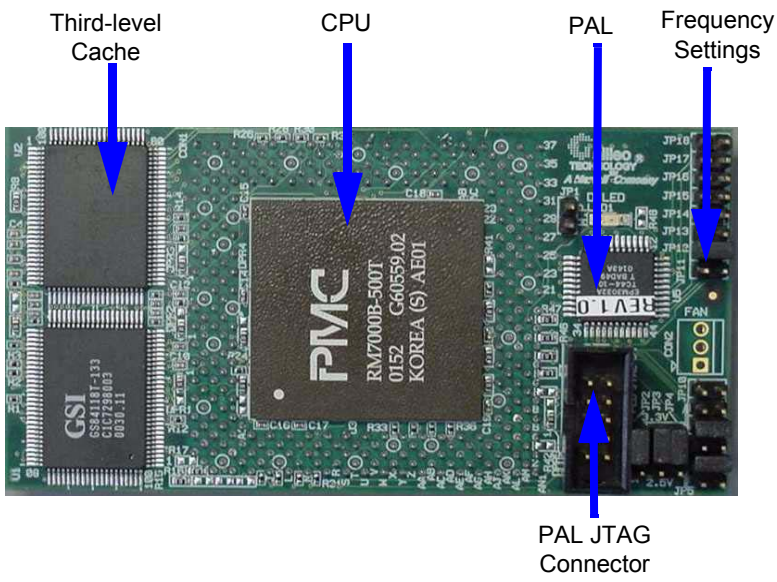
The DB-RM7000A/B-S7 includes the following features:

- Up to 125 MHz CPU bus frequency
- Onboard L3 cache which supports 2 MB or 4 MB of L3 cache
- Configurable jumpers for logic reset
- Configurable DPR for logic reset, L3 cache (SRAM size), L3 cache (TAG RAM type), backplane indication
- Configurable resistor for Linear or Interleave Burst mode, VCC INT voltage
- Reference power supply circuit which supports a number of CPU voltages

6.1 Description

The DB-RM7000A/B-S7 module components are illustrated in Figure 5.

Figure 5: DB-RM7000A/B-S7 Module Components



6.2 DB-RM7000A/B-S7 Module Jumpers

Table 9 details the DB-RM7000A/B-S7 module jumpers.

Table 9: DB-RM7000A/B-S7 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1	In	Write protect	Serial EEPROM Write protect: In: Write protect Out: Write enable
JP2-JP4	1-2	Configure Vcc IO	Configure Vcc IO to 2.5V/3.3V: 1-2: Vcc IO 2.5V 2-3: Vcc IO 3.3V
JP5	Out		Reserved input to PAL
JP6 (CFG11)	In	CPU timer interrupt disable	Disables timer interrupt on INT[5]: (For VxWorks, must be "In".) In: Timer interrupt enable Out: Timer interrupt disable
JP7 (CFG12)	Out	Enable tertiary cache	Tertiary cache interface: In: Disable Out: Enable
JP8 (CFG25)	Out	Enable secondary cache	Enables integrated secondary cache: In: Disable Out: Enable
JP9 (CFG26)	Out	Disable	Enables two outstanding read write out-of-order returns: In: Enable Out: Disable **NOTE:** This feature can only be enabled if the tertiary cache is disabled.
JP10 (DRVOUT-FAST)	Out	CPU output drive slow rate control	CPU output drive slow rate control: In: 100% Out: 83%
JP11 (Multi- 2.5)	Depends on the CPU's maximum frequency	CPU's bus frequency multiplied by 2.5	The CPU's bus frequency multiplied by 2.5. If more than one jumper is used, the lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP12 (Multi-3)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 3	The CPU internal frequency multiplied by 3. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.

Table 9: DB-RM7000A/B-S7 Module Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
JP13 (Multi-3.5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 3.5	The CPU internal frequency multiplied by 3.5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP14 (Multi-4)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 4	The CPU internal frequency multiplied by 4. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP15 (Multi-4.5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 4.5	The CPU internal frequency multiplied by 4.5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP16 (Multi-5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 5	The CPU internal frequency multiplied by 5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP17 (Multi-5.5)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 5.5	The CPU internal frequency multiplied by 5.5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP18 (Multi-6)	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 6	The CPU internal frequency multiplied by 6. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.

Table 10 details the DB-RM7000A/B-S7 module DPRs.

Table 10: DB-RM7000A/B-S7 Module DPRs

DPR	Shipping Configuration	Assignment	Description
DPR1	1-2	2 MB Third-level cache	Configuration for 2 MB or 4 MB Third-level cache: 1-2: 2 MB 2-3: 4 MB
DPR2	1-2	2 MB Third-level cache	Configuration for 2 MB or 4 MB Third-level cache: 1-2: 2 MB 2-3: 4 MB
DPR3	1-2	GS84118T	Configuration for GS84118T or MCM69T618/GVT164T18 tag RAM: 1-2: GS84118T 2-3: MCM69T618/GVT164T18
DPR4	1-2	GS84118T	Configuration for GS84118T or MCM69T618/GVT164T18 tag RAM: 1-2: GS84118T 2-3: MCM69T618/GVT164T18
DPR5	1-2		Reserved input to backplane PAL
DPR6	1-2	2 MB Third-level cache	Configuration for 2 MB or 4 MB Third-level cache: 1-2: 2 MB 2-3: 4 MB
DPR7	1-2	CPU type RM7000A/B	Select CPU type RM7000A/B: 1-2: ‘0’ 2-3: ‘1’
DPR8	1-2	CPU type RM7000A/B	Select CPU type: 1-2: ‘0’ 2-3: ‘1’
DPR9	1-2	LVCMOS	CPU interface to GT is HSTL or LVCMOS: 1-2: LVCMOS 2-3: HSTL
DPR10	1-2	Vcc IO voltage 2.5V	Indication of Vcc IO voltage for backplane 2.5V/3.3V: 1-2: 2.5V 2-3: 3.3V
DPR11	1-2	Big Endian	Specified byte ordering Big Endian or Little Endian: 1-2: Big Endian 2-3: Little Endian

Table 11 details the RM7000A/B module resistor configuration.

Table 11: DB-RM7000A/B-S7 Module Configuration Resistor

Resistor	Shipping Configuration	Assignment	Description
R6	Not connected	Interleave Burst	Linear or Interleave Burst mode: Connected - Linear Burst Not connected - Interleave Burst

Table 12 details the DB-RM7000A/B module Vcc INT voltage resistor configuration.

Table 12: Vcc INT Voltage Resistor Configuration

Resistor	RM7000A - 1.65V Vcc INT	RM7000B - 1.5V Vcc INT
R15	Connected	Connected
R16	Connected	Connected
R17	Not connected	Not connected
R19	Connected	Not connected
R20	Connected	Not connected
R21	Not connected	Not connected
R22	Not connected	Not connected
R41	Not connected	Not connected
R42	Not connected	Not connected
R43	Not connected	Not connected
R48	Not connected	Not connected

Section 7. DB-RM7000C

The DB-RM7000C is a CPU and L3 cache module. This module enables Marvell devices to operate with RM7000C CPUs. The module plugs into the Socket-7 connector designed for it.

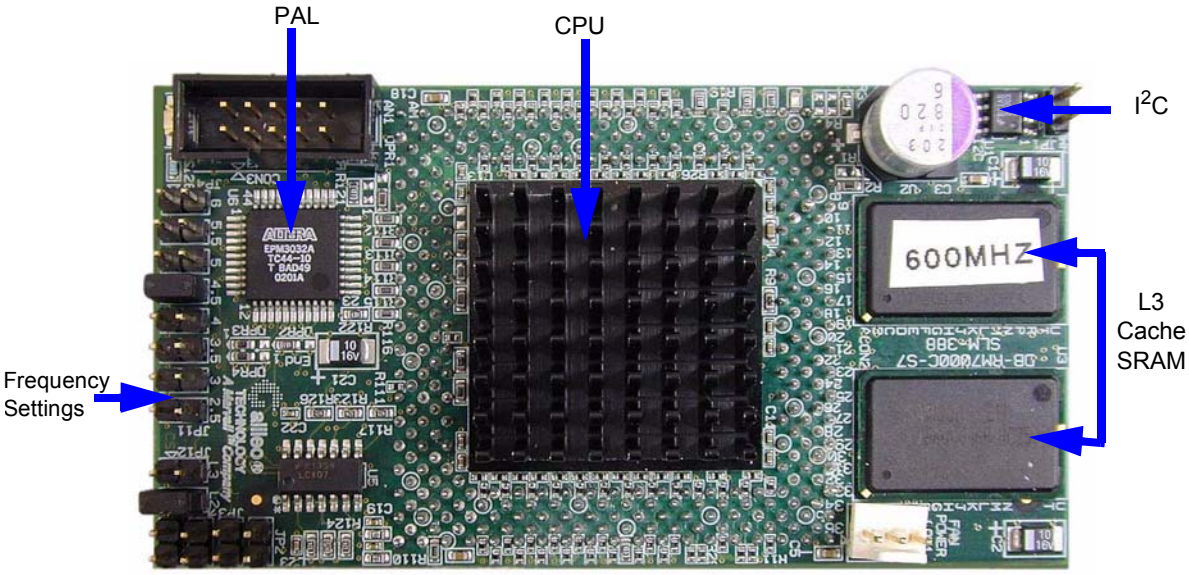
The DB-RM7000C includes the following features:

- Up to 200 MHz maximum frequency using HSTL signaling on the SysAD bus
- Onboard L3 cache
  - Supports EZ cache protocol, which eliminates the need for external tag RAMs
- Configurable jumpers for logic reset
- Configurable DPR for logic reset, backplane indication
- Configurable resistor for Linear or Interleave Burst mode, Vcc INT voltage
- Reference power supply circuit
  - Supports a number of CPU voltages

7.1 Description

The DB-RM7000C module components are illustrated in Figure 6.

Figure 6: DB-RM7000C Module Components



7.2 DB-RM7000C Module Jumpers

Table 13 details the DB-RM7000C module jumpers.

Table 13: DB-RM7000C Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP15	Out	Reserved input for PAL	
JP3	In	TmrIntEn	Timer Interrupt In: Enabled Out: Disabled
JP12	Out	Tertiary cache interface	Enable tertiary cache In: Disabled Out: Enabled
JP14	Out	Integrated Secondary cache	Enable secondary cache In: Disabled Out: Enabled
JP2	Out	Two outstanding reads with out-of-order return	Enables two outstanding read write out-of-order returns: In: Enable Out: Disable **NOTE:** This feature can only be enabled if the tertiary cache is disabled.
JP4-JP11	CPU Dependant	CPU interface frequency multipliers	The default value is x2 (all jumpers are Out.) If more than one jumper is, inserted, the smallest value is taken.
JP13	Out	CPU output drive slew rate control: 100/83%	In: 100% Out: 83%
JP1	Out	I^2C write protect	In: Write protect Out: No write protect

Table 14 details the DB-RM7000C module DPR.

Table 14: DB-RM7000C Module DPR

DPR	Shipping Configuration	Assignment	Description
DPR1	Connected on pins 1-2	PAL[0]	Reserved for internal use
DPR2	Connected on pins 1-2	EndBIt - Specifies byte ordering. Logically ORed with the Big Endian signal	Big Endian Ordering 1-2: Big endian 2-3: Little Endian
DPR3	Connected on pins 1-2	CPU_TYPE0	RM7000C
DPR4	Connected on pins 1-2	CPU_TYPE1	RM7000C

Table 14: DB-RM7000C Module DPR (Continued)

DPR	Shipping Configuration	Assignment	Description
DPR5	Connected on pins 1-2	SRAM0 ZQ	Reserved for internal use
DPR6	Connected on pins 1-2	SRAM1 ZQ	Reserved for internal use

Table 15 details the DB-RM7000C module Vcc INT voltage resistor configuration.

Table 15: Vcc INT Voltage Resistor Configuration

Resistor	RM7000C - Vcc INT
R1	Depends on local CPU voltage.
R2	Depends on local CPU voltage.
R3	Depends on local CPU voltage.
R4	Depends on local CPU voltage.
R5	Depends on local CPU voltage.
R6	Depends on local CPU voltage.
R7	Depends on local CPU voltage.
R109	Depends on local CPU voltage.
R112	Depends on local CPU voltage.
R116	Depends on local CPU voltage.

Section 8. DB-RM9000 Module

The DB-RM9000 is a CPU and L3 cache module. This module enables Marvell devices to operate with QED's RM9000 CPUs.

The DB-RM9000 includes the following features:

- Up to 125 MHz CPU bus frequency in CMOS mode, and 200 MHz in HSTL mode
- CPU RM9000
- Configurable jumpers for logic reset
- 128 DDR Memory (166 Mhz Max) connected to the CPU dedicated interface.

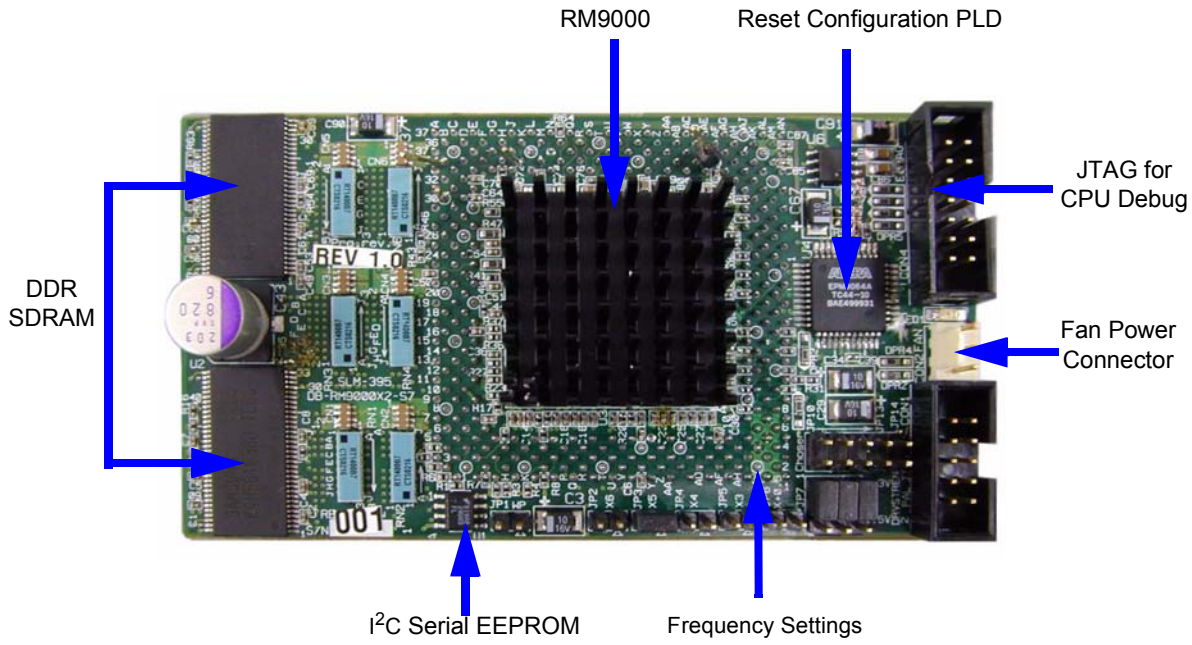
Note

The DB-RM9000 has a number of restrictions. For a list of restrictions, see "DB-RM9000 Restrictions" on page 30.

8.1 Description

The DB-RM9000 module components are illustrated in Figure 7.

Figure 7: DB-RM9000 Module Components



8.2 DB-RM9000 Module Jumpers

Table 16 details the DB-RM9000 module jumpers.

Table 16: DB-RM9000 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1	In	Write protect	Serial EEPROM Write protect: In: Write protect Out: Write enable
JP7-JP9	1-2	Configure Vcc IO	Configure Vcc IO to 1.5V/3.3V: 1-2: Vcc IO 3.3V 2-3: Vcc IO 1.5V (HSTL mode)
JP11	Out	CPU Core B enable	In: Core B enable Out: Core B disable
JP13	In	CPU timer interrupt disable	Disables timer interrupt on INT[5] (For VxWorks, must be "In".) In: Timer interrupt enable Out: Timer interrupt disable
JP14	Out	CPU output drive slew rate control (100%)	CPU output drive slew rate control: In: 100% Out: 83%
JP10	Out	Not in use.	
JP6	Depends on the CPU's maximum frequency		Add 0.5 to the CPU internal frequency multiplier (configured by JP7-JP9).
JP5	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 3.	The CPU internal frequency multiplied by 3. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP4	Depends on the CPU's maximum frequency.	CPU internal frequency multiplied by 5.	The CPU internal frequency multiplied by 5. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP3	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 7.	The CPU internal frequency multiplied by 7. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.

Table 16: DB-RM9000 Module Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
JP2	Depends on the CPU's maximum frequency	CPU internal frequency multiplied by 8.	The CPU internal frequency multiplied by 8. The lowest value is used. The maximum frequency is limited by the CPU device capabilities. Refer to the respective CPU specification for more information.
JP12	Out	Second level cache enable	In: Disable Out: Enable

Table 17 details the DB-RM9000 module DPR.

Table 17: DB-RM9000 Module DPR

DPR	Shipping Configuration	Assignment	Description
DPR1	1-2		Reserved input to PAL
DPR10	1-2	LVCMOS	CPU interface to MV is HSTL or LVCMOS: 1-2- LVCMOS 2-3- HSTL
DPR3	2-3	Vcc IO voltage	Indication of Vcc IO voltage for backplane 1.5V/3.3V: 1-2: 1.5V 2-3: 3.3V
DPR4	1-2	Big Endian	Specified byte ordering Big Endian or Little Endian: 1-2- Big Endian 2-3- Little Endian
DPR5	1-2	SPARE0 (into the PAL)	1-2- "1"
DPR6	1-2	SPARE1 (into the PAL)	2-3- "0"
DPR7	1-2	1-2: Pull-Down 2-3: Pull-Up	Reserved
DPR8	1-2	1-2: Pull-Up 2-3: Pull-Down	Reserved.
DPR9	1-2	1-2: Pull-Up 2-3: Pull-Down	Reserved.
DPR2	1-2	CPU bus voltage type	1-2: CMOS 2-3: HSTL

Table 18 details the DB-RM9000 module VCC INT voltage resistor configuration.

Table 18: VCC INT Voltage Resistor Configuration

Resistor	DB-RM9000 - 1.25V Vcc INT
R6	Not connected
R7	Not connected
R5	Not connected
R11	Not connected
R12	Not connected
R14	Not connected
R1	Not connected
R25	Not connected
R97	Not connected
R42	Not connected

8.3 DB-RM9000 Restrictions

The DB-RM9000 has the followings restrictions:

- When using the DB-RM9000 with the DB-64340-BP and PMON monitor, the DB-64340-BP can only be equipped with 128 MB of memory. Using more than 128 MB will cause the system to hang.
- The RM9000 internal registers base address is set by the boot stream initialization PAL to address: 0x8000000. To use a different base address, reprogram the PAL. The source code for the PAL can be found on the secure web site.

Section 9. Revision History

Table 19: Revision History

Revision Number	Date	Comments
Rev. A	May 21, 2002	First Release
Rev. B	June 12, 2002	1. Added Section 3 (DB-SR71010-S7) 2. Added Section 4 (DB-IBM750CXe-S7) 3. Added Section 5 (DB-IBM750FX-S7) 4. Added Section 6 (DB-MPC7410-S7)
Rev. C.	June 19, 2002	1. Updated Section 2 (DB-MPC7455DDR-L3-S7) 2. Deleted Section 6 (DB-MPC7410-S7)
Rev. D	Nov. 26, 2002	1. Updated the Jumper settings in Table 1 of Section 2. 2. Changed JP2-JP4 shipping configuration in Table 3 of Section 3. 3. Added Section 6 (DB-RM7000A/B-S7) 4. Added Section 7 (DB-RM7000C) 5. Added Section 8 (DB-RM9000)
Rev. E	January 30, 2003	1. Updated Section 2 (DB-MPC7455DDR-L3-S7); note concerning L3 cache frequency added. 2. Added Address Page 3. Cover Page replaced

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