COMMUNICATIONS
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Marvell Solutions

DB-64340/60-BP

Development Board User Guide

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Advanced Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Document Conventions

Note

Provides related information or information of special importance.

Caution

Indicates potential damage to hardware or software, or loss of data.

Warning

Indicates a risk of personal injury.

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Section 1. Introduction

The DB-64340/60-BP Development Board was designed to evaluate the Marvell® high-end MV64340/360 system controller. The DB-64340/60-BP Development Board provides you with a reference design platform to begin system development prior to hardware availability.

1.1 DB-64340/60-BP Components and Features

The features and components of the DB-64340/60-BP Development Board are as follows:

- PPC Single/Dual processor support (Via one/two SOCKET-7 connectors):
  - Motorola MPC7410
  - Motorola MPC7455
  - Motorola MPC7450
  - IBM 750FX
  - IBM 750CXE
- MIPS processor support (via one SOCKET-7 connector)
  - RM7000A/B
  - SR71010
  - RM9000
  - RM7000C (HSTL interface)
- Marvell's DB-64340/60-BP (133 MHz) system controller
  - Features Marvell's MIPS/PPC system controller (2 X 66 64-bit MHz PCI 2.2 or 2 X 133 MHz PCI-X).
- Double Data Rate (DDR) SDRAM (PC266) Memory support:
  - Dual Inline Memory Module (DIMM) sockets to support PC266 compliant (64, 128, 256, 512, or 1 Gb device) modules. Up to 8 GB of memory, registered and non-registered modules.
- Two COM ports connectors:
  - Can be driven by the device module's Dual UART or the MV64340/360's MPSCs.
- Two 60-pin MPSC connectors:
  - Connected to the MV64340/360 MPSC's interface and uses Marvell's special modules.
- Two-Wire Serial Interface (TWSI) EEPROM and interface:
  - The MV64340/360 can be initialized from an TWSI EEPROM. It also has full TWSI master and slave capabilities. The TWSI bus is connected to two DDR SDRAM DIMMs and to a connector which allows the connection of external devices.
- The board is designed with the ATX form factor standard.

1.2 Shipping Contents

The DB-64340/60-BP package is shipped with the following components.

- One DB-64340/60-BP Development Board
- One/two CPU modules installed on the board.

Warning

Do not remove the CPU modules from the board. Doing so may cause damage to the board and/ or the modules. Marvell takes no responsibility for damage caused to the boards or the modules if you do not heed this warning.

- One/two power modules
- One device module (EV-DEVICES-D144)
- One DDR SDRAM DIMM

Note

The DIMM must be installed for proper operation.

If any of the above items are missing or damaged, contact your distributor or local Marvell FAE.

1.3 Related Documentation

See the Marvell SOCKET-7 CPU Modules User Manual for additional information.

1.4 Additional Collateral

See the Marvell website, http://www.marvell.com for the following collateral:

- PLD equations
- Assembly map drawings
- Monitor Manuals
- Monitor Source Code
- Software Drivers
- BOM
- Block Diagram
- A list of modules that work with this board
- Gerber files

Section 2. DB-64340/60-BP Description

Figure 1 illustrates the main components on the board.

Figure 1: DB-64340/60-BP Components

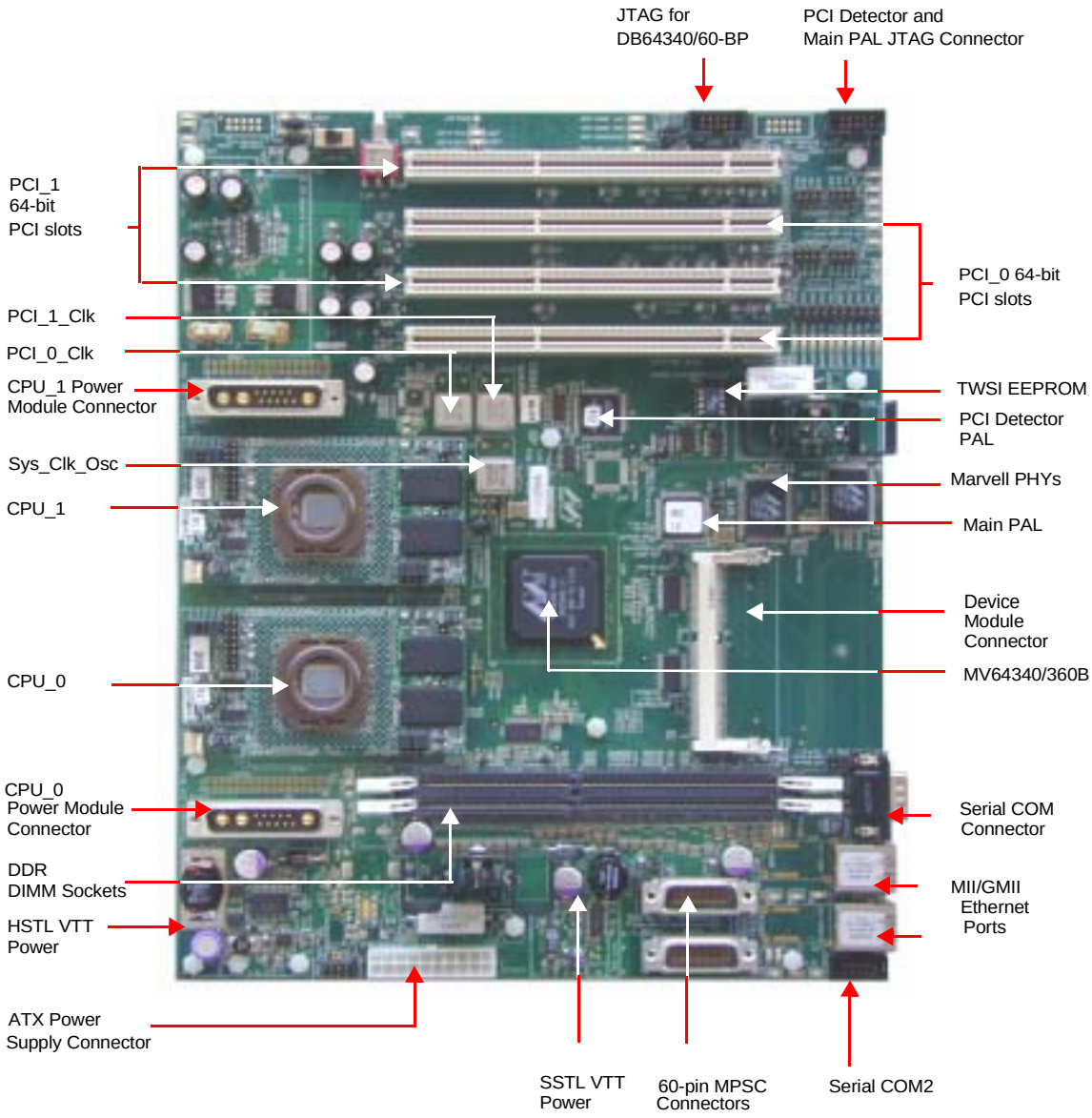
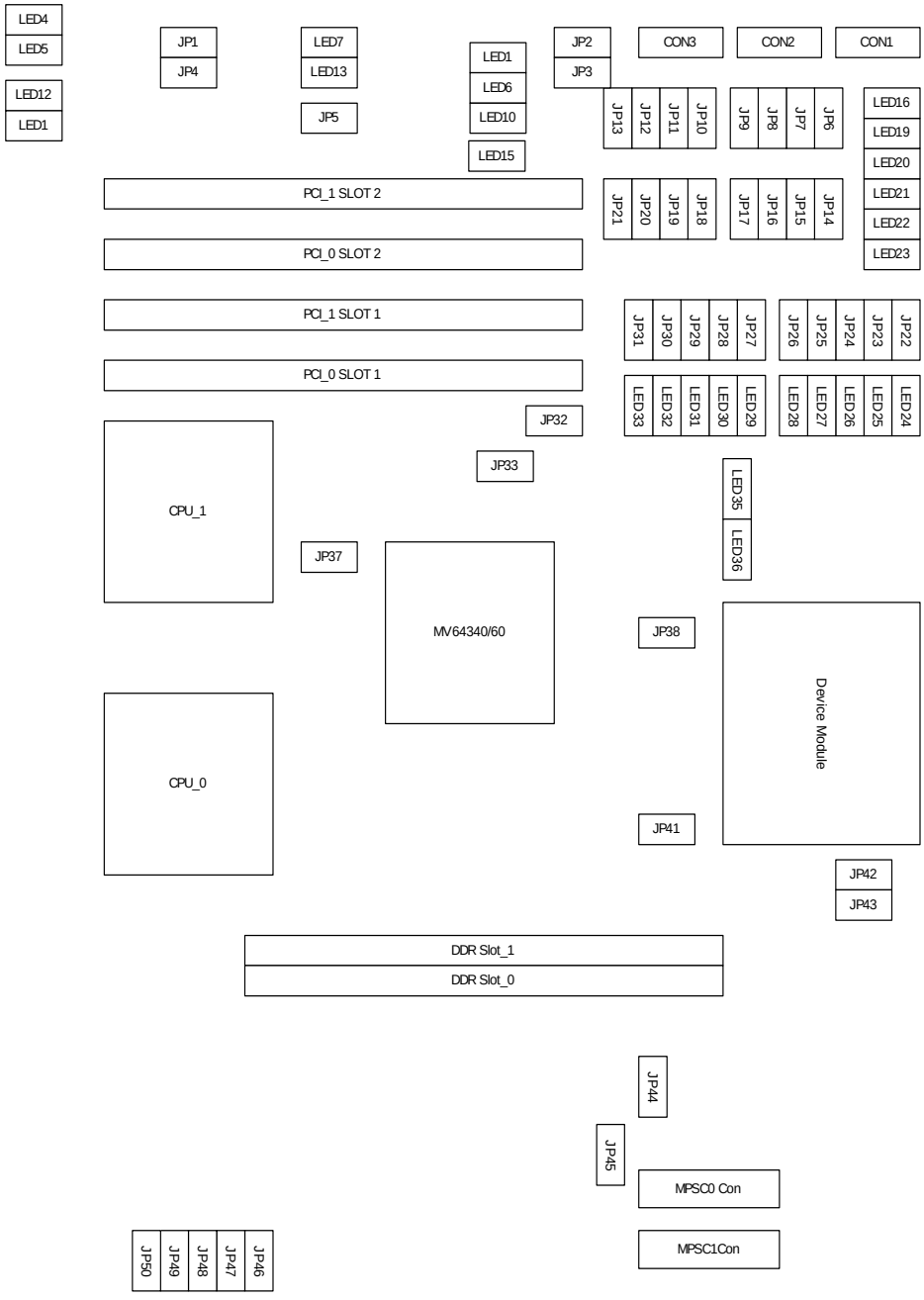


Figure 2 details the jumper locations.

Figure 2: DB-64340/60-BP Jumper Location



Section 3. Getting Started

The DB-64340/60-BP is preconfigured and ready to run.

Note

Marvell recommends testing the board with this standard configuration before changing jumpers or other configuration options.

3.1 Additional Required Items

To use the DB-64340/60-BP Development Board, you need the following items which are not included in the board package:

- Null-modem cable, 9-pin (COM cable)
- ATX PC power supply
- Terminal emulation software, such as Windows 9x, or Windows NT HyperTerminal

Section 4. Hardware Setup

The DB-64340/60-BP expansion cards contain delicate Integrated Circuits (ICs). To protect them against ESD damage, take the following precautions.

Warning

Make sure that the ATX power supply is switched off before you plug in or remove the ATX power connector on the DB-64340/60-BP.

1. Unplug the DB-64340/60-BP power supply.
2. Use a grounded wrist strap before handling DB-64340/60-BP components. If you do not have one, touch your hands briefly to a safely grounded object or to a metal object, such as the power supply case, and then continue.
3. Hold the components by the edges and try not to touch the ICs, connectors, or other components.
4. Place components on a grounded anti-static pad or on the bag that came with the DB-64340/60-BP.

Take the following steps before applying power to the DB-64340/60-BP:

1. Check the DB-64340/60-BP settings. (See Section 4.1)
2. Install the memory modules. (See Section 4.5)
3. Install the CPU power module. (See Section 4.6)
4. Apply power to the DB-64340/60-BP. (See Section 4.7)

4.1 DB-64340/60-BP Feature Settings

The DB-64340/60-BP features are adjusted via the jumpers or the DPRs. The DPRs are used for various functions and are usually left in their default states.

DPRs are the same as 3-pad jumpers. The resistor can be placed on pads 1-2 or pads 2-3.

Table 1: JTAG Chain Bypassing

JP/DPR	Default	Functionality
DPR13 DPR14	1-2 (Bypass)	PHY1 JTAG Chain Bypass 1-2: Bypass 2-3: PHY1 in the chain.
DPR15 DPR16	1-2 (Bypass)	PHY0 JTAG Chain Bypass 1-2: Bypass 2-3: PHY0 in the chain
DPR1 DPR2	1-2 (Bypass)	PCI_1 Device8 JTAG Chain Bypass 1-2: Bypass 2-3: PCI_1 Device8 in the chain

Table 1: JTAG Chain Bypassing (Continued)

JP/DPR	Default	Functionality
DPR3 DPR4	1-2 (Bypass)	PCI_0 Device8 JTAG Chain Bypass 1-2: Bypass 2-3: PCI_0 Device8 in the chain
DPR5 DPR6	1-2 (Bypass)	PCI_1 Device7 JTAG Chain Bypass 1-2: Bypass 2-3: PCI_1 Device7 in the chain
DPR7 DPR8	1-2 (Bypass)	PCI_0 Device7 JTAG Chain Bypass 1-2: Bypass 2-3: PCI_0 Device7 in the chain
DPR12 DPR17	1-2 (Bypass)	CPU_1 JTAG Chain Bypass 1-2: Bypass 2-3: CPU_1 in the chain
DPR22 DPR23	1-2 (Bypass)	CPU_0 JTAG Chain Bypass 1-2: Bypass 2-3: CPU_0 in the chain

Table 2: Reset Sample

DPR	Default	Functionality
DPR51	1-2 (Enable)	DRAM Pad Calibration Enable 1-2: Enable 2-3: Disable
DPR47 [LSB] DPR46 [MSB]	1-2 1-2 ‘00’	Serial ROM Address ‘00’: Address = 1010000 ‘01’: Address = 1010001 ‘10’: Address = 1010010 ‘11’: Address = 1010011
DPR43	1-2	Internal Register Base Address 1-2: 0x14000000 2-3: 0xF1000000
DPR42	1-2 (Enable)	CPU Pad Calibration Enable 1-2: Enable 2-3: Disable
DPR40 [LSB] DPR39 [MSB]	1-2 1-2 ‘00’	Multi-MV Address ID ‘00’: MV response to CPU Address ‘00’ ‘01’: MV response to CPU Address ‘01’ ‘10’: MV response to CPU Address ‘10’ ‘11’: MV response to CPU Address ‘11’
DPR48	1-2 (Enable)	PCI_0 Pad Calibration Enable 1-2: Enable 2-3: Disable

Table 2: Reset Sample (Continued)

DPR	Default	Functionality
DPR45	1-2 (Enable)	PCI_1 Pad Calibration Enable 1-2: Enable 2-3: Disable
DPR19	1-2 (Disable)	PCI Retry 1-2: Disable 2-3: Enable
DPR49	1-2	DRAM Clock 1-2: Core clock (Synchronized Clock) 2-3: Separate Clock (Asynch mode)
DPR30	1-2 (pos-edge)	DRAM Address/Control toggle 1-2: pos-edge 2-3: neg-edge
DPR33 DPR27	1-2 1-2 (One Stage)	DRAM Control pipeline [1:0] ‘00’: Reserved ‘01’: One Stage ‘10’: Two stages ‘11’: Three stages
DPR29 DPR35 DPR28	1-2 1-2 1-2 ‘000’	DRAM read path control
DPR26	1-2 (Disable)	Giga Port #3 Enable 1-2: Disable 2-3: Enable
DPR38 DPR37 DPR25 DPR24 DPR53 DPR52 DPR32 DPR31	2-3 2-3 1-2 2-3 1-2 2-3 1-2 1-2	PLL1 N divider Default Value: “00101011” (N=43)
DPR57	1-2	PLL NP input Default setting ‘1’
DPR55	1-2	PLL1 HIKVCO input Default setting ‘0’
DPR56	1-2 (Normal Operation)	DRAM PLL Power-up 1-2: PLL Power-up 2-3: PLL Power-down

Table 2: Reset Sample (Continued)

DPR	Default	Functionality
DPR82	1-2	Giga Port 0 interface 1-2: MII/GMII 2-3: PCS
DPR76 DPR74 DPR10 DPR73 DPR70 DPR69	1-2 2-3 1-2 1-2 1-2 2-3	PLL1 M divider Default Value: “100010” (M=34)
DPR83	1-2	Giga Port 1 interface 1-2: MII/GMII 2-3: PCS
DPR71	1-2	JTAG Pad Calibration Bypass 1-2: Normal Operation 2-3: Bypass Pad Calibration
DPR77	1-2	Core PLL Bypass 1-2: Normal Operation 2-3: Bypass the core’s PLL
DPR78 DPR72 DPR75	2-3 1-2 2-3	Core PLL Control

Table 3: PCI Configuration

JP/DPR	Default	Functionality
JP1	1-2 (3.3V)	PCI_0 Vi/o select 1-2: 3.3V 2-3: 5V
JP2	2-3 (64-bit)	PCI_1 32/64-bit select 1-2: 32-bit 2-3: 64-bit
JP3	2-3 (64-bit)	PCI_0 32/64-bit select 1-2: 32-bit 2-3: 64-bit
JP4	1-2 (3.3V)	PCI_1 Vi/o select 1-2: 3.3V 2-3: 5V
JP5	Out	PCI Arbiter DEBUG IN In: ‘0’ Out: ‘1’

Table 3: PCI Configuration (Continued)

JP/DPR	Default	Functionality
DPR9 DPR79 DPR80 DPR81 DPR84 DPR85 DPR86 DPR87	1-2 (Internal)	Internal/External PCI Arbiter 1-2: Internal 2-3: External
JP22	Out	PCI_0 Conventional 33 MHz manual select In: Select PCI_0 conventional 33 MHz Out: Disable PCI_0 conventional 33 MHz
JP23	Out	PCI_0 Conventional 66 MHz manual select In: Select PCI_0 conventional 66 MHz Out: Disable PCI_0 conventional 66 MHz
JP24	Out	PCI_0 66 MHz PCI-X manual select In: Select PCI_0 PCI-X 66 MHz Out: Disable PCI_0 PCI-X 66 MHz
JP25	Out	PCI_0 100 MHz PCI-X manual select In: Select PCI_0 PCI-X 100 MHz Out: Disable PCI_0 PCI-X 100 MHz
JP26	Out	PCI_0 133 MHz PCI-X manual select In: Select PCI_0 PCI-X 133 MHz Out: Disable PCI_0 PCI-X 133 MHz
JP27	Out	PCI_1 Conventional 33 MHz manual select In: Select PCI_1 conventional 33 MHz Out: Disable PCI_1 conventional 33 MHz
JP28	Out	PCI_1 Conventional 66 MHz manual select In: Select PCI_1 conventional 66 MHz Out: Disable PCI_1 conventional 66 MHz
JP29	Out	PCI_1 66 MHz PCI-X manual select In: Select PCI_1 PCI-X 66 MHz Out: Disable PCI_1 PCI-X 66 MHz
JP30	Out	PCI_1 100 MHz PCI-X manual select In: Select PCI_1 PCI-X 100 MHz Out: Disable PCI_1 PCI-X 100 MHz
JP31	Out	PCI_1 133 MHz PCI-X manual select In: Select PCI_1 PCI-X 133 MHz Out: Disable PCI_1 PCI-X 133 MHz

Notes

- In group JP22-JP26, only one jumper can be inserted. When all jumpers are out, the auto-detect function configures the PCI_0 bus according to the PCI specification.
- In group JP27-JP31, only one jumper can be inserted. When all jumpers are out, the auto-detect function configures the PCI_1 bus according to the PCI specification.

Table 4: PCI Interrupts from PCI to MV-Interrupt Controller

Jumper	Default	Functionality
JP6	Out	PCI_0 INT_A to MV Interrupt Controller In: Connect INT_A to MV Out: Disconnects INT_A from MV
JP7	Out	PCI_0 INT_B to MV Interrupt Controller In: Connect INT_B to MV Out: Disconnects INT_B from MV
JP8	Out	PCI_0 INT_C to MV Interrupt Controller In: Connect INT_C to MV Out: Disconnects INT_C from MV **NOTE:** Only one (JP6 or JP8) can be inserted at a time.
JP9	Out	PCI_0 INT_D to MV Interrupt Controller In: Connect INT_D to MV Out: Disconnects INT_D from MV **NOTE:** Only one (JP7 or JP9) can be inserted at a time.
JP10	Out	PCI_1 INT_A to MV Interrupt Controller In: Connect INT_A to MV Out: Disconnects INT_A from MV
JP11	Out	PCI_1 INT_B to MV Interrupt Controller In: Connect INT_B to MV Out: Disconnects INT_B from MV
JP12	Out	PCI_1 INT_C to MV Interrupt Controller In: Connect INT_C to MV Out: Disconnects INT_C from MV **NOTE:** Only one (JP6 or JP8) can be inserted at a time.
JP13	Out	PCI_1 INT_D to MV Interrupt Controller In: Connect INT_D to MV Out: Disconnects INT_D from MV **NOTE:** Only one (JP7 or JP9) can be inserted at a time.

Table 5: PCI Interrupts from MV-PCI Interface to PCI0/PCI1

Jumper	Default	Functionality
JP14	Out	PCI_0 INT_A **from** MV to PCI_0 bus. In: Drives INT_A to PCI_0 bus. Out: Disconnects INT_A from MV.

Table 5: PCI Interrupts from MV-PCI Interface to PCI0/PCI1 (Continued)

Jumper	Default	Functionality
JP15	Out	PCI_0 INT_B **from** MV to PCI_0 bus. In: Drives INT_B to PCI_0 bus. Out: Disconnects INT_B from MV.
JP16	Out	PCI_0 INT_C **from** MV to PCI_0 bus. In: Drives INT_C to PCI_0 bus. Out: Disconnects INT_C from MV.
JP17	Out	PCI_0 INT_D **from** MV to PCI_0 bus. In: Drives INT_D to PCI_0 bus. Out: Disconnects INT_D from MV.
JP18	Out	PCI_1 INT_A **from** MV to PCI_1 bus. In: Drives INT_A to PCI_1 bus. Out: Disconnects INT_A from MV.
JP19	Out	PCI_1 INT_B **from** MV to PCI_1 bus. In: Drives INT_B to PCI_1 bus. Out: Disconnects INT_B from MV.
JP20	Out	PCI_1 INT_C **from** MV to PCI_1 bus. In: Drives INT_C to PCI_1 bus. Out: Disconnects INT_C from MV.
JP21	Out	PCI_1 INT_D **from** MV to PCI_1 bus. In: Drives INT_D to PCI_1 bus. Out: Disconnects INT_D from MV.

Table 6: MPSC Devices and Boot Option Jumpers

Jumper	Default	Functionality
JP42	1-2	UART Over MPSC to Connector 1-2: RS232 9-pin 2-3: MPSC_0 Connector.
JP43	1-2	UART Source 1-2: From UART located on the device module. 2-3: From UART over MPSC.
JP39	Out	NOT Supported
JP40	Out	NOT Supported
JP41	Out	Swap Boot Flash In: Boot from 32-bit flash on the Device Module. Out: Boot from 8-bit flash on the Device Module.

Table 7: Internal Use

JP/DPR	Default	Functionality
DPR34 DPR36 DPR65 DPR68	1-2 1-2 1-2 1-2	Pad Calibration Voltage
JP35	Out	General Purpose #1 input to PAL In: '1' Out: '0'
JP36	Out	General Purpose #0 input to PAL In: '1' Out: '0'
JP37	1-2 (CPU_VCC_IO)	Clock to CPU Voltage. 1-2: Depends on CPU_VCC_IO 2-3: 2.5V

Table 8: TWSI

JP/DPR	Default	Functionality
JP32	2-3 (normal)	TWSI Write Protect 1-2: Write Protect 2-3: Normal Operation
JP38	1-2 (Disable)	TWSI Support 1-2: Disable. 2-3: Enable. (Only if using Single/Double MPC7450 CPUs).
DPR90 DPR89 DPR88	1-2 1-2 1-2	TWSI Address

Table 9: Related CPU Configuration

DPR	Default	Functionality
DPR41 DPR21 DPR50 DPR64 DPR20 DPR11	1-2 (Internal)	Internal/External CPU Arbiter 1-2: Internal 2-3: External
JP45	MIPS: 2-3 PPC: 1-2	MIPS: 1-2: Little Endian 2-3: Big Endian PPC: 1-2: Internal Arbiter 2-3: External Arbiter

Table 9: Related CPU Configuration (Continued)

DPR	Default	Functionality
DPR65	2-3	Multi MV Socket Selection 1-2: Socket#1 2-3: Socket#0

Table 10: Connectors for a PC ATX-Case

Jumper	Default	Functionality
JP46	1-2	Power Up source 1-2: On/off swtich or JP48 (ATX switch button). 2-3: ATX push button.
JP44	Out	External ATX push button.
JP33	Out	External ATX reset.
JP48	Out	External ATX switch button.
JP49	Out	External Flash Busy Indication
JP50	Out	External Speaker Connector

4.2 Multi-Purpose Pins (MPPs)

The DB-64340/60-BP has 32 MPPs. Table 11 details the default MPP configuration (in the default column) that is shipped with the DB-64340/60-BP and supported by the DINK32 monitor and the VxWorks Operating System. The other columns detail additional options for the MPPs. These options are for internal use only.

Warning

Changing the configuration of the MPPs in the software (via the MPP registers) or changing the hardware connection on the board (via the jumpers) may cause the board to stop functioning. See the comments column for more details.

Table 11: Multi-Purpose Pins

MPP #	Default	Multiplexed #1	Multiplexed #2	Multiplexed #3	Comments
MPP0	TxD0				
MPP1	RxD0				
MPP2	RTS0				
MPP3	CTS0				
MPP4	CD0				

Table 11: Multi-Purpose Pins (Continued)

MPP #	Default	Multiplexed #1	Multiplexed #2	Multiplexed #3	Comments
MPP5	SCLK0				
MPP6	TSCLK0				
MPP7	GPIO[7] – G0_Int Interrupt from PHY_0 DPR58 1-2	CTS1 DPR58 2-3			When MPSC_1 is working with its full protocol (not only RXD and TXD), PCI_1 Device7 and both interrupts driven from the PHYs will not be functional.
MPP8	GNT1[4] – grant from PCI internal arbiter to PCI_1 device 7. DPR54 1-2	CD1 DPR54 2-3			
MPP9	REQ1[4] – request from PCI_1 device 7 to PCI internal arbiter. DPR63 1-2	SCLK1 DPR63 2-3			
MPP10	GPIO[10] – G1_Int Interrupt from PHY_1 DPR59 1-2	TSCLK1 DPR59 2-3			
MPP11	RXD1				
MPP12	TXD1				
MPP13	RTS1				
MPP14	GNT1[1]] – grant from PCI internal arbiter to PCI_1 device 8.				These MPPs are for PCI_1 Device8 internal Arbiter control. Changing the default setting will cause PCI_1 Device8 to be non-functional.
MPP15	REQ1[1]] – request from PCI_1 device 8 to PCI internal arbiter.				

Table 11: Multi-Purpose Pins (Continued)

MPP #	Default	Multiplexed #1	Multiplexed #2	Multiplexed #3	Comments
MPP16	GNT0[0]] – grant from PCI internal arbiter to PCI_0 device 7.				These MPPs are for PCI_0 Device7 and Device8 internal Arbiter control. Changing the default setting will cause PCI_0 Device7 and Device8 to be non-functional.
MPP17	REQ0[0]] – request from PCI_0 device 7 to PCI internal arbiter.				
MPP18	GNT0[1]] – grant from PCI internal arbiter to PCI_0 device 8.				
MPP19	REQ0[1]] – request from PCI_0 device 8 to PCI internal arbiter.				
MPP20	InitAck				Both default settings are essential for I^2C Boot and must not be changed.
MPP21	BclkIn				
MPP22	GPIO[22] – RS232B interrupt. DPR61 1-2	DmrEQ3 DPR61 2-3			These multiple options are used for System Validation (SV) tests. Check the main PAL equations for more details on these tests.
MPP23	BclkOut DPR62 1-2 DPR18 1-2	TBEN DPR62 1-2 DPR18 2-3 DPR60 1-2	DMAAck3 DPR62 2-3	EOT0 DPR62 1-2 DPR18 2-3 DPR60 2-3	
MPP24	WDNMI				
MPP25	WDE	TCTcnt0			These multiple options are used for System Validation (SV) tests. Check the main PAL equations for more details on these tests.
MPP26	GPIO[26] – TP21 optional TP DPR67 1-2	TCEn1 DPR67 2-3			
MPP27	GPIO[27] – RS232A				

Table 11: Multi-Purpose Pins (Continued)

MPP #	Default	Multiplexed #1	Multiplexed #2	Multiplexed #3	Comments
MPP28	GPIO[28] – PCI1 B,D interrupts				
MPP29	GPIO[29] – PCI1 A,C interrupts				
MPP30	GPIO[30] – PCI0 B,D interrupts				
MPP31	GPIO[31] – PCI1 A,C interrupts				

4.3 Indication and Warning LEDs

Table 12 provides a list of LEDs, their functionality and when they are lit.

Table 12: Indication and Warning LEDs

LED	Functionality	Lit When
LED 21	HSTL Mode Indication	CPU interface is configured to HSTL mode.
LED 20	Multi-MV Mode Indication	MV64340/60A is configured to Multi-MV mode.
LED 19	MPX Bus Indication	CPU interface is configured to MPX bus mode.
LED 16	PCI External Arbiter Disabled	Working with the enabled MV64340/60A PCI internal arbiter.
LED 22	CPU's V I/O differential	Working with dual CPUs and each CPU requires a different CPU VI/O.
LED 23	CPU's bus type differential	Working with dual CPUs and each CPU is configured to a different bus type. For example, CPU0 is configured to 60x and CPU1 is configured to MPX.

Warning

When either LED 22 or 23 is lit, turn the power off immediately.

4.4 PCI Auto-Detect

The DB-64340/60-BP supports the PCI auto-detect feature. This mechanism is implemented according to the PCI-X specification, Rev. 1.0, Chapter 6.2 and Appendix E (Detection of PCI-X Add-in and capability.)

Each PCI interface has five LEDs and five respective jumpers.

- PCI Conventional 33 MHz
- PCI Conventional 66 MHz
- PCI-X 66 MHz
- PCI-X 100 MHz
- PCI-X 133 MHz

When one of the jumpers is inserted, the mode is set manually. The Auto-Detect feature is enabled when all five jumpers are "out".

4.5 System Memory (DIMM)

The DB-64340/60-BP only uses DDR (Double Data Rate) Dual Inline Memory Modules (DIMMs). Two sockets are available for 2.5 V power level unbuffered or registered DDR-Synchronous Dynamic Random Access Memory DDR (SDRAM) of 64, 128, 256, 512, or 1024 Mb.

Notes

- Only use DDR-SDRAMs that are compatible with the current PC266 DDR-SDRAM specification.
- Do not mix registered DDR-SDRAMs with unbuffered ones.
- When using registered DDR-SDRAM, configure the MV64340/360 prior to the CPU access of the DDR-SDRAM.
- When using two memory modules, install the larger module in CON17.

4.6 CPU Module

The DB-64340/60-BP provides two SOCKET-7 connectors for two CPU modules which are installed on the board. There are two power module connectors which provide each socket with the CPU's internal voltage.

Warning

Do not remove the CPU modules from the board. Doing so may cause damage to the board and/ or the modules. Marvell takes no responsibility for damage caused to the boards or the modules if you do not heed this warning.

Note

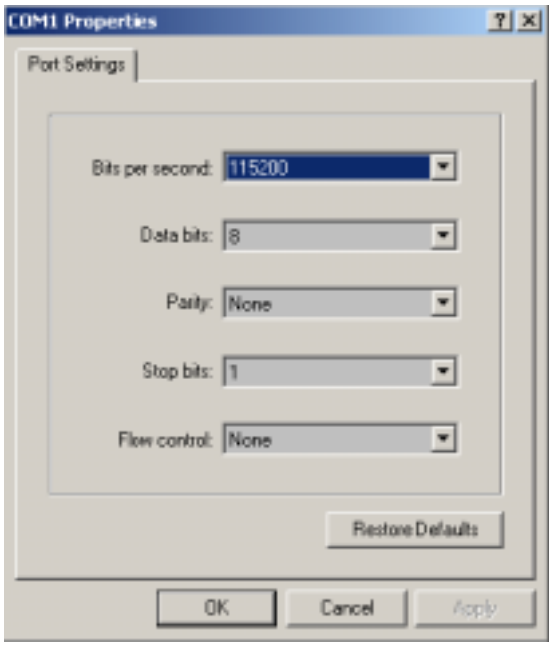
When one or both sockets are populated with a CPU module, the power module must be connected. Do not power up the system unless the power module is connected.

4.7 Applying Power to the DB-64340/60-BP

The DB-64340/60-BP uses a hyperterminal for communication with the system. You need an RS232 cable and a PC which runs a hyperterminal application.Take the following steps to apply power to the board:

1. Make sure that all power switches are off.
2. Connect the power supply cord connector to the ATX header on the board.
3. Connect the RS232 cable to the COM1 port on the DB-64340/60-BP and to the PC's COM port.
4. Open the hyperterminal window. You will see a File Menu on your PC screen.
5. From the File menu, select File|Properties.
6. In the Properties dialog box, click Configure, and confirm that the displayed parameters match the parameters in Figure 3.
7. Click OK.
8. From the File Menu, Choose File. Follow the instructions below.
9. The CPU fan can be connected to the system in one of the following two options:
   - Connect the CPU fan to the ATX power supply connector.
   - Connect the CPU fan to the on-board CPU fan connector.

Figure 3: COM1 Properties Dialog Box



10. Turn on the power. The operating system's logo appears in the Main window. The power LEDs on the DB-64340/60-BP turn on. If, for some reason, one of LEDs does not turn on immediately, turn the power off. When the unit powers up, LED0, LED1, and LED2 light up in order. This is an indication that the monitor was fired up properly. Afterwards, these LEDs turn off. The system is now ready for operation.

Section 5. Software

The DB-64340/60-BP is shipped with DINK 32 Operating System (PPC)/PMON operating system (MIPS). PMON was originally released by Algorithmics. Marvell has ported the PMON Operating System software so that it complies with the DB-64340/60-BP. It has many useful commands as well as a simple flash file system. You can download software to the DB-64340/60-BP via the hyperterminal or by using one of the Ethernet ports in conjunction with various application provided by Marvell.

Notes

- The commands will be listed in the PMON manual in the near future.
- The VxWorks Board Support Package is shipped with the IBM CPUs.

5.1 MV64340/360 Drivers

To ease the process of software development, Marvell is in the process of developing low-level drivers for the DB-64340/60-BP. These will be available in the near future.

Section 6. Revision History

Table 13: Revision History

Document Type	Rev. #	Date	Comments
First Release	Rev. A	May 20, 2002	
	Rev. B	June 26, 2002	1. Updated photograph in Figure 1. 2. Updated the following tables: Table 1, Table 2, Table 3, Table 6 and Tables 7-12. 3. Added Section 4.3 and Section 4.4.
	Rev. C	July 15,2002	Added the following warning in Section 1.2 and Section 4.6: "Do not remove the CPU modules from the board. Doing so may cause damage to the board and/or the modules. Marvell takes no responsibility for damage caused to the boards or the modules if you do not heed this warning."
	Rev. D	June 25, 2003	1. Added an additional CPU fan connection option in Section 4.7 Step 9. 2. Updated Disclaimer 3. Replaced I^2C with TWSI. 4. Picture Replaced

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