DB-MV64340A/60A-BP Schematic

Revision 2.1 18/06/2002

Table of Contents:

Changes from Rev. 0.9:

1. Sheet: "MV64340_60_POWER"

DRAM_ACAL and DRAM_DCAL Balls have a separate DPR. DPR175 was added. (Connection to 2.5V or GND).

2. Sheet: "MV64340_60_POWER"

DPRs: 165,166,167: Value changed from 4.7Kohm to 0 ohm.

3. Sheet: "CPU_MODULE":

DPR176 was added in order to give the option to select the socket, which will configure for Multi-MV mode.

4. Sheets: "PCI_CONFIG", "MV_INITIALIZATION":

- Implementing a warning LED for different Vi/o requirement for the two CPU modules.
- Implementing a warning LED for different CPU bus configuration by the two CPU modules (60X and MAX bus for example).

If any of the two warning LEDs is on, the board should be turned of immediately.

5. Sheets: "CPU_MODULE_0", "CPU_MODULE_1":

The connectors were fixed due to polarity signal mistakes.

6. Sheet: "MV_INITIALIZATION":

- The Text was changed with accordance to the updated D.S.
- Led41 (PCI External Arbiter Disabled) – The polarity has been changed meaning: the led lit when the External Arbiter is disabled. LEDs 38,39 were mistakenly connected *in the opposite direction*.

- Sample of P1_AD[56] (DPR164 in Rev 0.1) was removed.

7. Sheet: "2_MPSC_CONNECTORS_UART":

CON-1 D-type 9 connector was placed wrong.

8. Sheet: "DEVICE_MODULE":

Pins 75,89 in U12 (Main Pal) were switched.

9. Sheet: "CLOCKS":

- U-29 and U-31 had a wrong connection to the OE pin.

- SSTL clock Buffer U-26 and HSTL clock Buffer U-28 required a special filtering for the AVDD taken from ICST up note.

- HSTL clock Buffer U-28 pin7 is left unconnected.

- HSTL and SSTL clocks were mistakenly given same name.
  HSTL clocks:
  H_CK0, H_CK0~, H_CK1, H_CK1~, H_CK2, H_CK2~, H_CK3, H_CK3~
  SSTL clocks:
  S_CK0, S_CK0~, S_CK1, S_CK1~, S_CK2, S_CK2~, S_CK3, S_CK3~, S_CK4, S_CK4~, S_CK5, S_CK5~

- PCI0,PCI1 PLLs (U30,U32) output pins 7,8 (CLK,CLK/2) were switched.

- PLL filtering (PAVDD) was added to U26 (SSTL Clock Buffer) and U28 (HSTL Clock Buffer) according to ICST up note.

10. Sheet "2_MPSC_CONNECTORS_UART":

R196 was added – READ_ID~ require a pull up.

Changes from Rev. 1.0:

1. Sheet: "CLOCKS"

3 filtering capacitors were missing in SYS_CLK clock buffer (U-39) in pins: 5,6 to GND, 23,24 to GND and pin 15 to GND. (All 3 capacitors Values are 100nF).

2. Sheet: ""DEVICE_MODULE""

On Board EPROM (U-22) and on Board flash EPROM (U-19) were removed, in order to place SSTL VTT plane as close as possible to the DDR Dimms. Both Boot Devices are covered by the Device Module, which includes both Boots option.

3. Sheet: "DDR_DIMMs":

Dimms location has been swapped between their selves: CON11 CS_0/1 – primary Dimm (The socket which is closer to the MV64340/60A) is now wired to CS_2/3 and CON12 - secondary dimm (The socket which far from the MV64340/60A) is now wired to CS_0/1 and became primary Dimm. The I2C addresses were also switched in order to sustain software compatible between the two revisions. This change has been made in order to support the DDR Dimm Test Point.

4. Sheet: "MV 64340_60_PCI":

Both PCI External arbiter signals: P0_GNT_GT~ and P1_GNT_GT~ were replaced from pull-ups to pull-downs. When working with PCI internal arbiter (No external arbiter is locate on board) the software must initial the internal arbiter. Until the software is enabling the internal arbiter no agent is parked on either PCI_0 or PCI_1 buses. The pull-downs will guarantee that till initialization completes the MV64340/60A will be parked on both Buses.

5. Sheet: “PCI_CONFIGURATION ” + added new SHEET: “DIFFERENTIAL_AMPLIFIERS”

- The PCI auto-detect implementation had some problems with the differential amplifiers. A new design which uses hysterezis- TBD has been implemented using another quad differential amplifier, and the PCI-detect pal equations have been also changed. (The equations for the PCI-DETECT PAL has been changed)
- The VI/O conflict differential amplifiers had the same problem as the PCI-DETECT amplifiers had. A new design, which uses hysterezis, has been implemented. (The equations for the PCI-DETECT PAL has been changed)

6. Sheet: “FILTERING_CAPACITORS”:

More 100nF compensation capacitors were added between VDDQ (2.5V) to GND to the VDDQ supply balls of the MV64340/60A.

7. Sheets: “HSTL_SSTL_SUPPLY”,“DDR_TERMINATIONS”:

The following sections regarding the SSTL VTT changes:

- The SSTL VVT & VREF DC2DC circuit was removed from the PCI location to the back of the DDRs Dimm location (instead of the EPROMs mention in section 2). – Layout change.
- A new SSTL VTT plane has created which will be as little as possible and will connect all SSTL signals through 60-Ohm termination. A new RNETs were placed instead the formers RNETs.
- 3 (additional 2 vs. REV.1) Low ESR capacitors will be located On both new SSTL VTT plane, these capacitors are needed for compensation purpose.
- Additional 3-10uF, 4-100nF and 4-100pF capacitors, which will be placed, equally on the SSTL VTT plane. These capacitors are for filtering.
- For each 2 parallel terminations place as close as possible to the resistors a 100nF capacitor to GND and another 100nF capacitor to VDDQ (2.5V) – new Cnets.
- A serial resistors were placed between the MV64340/60A to the DDR Dimms for the signals: DQ[63..0] and CB[7..0] in order reduce SSO in the MV64340/60A – will be Assembled with 0-Ohm value.

8. Sheets: “DDR_DIMMs”, “MV 64340_60_DDR”:

In REV-1 the SSTL-VREF to both MV64340/60A balls (D-24,E-10) and to both DDR Dimm pin-1 was taken from the SSTL DC2DC circuit (U-33). In REV-1.9 we used a simple voltage divider with capacitor for the 4 consumers (2-balls dimms).

9. Sheet: DDR_DIMMs”:

The two pairs: startBurstIn-StartBurstOut and – feedBackClockOut will have a parallel termination (60-Ohm) to VTT and will be routed with a clreansses of 20mil from other signals and between them selves.

Changes from Rev. 1.9:

1. Sheets: “CPU_MODULE_0”, “CPU_MODULE_1”

The SVTT (SSTL VTT) which connected to pin AL33 on both sockets is now connected only to CPU_0 socket and to pins: A5,B4 and C5.

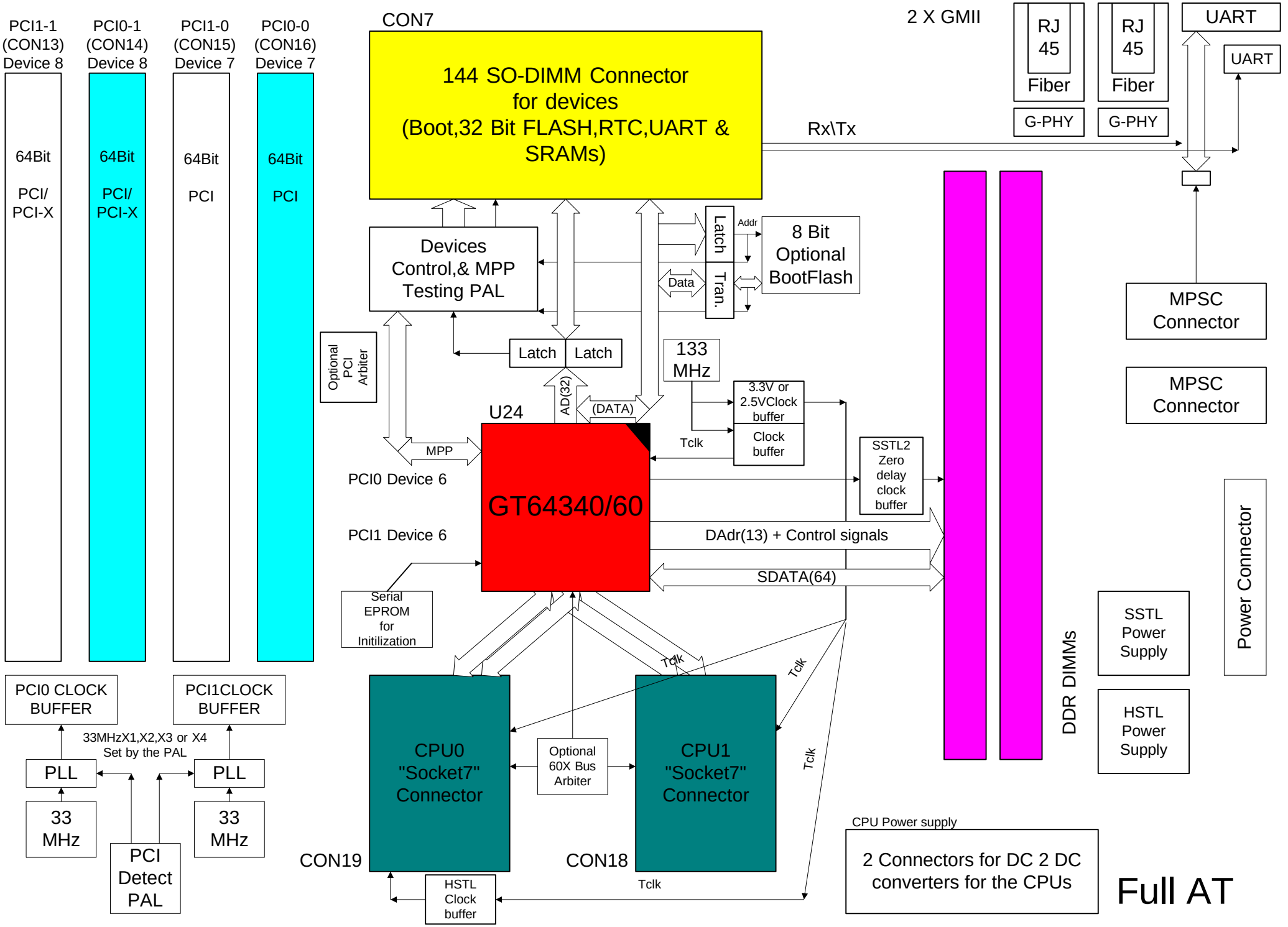
2. All Sheets

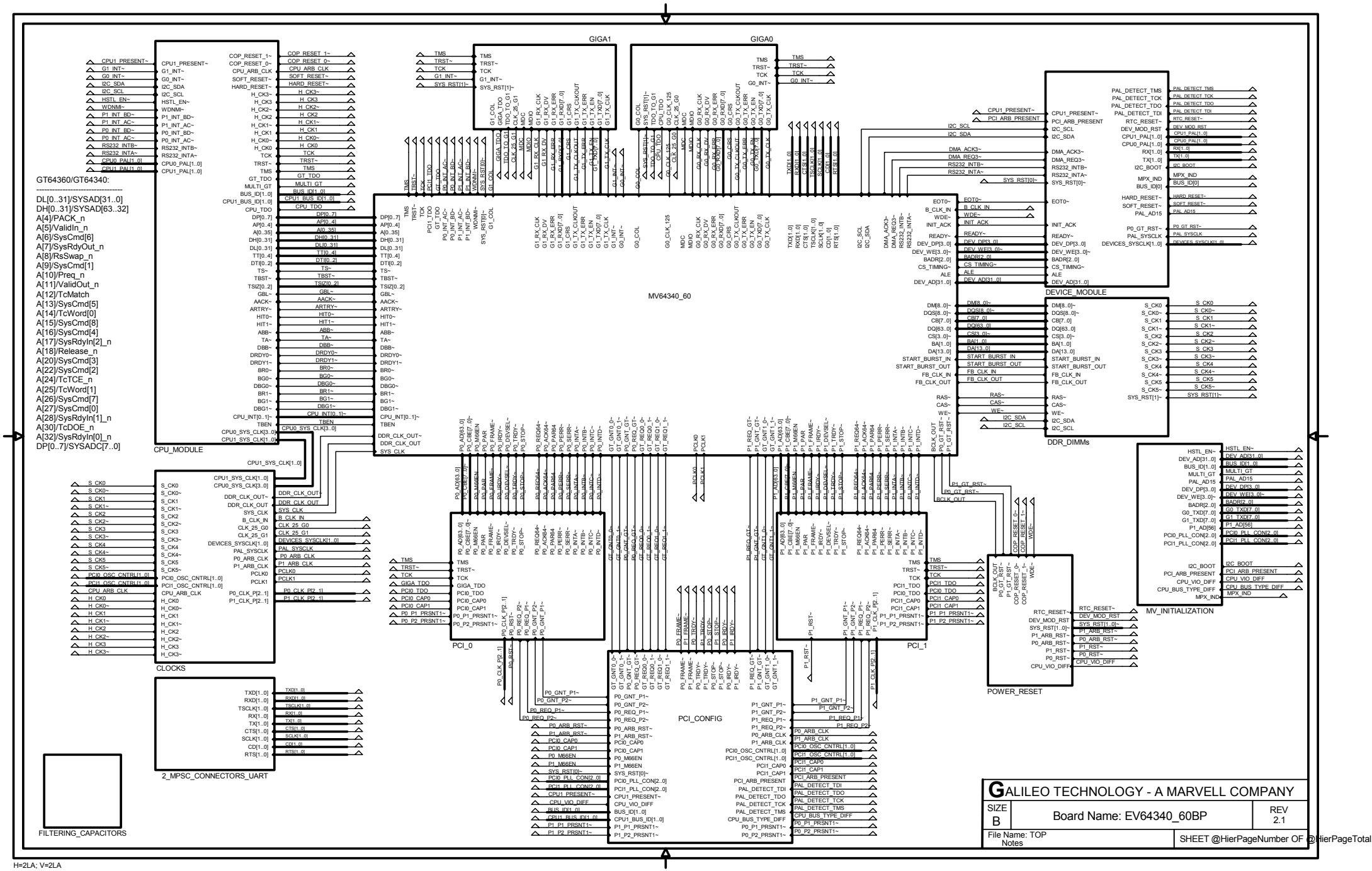
The REF Designators has been changed in all parts.

Changes from Rev. 2.0:

1. Sheets: “CPU_MODULE_0”

All HSTL clock (only for the RM7000C CPU) must have a termination of 50 ohm to GND, according to ICS8624 (HSTL clock buffer) Note.
8 resistors were placed at the CPU_SOCKET0 (CON-13) pins: A33,B34,D36,E37,E35,F36,C33 and D34.


PCI1-1 (CON13) Device 8
PCI0-1 (CON14) Device 8
PCI1-0 (CON15) Device 7
PCI0-0 (CON16) Device 7
64Bit PCI/ PCI-X
64Bit PCI/ PCI-X
64Bit PCI
64Bit PCI
CON7
144 SO-DIMM Connector for devices (Boot,32 Bit FLASH,RTC,UART & SRAMs)
2 X GMII
RJ 45
Fiber
RJ 45
Fiber
G-PHY
G-PHY
UART
UART
Rx\Tx
Devices Control,& MPP Testing PAL
Latch
Addr
Data
Tran.
8 Bit Optional BootFlash
MPSC Connector
MPSC Connector
Optional PCI Arbiter
Latch
Latch
133 MHz
AD(32)
(DATA)
U24
3.3V or 2.5VClock buffer
Clock buffer
Tclk
MPP
PCI0 Device 6
PCI1 Device 6
GT64340/60
SSTL2 Zero delay clock buffer
DAdr(13) + Control signals
SDATA(64)
Serial EPROM for Initilization
DDR DIMMs
SSTL Power Supply
HSTL Power Supply
Power Connector
PCI0 CLOCK BUFFER
PCI1CLOCK BUFFER
33MHzX1,X2,X3 or X4 Set by the PAL
PLL
PLL
33 MHz
33 MHz
PCI Detect PAL
CPU0 "Socket7" Connector
Optional 60X Bus Arbiter
CPU1 "Socket7" Connector
CON19
CON18
Tclk
Tclk
Tclk
Tclk
HSTL Clock buffer
CPU Power supply
2 Connectors for DC 2 DC converters for the CPUs
Full AT


GT64360/GT64340:
DL[0..31]/SYSAD[31..0]
DH[0..31]/SYSAD[63..32]
A[4]/PACK_n
A[5]/ValidIn_n
A[6]/SysCmd[6]
A[7]/SysRdyOut_n
A[8]/RsSwap_n
A[9]/SysCmd[1]
A[10]/Preq_n
A[11]/ValidOut_n
A[12]/TcMatch
A[13]/SysCmd[5]
A[14]/TcWord[0]
A[15]/SysCmd[8]
A[16]/SysCmd[4]
A[17]/SysRdyIn[2]_n
A[18]/Release_n
A[20]/SysCmd[3]
A[22]/SysCmd[2]
A[24]/TcTCE_n
A[25]/TcWord[1]
A[26]/SysCmd[7]
A[27]/SysCmd[0]
A[28]/SysRdyIn[1]_n
A[30]/TcDOE_n
A[32]/SysRdyIn[0]_n
DP[0..7]/SYSADC[7..0]
CPU_MODULE
GIGA1
GIGA0
MV64340_60
DEVICE_MODULE
DDR_DIMMs
CLOCKS
PCI_0
PCI_1
PCI_CONFIG
MV_INITIALIZATION
POWER_RESET
2_MPSC_CONNECTORS_UART
FILTERING_CAPACITORS
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
Board Name: EV64340_60BP
REV 2.1
File Name: TOP
Notes
SHEET @HierPageNumber OF @HierPageTotal
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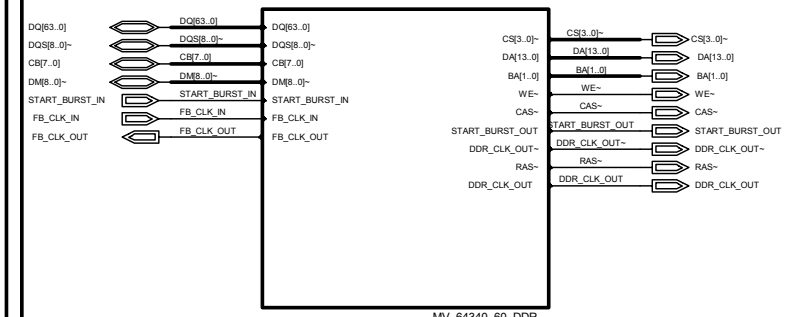

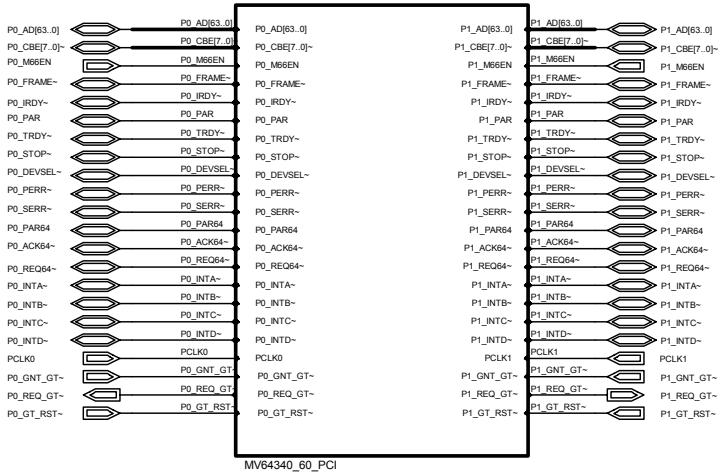

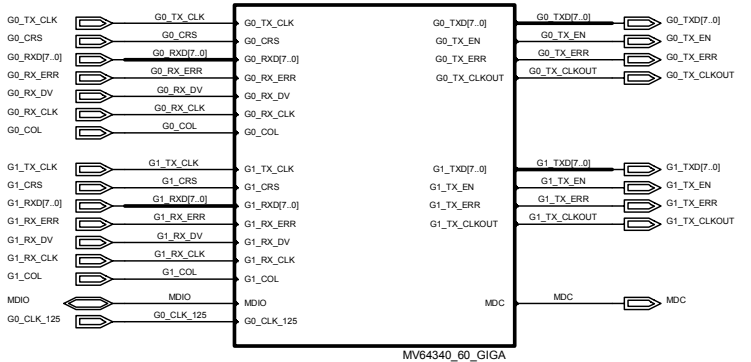

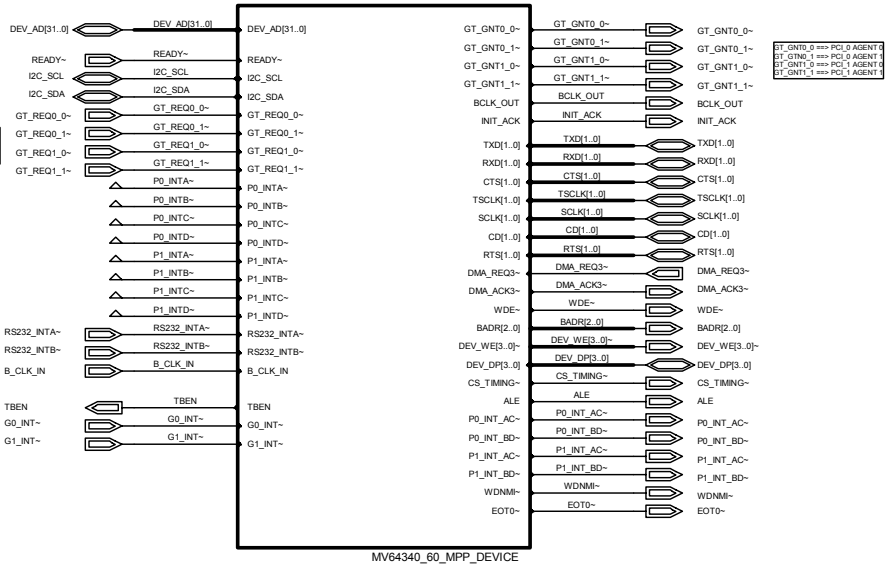

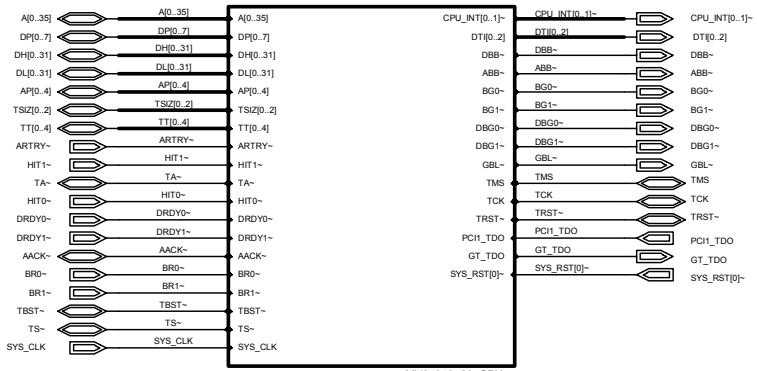

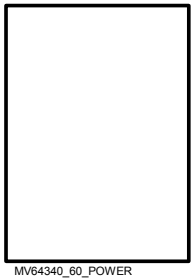

GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	Board Name: EV64340_60BP	REV 2.1
File Name: MV64340_60 Notes	SHEET @HierPageNumber OF @HierPageTotal	

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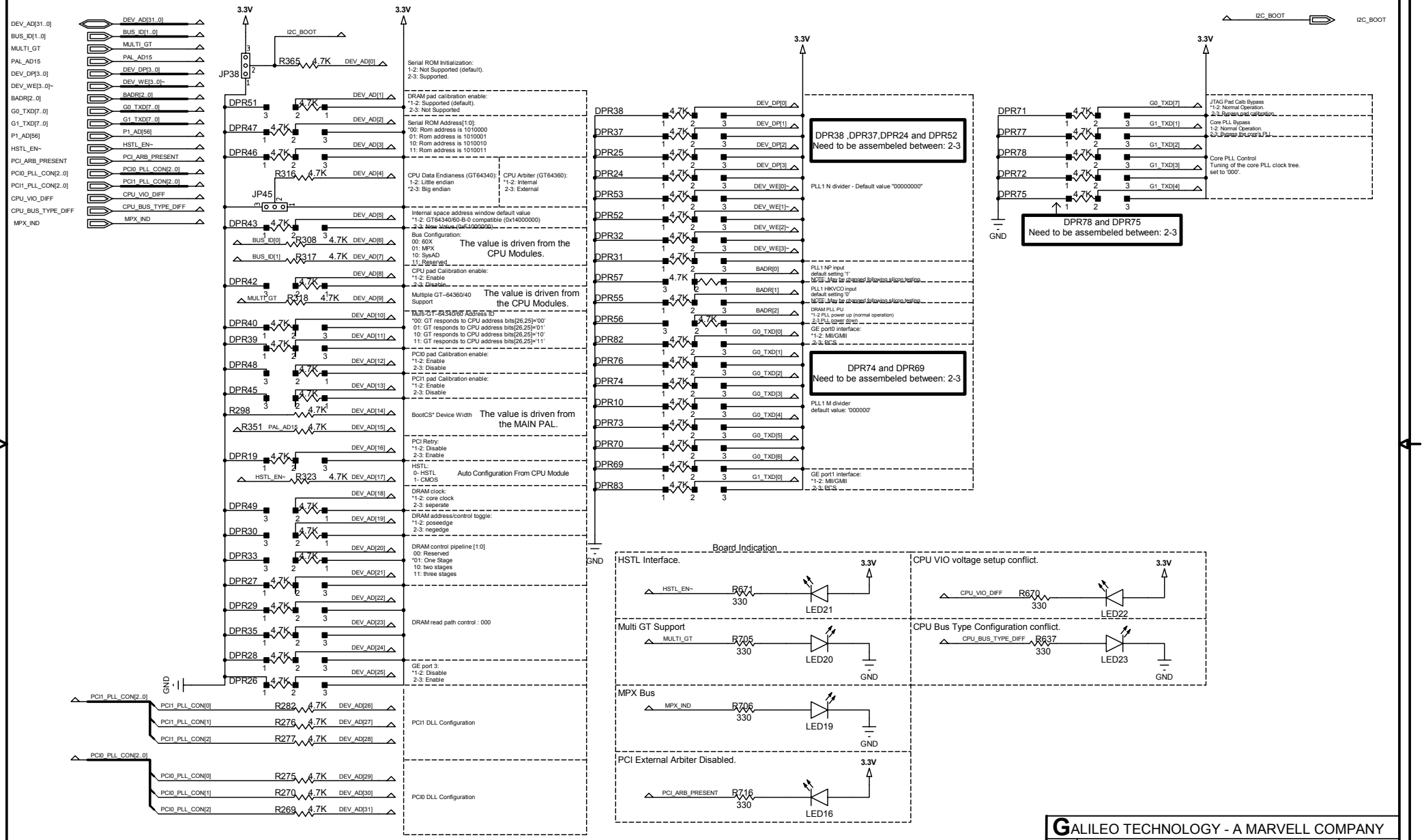
DEV_AD[31..0]
BUS_ID[1..0]
MULTI_GT
PAL_AD15
DEV_DP[3..0]
DEV_WE[3..0]~
BADR[2..0]
G0_TXD[7..0]
G1_TXD[7..0]
P1_AD[56]
HSTL_EN~
PCI_ARB_PRESENT
PCI0_PLL_CON[2..0]
PCI1_PLL_CON[2..0]
CPU_VIO_DIFF
CPU_BUS_TYPE_DIFF
MPX_IND
I2C_BOOT
3.3V
GND
JP38
R365 4.7K
JP45
Serial ROM Initialization:
1-2: Not Supported (default).
2-3: Supported.
DRAM pad calibration enable:
*1-2: Supported (default).
2-3: Not Supported
Serial ROM Address[1:0]:
*00: Rom address is 1010000
01: Rom address is 1010001
10: Rom address is 1010010
11: Rom address is 1010011
CPU Data Endianess (GT64340):
1-2: Little endian
*2-3: Big endian
CPU Arbiter (GT64360):
*1-2: Internal
2-3: External
Internal space address window default value
*1-2: GT64340/60-B-0 compatible (0x14000000)
2-3: New Values (0xf1000000)
Bus Configuration:
00: 60X
01: MPX
10: SysAD
11: Reserved
The value is driven from the CPU Modules.
CPU pad Calibration enable:
*1-2: Enable
2-3: Disable
Multiple GT–64360/40 Support
The value is driven from the CPU Modules.
Multi GT–64340/60 Address ID:
*00: GT responds to CPU address bits[26,25]='00'
01: GT responds to CPU address bits[26,25]='01'
10: GT responds to CPU address bits[26,25]='10'
11: GT responds to CPU address bits[26,25]='11'
PCI0 pad Calibration enable:
*1-2: Enable
2-3: Disable
PCI1 pad Calibration enable:
*1-2: Enable
2-3: Disable
BootCS* Device Width
The value is driven from the MAIN PAL.
PCI Retry:
*1-2: Disable
2-3: Enable
HSTL:
0- HSTL
1- CMOS
Auto Configuration From CPU Module
DRAM clock:
*1-2: core clock
2-3: seperate
DRAM address/control toggle:
*1-2: posedge
2-3: negedge
DRAM control pipeline [1:0]
00: Reserved
*01: One Stage
10: two stages
11: three stages
DRAM read path control : 000
GE port 3:
*1-2: Disable
2-3: Enable
PCI1 DLL Configuration
PCI0 DLL Configuration
DPR38 ,DPR37,DPR24 and DPR52
Need to be assembeled between: 2-3
PLL1 N divider - Default value "00000000"
PLL1 NP input
default setting "1"
NOTE: May be changed following silicon testing
PLL1 HIKVCO input
default setting '0'
NOTE: May be changed following silicon testing
DRAM PLL PU
*1-2 PLL power up (normal operation)
2-3 PLL power down
GE port0 interface:
*1-2: MII/GMII
2-3: RGS
DPR74 and DPR69
Need to be assembeled between: 2-3
PLL1 M divider
default value: '000000'
GE port1 interface:
*1-2: MII/GMII
2-3: RGS
DPR78 and DPR75
Need to be assembeled between: 2-3
JTAG Pad Calb Bypass
*1-2: Normal Operation.
2-3: Bypass pad calibration.
Core PLL Bypass
1-2: Normal Operation.
*2-3: Bypass the core's PLL
Core PLL Control
Tuning of the core PLL clock tree.
set to '000'.
Board Indication
HSTL Interface.
LED21
CPU VIO voltage setup conflict.
LED22
Multi GT Support
LED20
CPU Bus Type Configuration conflict.
LED23
MPX Bus
LED19
PCI External Arbiter Disabled.
LED16
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
File Name: MV_INITIALIZATION
Notes
REV 2.1
Board Name: EV64340_60BP
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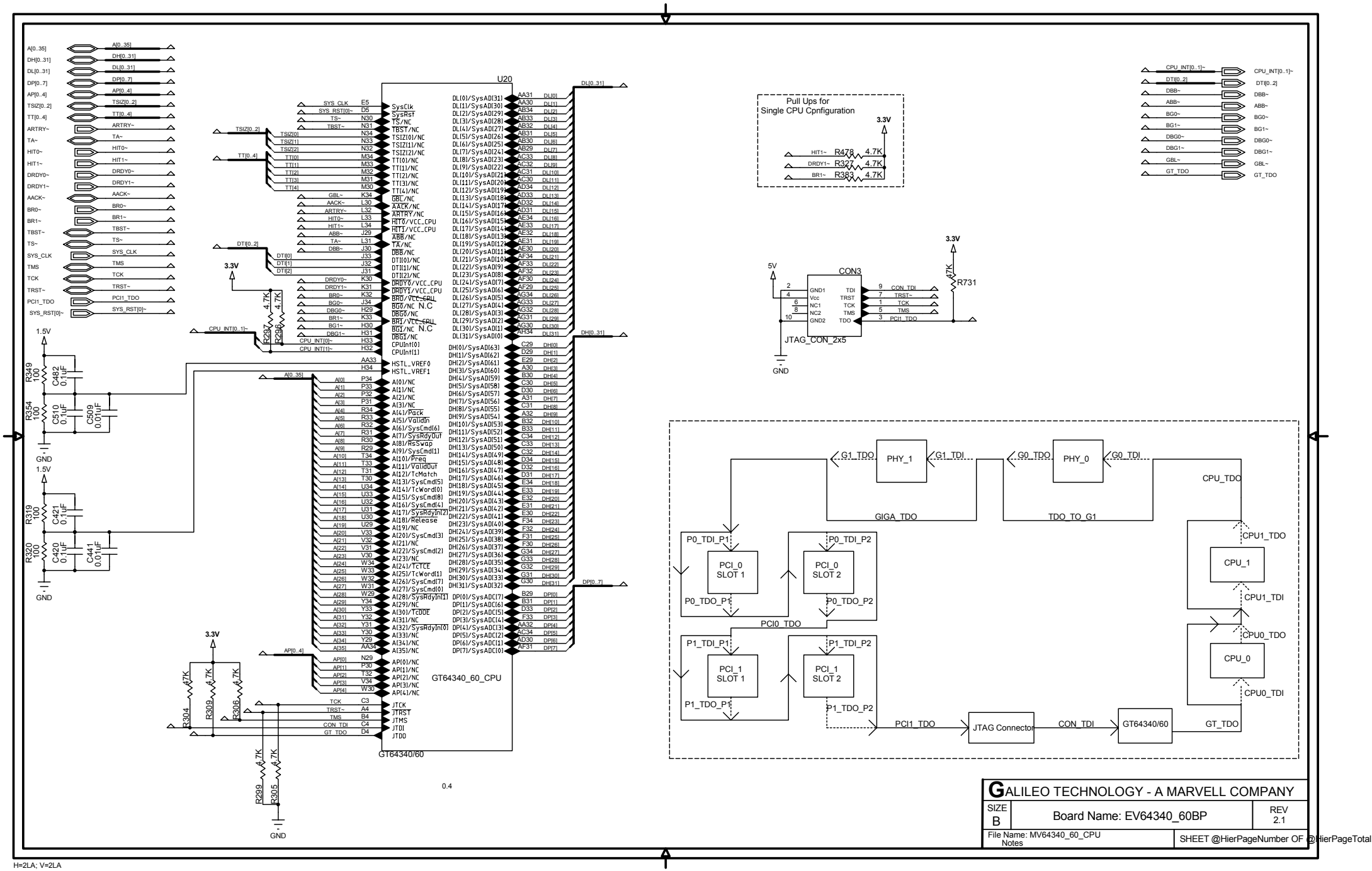
U20
GT64340_60_CPU
GT64340/60
Pull Ups for
Single CPU Cpnfiguration
3.3V
HIT1~ R478 4.7K
DRDY1~ R327 4.7K
BR1~ R383 4.7K
CON3
JTAG_CON_2x5
R731
5V
GND
PHY_1
PHY_0
G1_TDO
G1_TDI
G0_TDO
G0_TDI
GIGA_TDO
TDO_TO_G1
CPU_TDO
P0_TDI_P1
P0_TDI_P2
PCI_0 SLOT 1
PCI_0 SLOT 2
P0_TDO_P1
P0_TDO_P2
PCI0_TDO
P1_TDI_P1
P1_TDI_P2
PCI_1 SLOT 1
PCI_1 SLOT 2
P1_TDO_P1
P1_TDO_P2
PCI1_TDO
JTAG Connector
CON_TDI
GT64340/60
GT_TDO
CPU1_TDO
CPU_1
CPU1_TDI
CPU0_TDO
CPU_0
CPU0_TDI
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SIZE B
Board Name: EV64340_60BP
REV 2.1
File Name: MV64340_60_CPU
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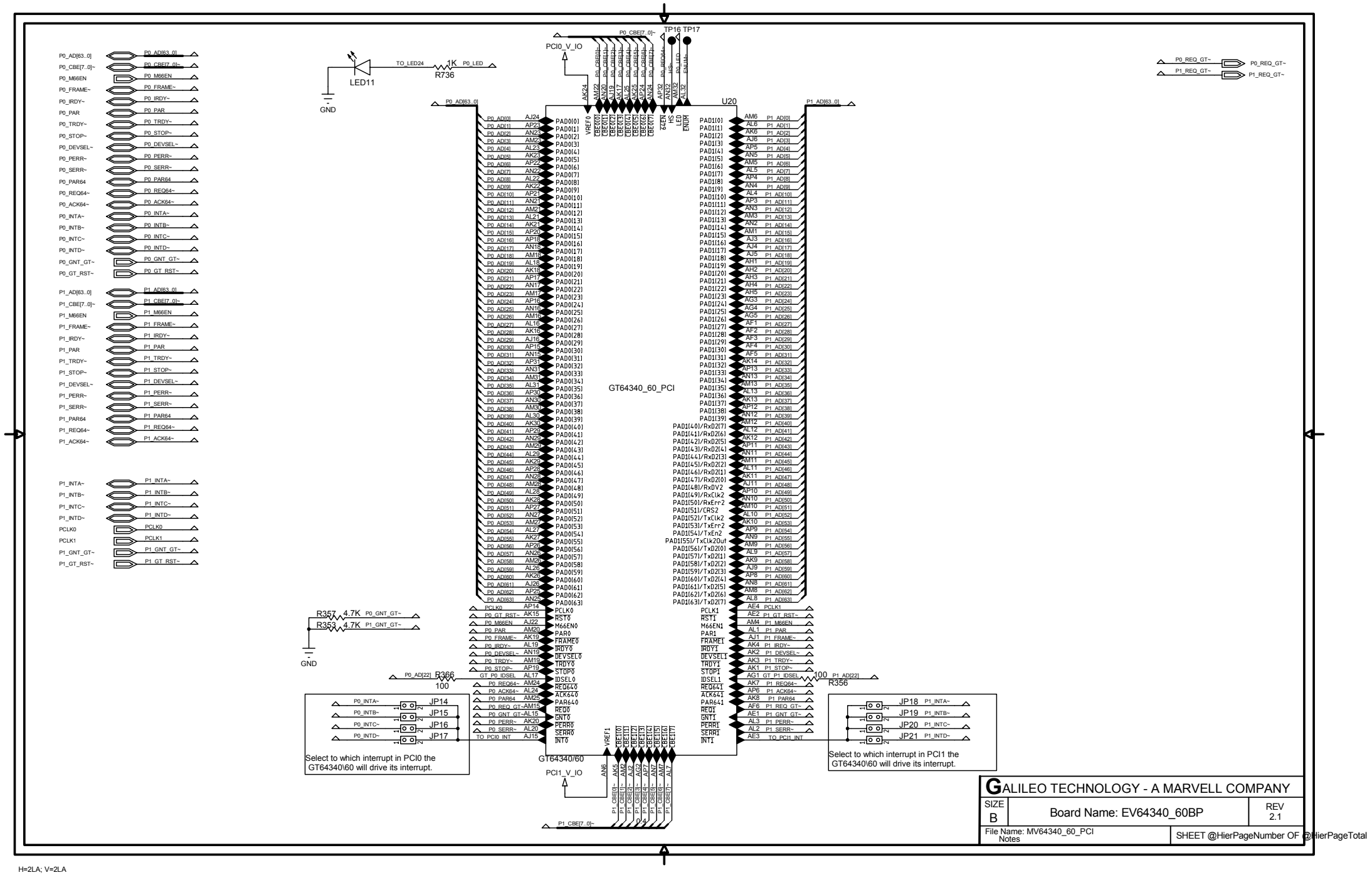

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SIZE B	Board Name: EV64340_60BP		REV 2.1
File Name: MV64340_60_PCI Notes		SHEET @HierPageNumber OF @HierPageTotal	

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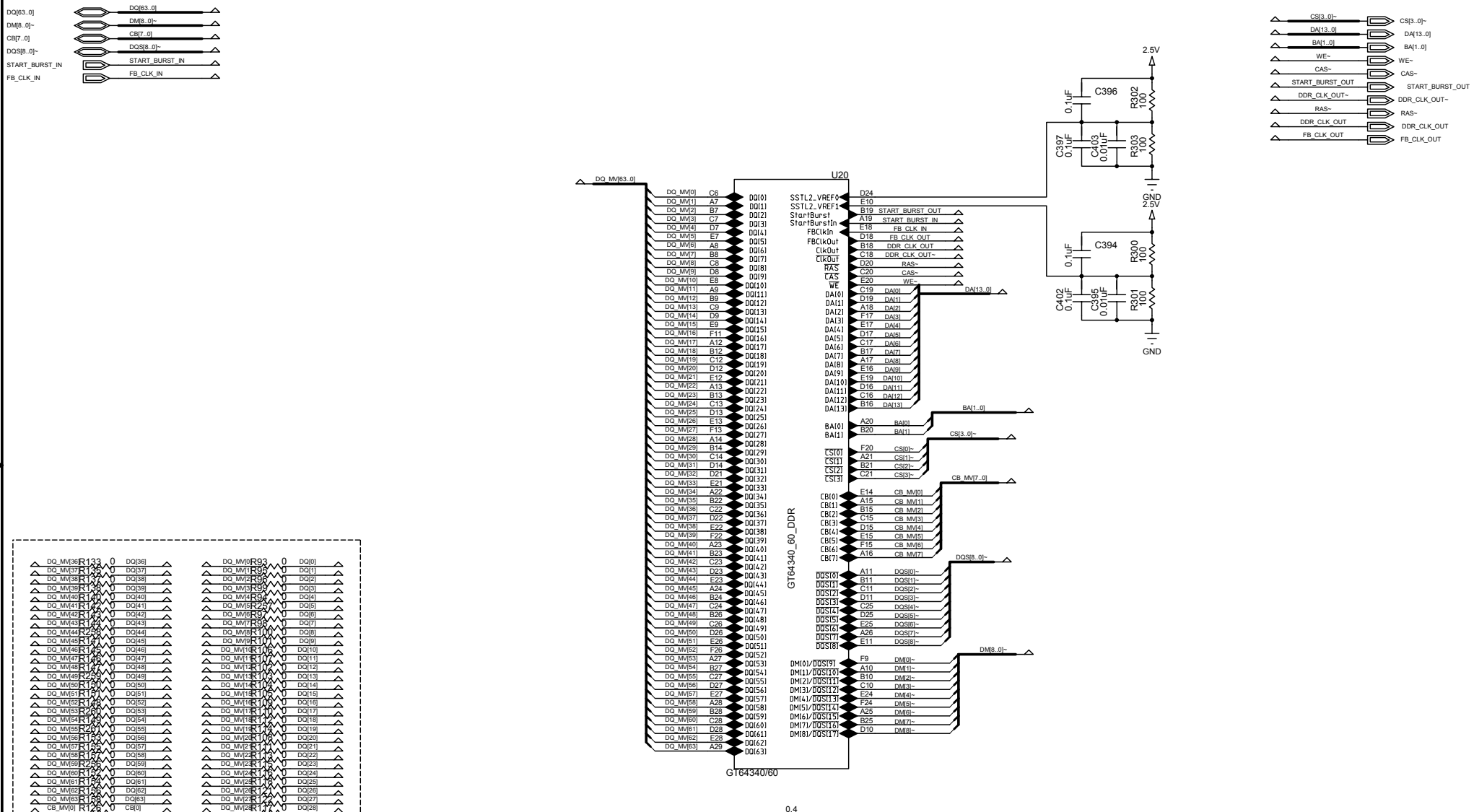
DQ[63..0]
DM[8..0]~
CB[7..0]
DQS[8..0]~
START_BURST_IN
FB_CLK_IN
CS[3..0]~
DA[13..0]
BA[1..0]
WE~
CAS~
START_BURST_OUT
DDR_CLK_OUT~
RAS~
DDR_CLK_OUT
FB_CLK_OUT
2.5V
C396
0.1uF
R302
100
C397
0.1uF
C403
0.01uF
R303
100
GND
C394
0.1uF
R300
100
C402
0.1uF
C395
0.01uF
R301
100
U20
DQ_MV[63..0]
SSTL2_VREF0
SSTL2_VREF1
StartBurst
StartBurstIn
FBClkIn
FBClkOut
ClkOut
ClkOut
RAS
CAS
WE
DA[0..13]
BA[1..0]
CS[3..0]~
CB_MV[7..0]
DQS[8..0]~
DM[8..0]~
GT64340_60_DDR
GT64340/60
Serial Termination For the data Line to reduce SSO.
0.4
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SIZE B
Board Name: EV64340_60BP
REV 2.1
File Name: MV_64340_60_DDR
Notes
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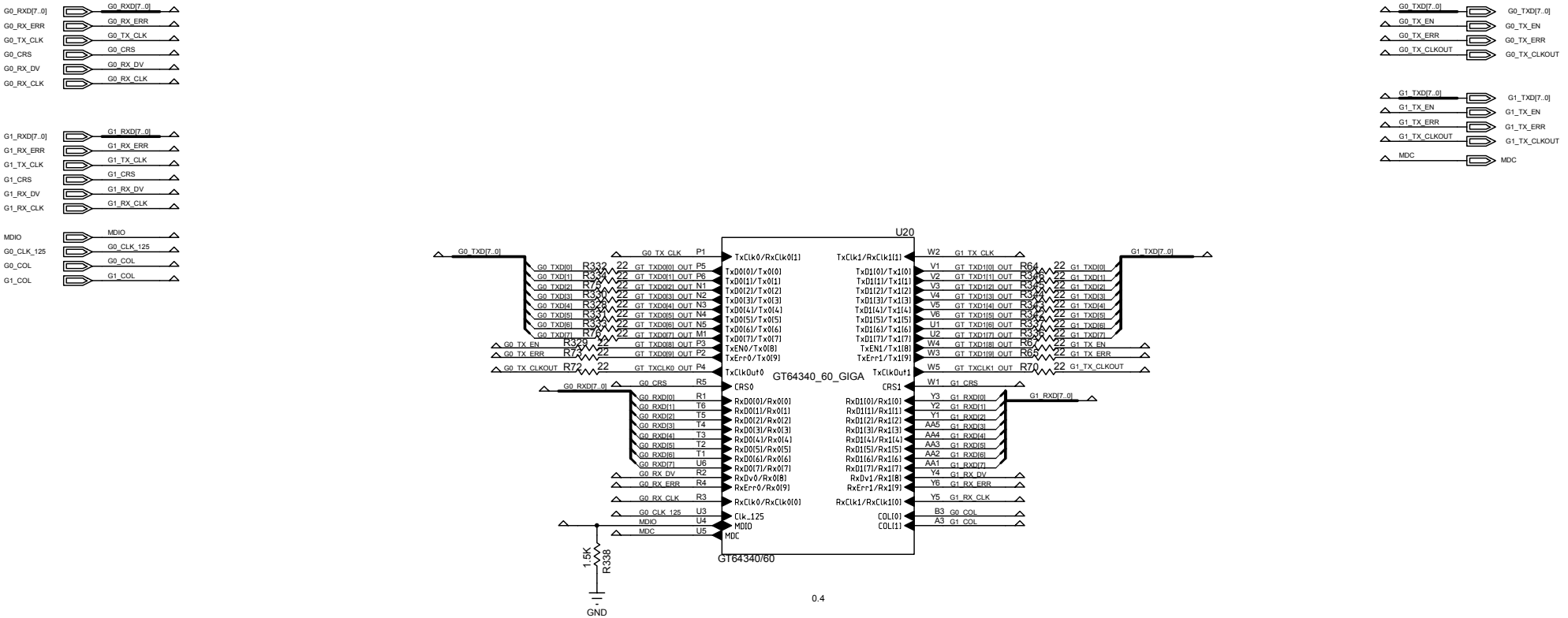
H=2LA; V=2LA



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SIZE B	Board Name: EV64340_60BP	REV 2.1
File Name: MV64340_60_GIGA Notes	SHEET @HierPageNumber OF @HierPageTotal	

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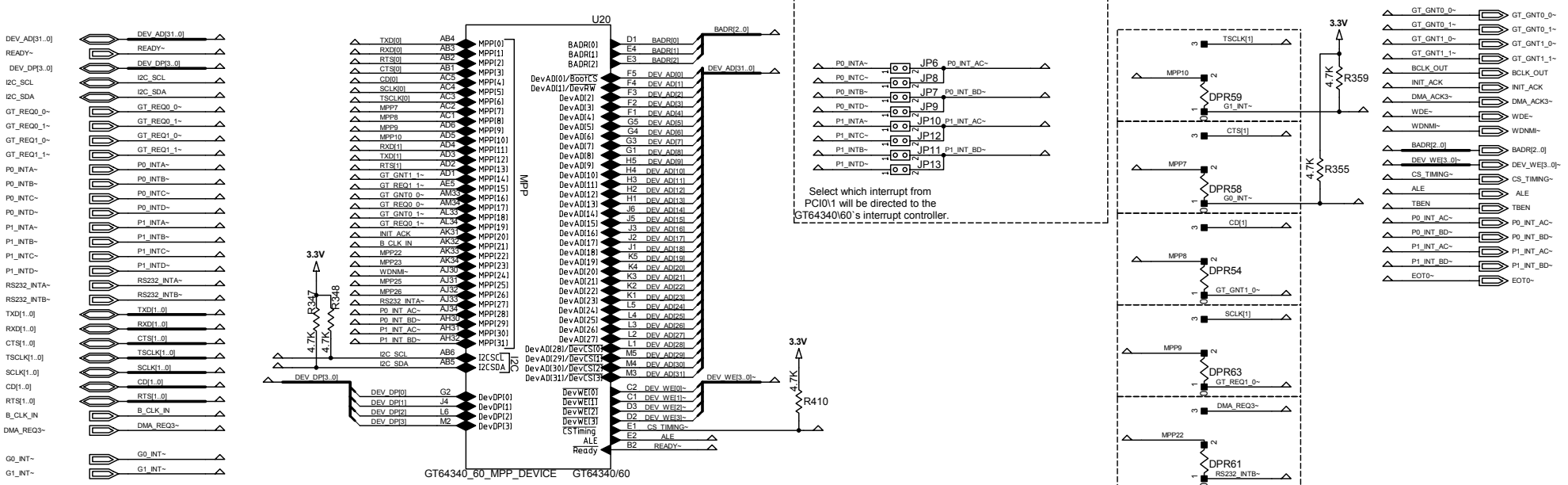

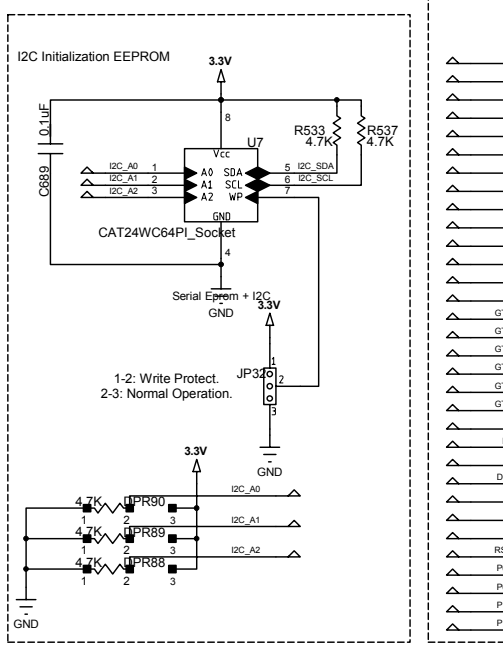

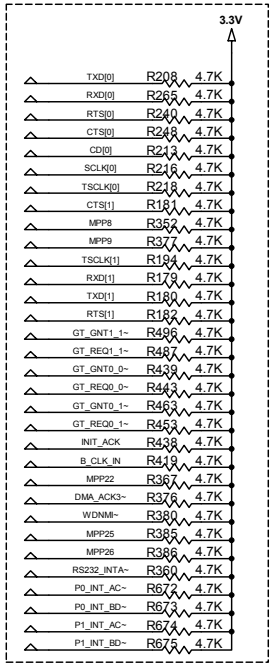

	Default setting	Multiplex #1	Multiplex #2	Multiplex #3
MPP0	TxD0			
MPP1	RxD0			
MPP2	RTS0			
MPP3	CTS0			
MPP4	CD0			
MPP5	SCLK0			
MPP6	TSCLK0			
MPP7	GPIO[7] - G0_INT*	CTS1		
MPP8	GNT1[4]	CD1		
MPP9	REQ1[4]	SCLK1		
MPP10	GPIO[7] - G1_INT*	TSCLK1		
MPP11	RXD1			
MPP12	TXD1			
MPP13	RTS1			
MPP14	GNT1[1]			
MPP15	REQ1[1]			
MPP16	GNT0[0]			
MPP17	REQ0[0]			
MPP18	GNT0[1]			
MPP19	REQ0[1]			
MPP20	InitAct			
MPP21	BClkIn			
MPP22	GPIO[22] - RS232B	DMAReq3		
MPP23	BClkOut	TBEN	DMAAck3	EOT0
MPP24	WDNMI			
MPP25	WDE	TCTcnt0		
MPP26	GPIO[26] - MPSCINT	TCEn1		
MPP27	GPIO[27] - RS232A			
MPP28	GPIO[28] - PCI1 B,D			
MPP29	GPIO[29] - PCI1 A,C			
MPP30	GPIO[30] - PCI0 B,D			
MPP31	GPIO[31] - PCI0 A,C			

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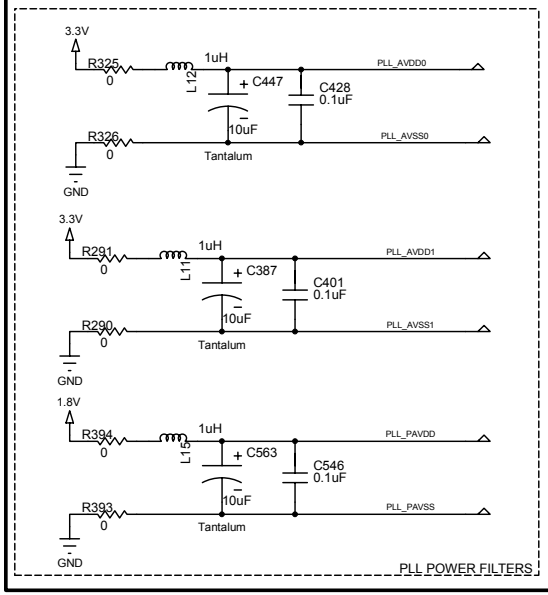
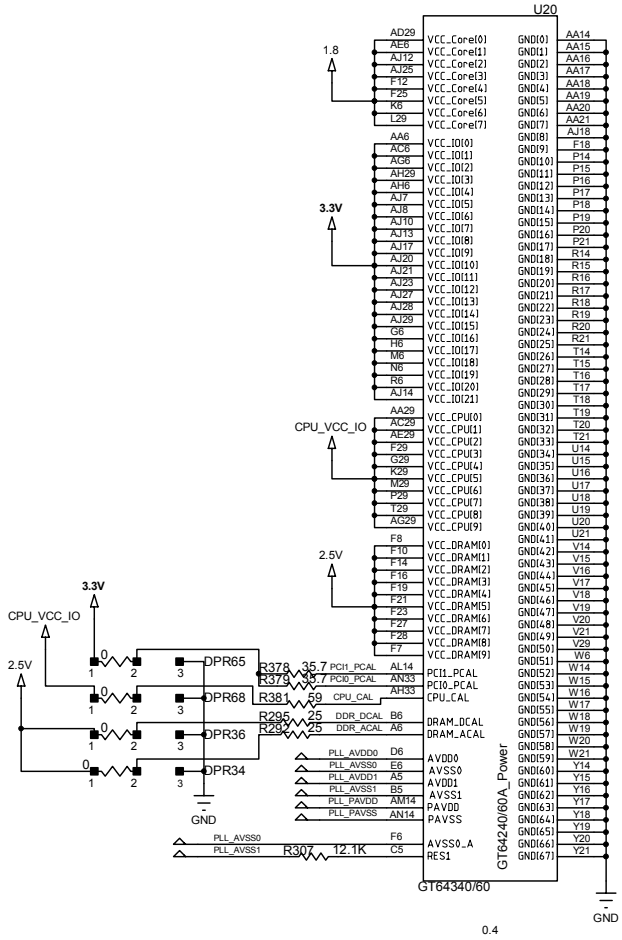
SIZE	Board Name: EV64340_60BP	REV
B		2.1

File Name: MV64340_60_MPP_DEVICE Notes

SHEET @HierPageNumber OF @HierPageTotal

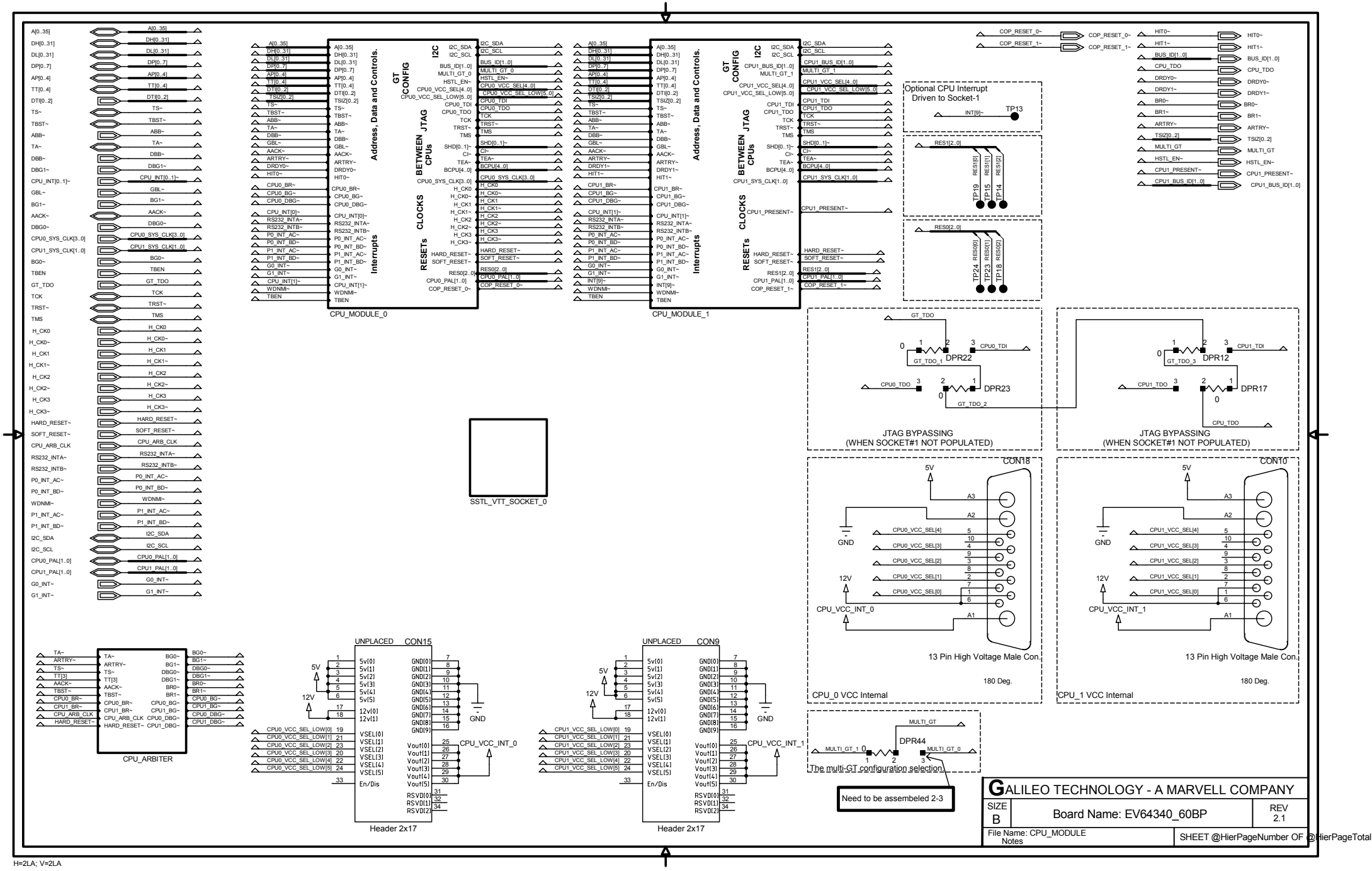
H=2LA; V=2LA

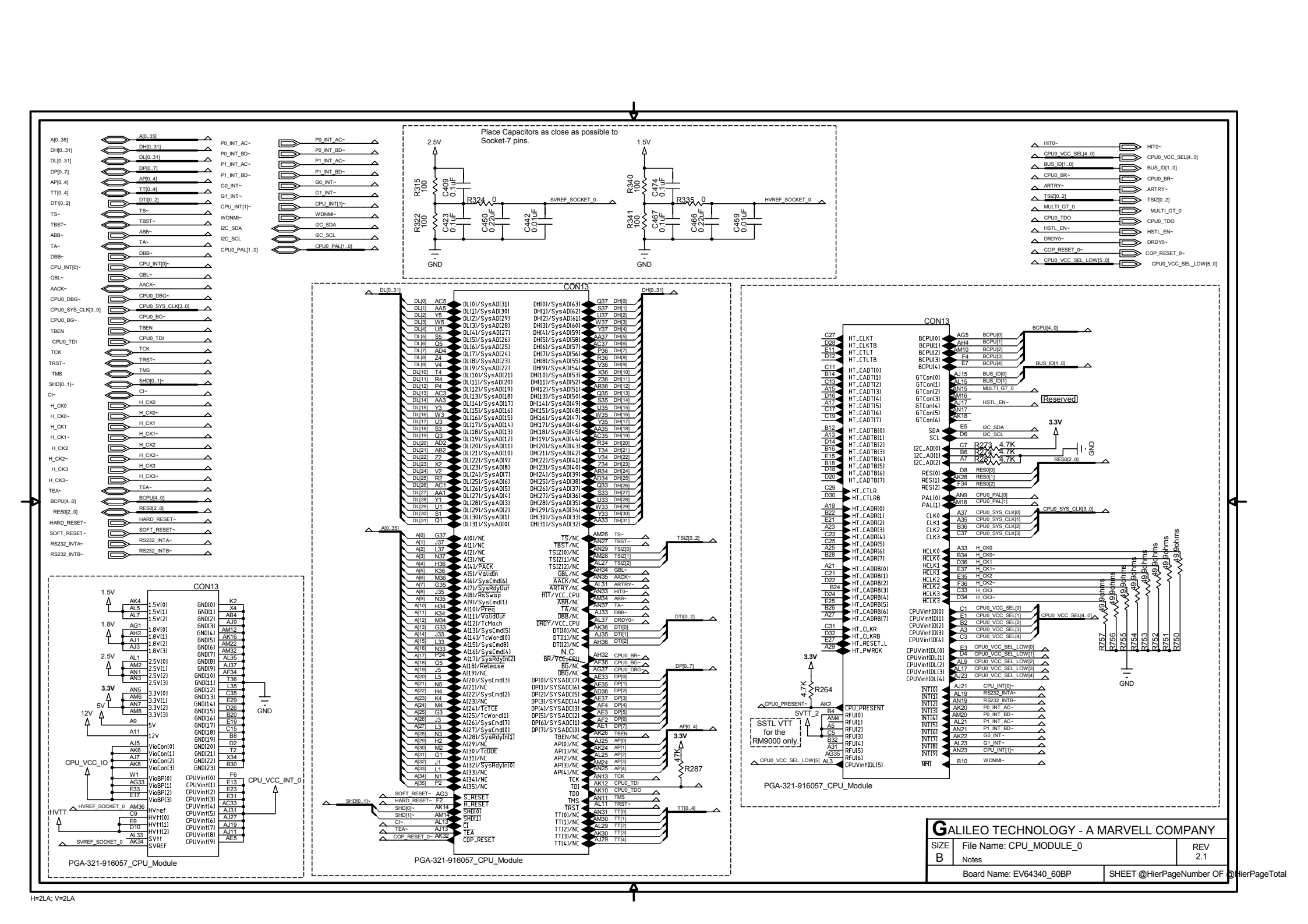


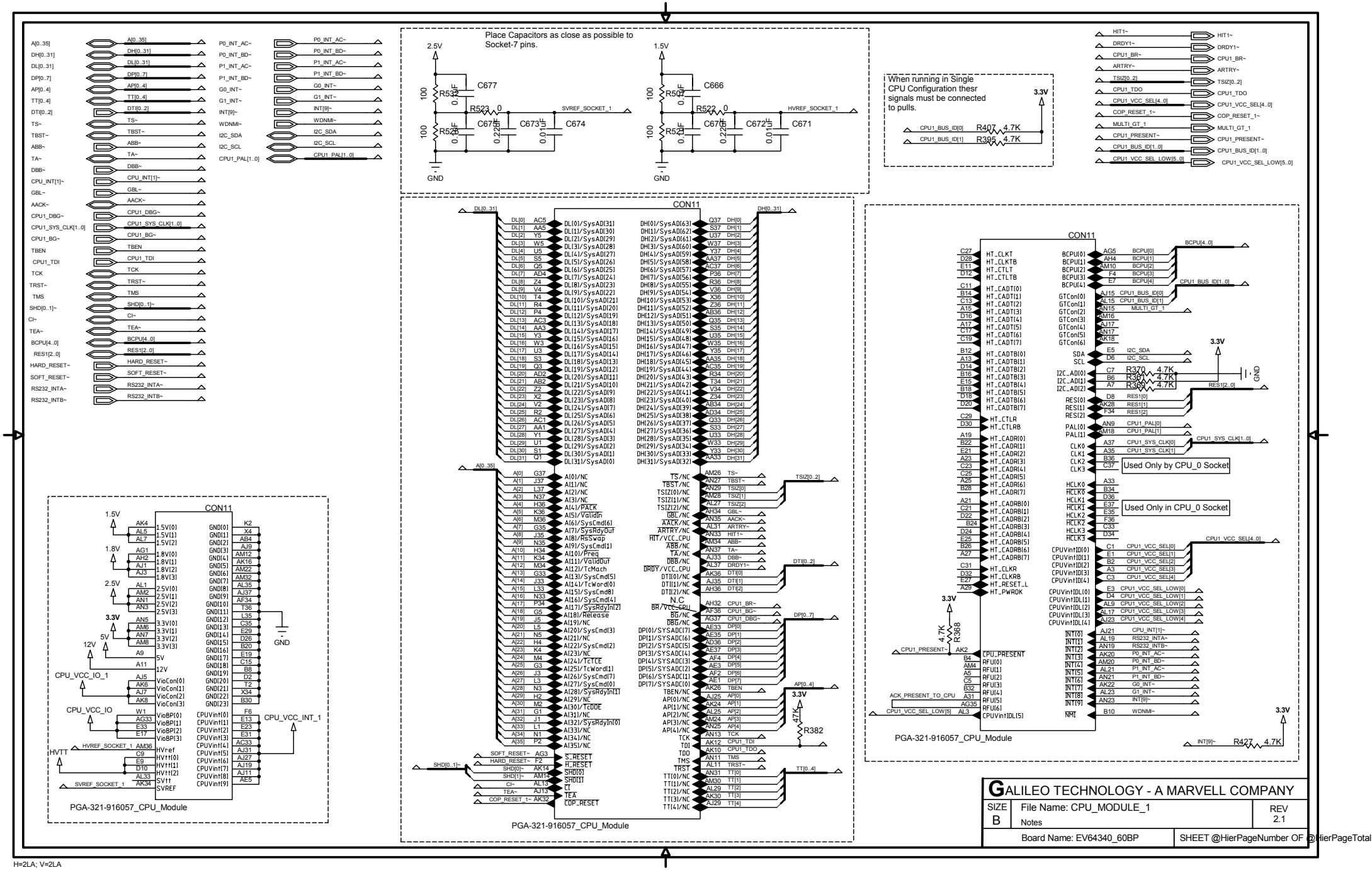


GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	Board Name: EV64340_60BP	REV 2.1
File Name: MV64340_60_POWER Notes	SHEET @HierPageNumber OF @HierPageTotal	

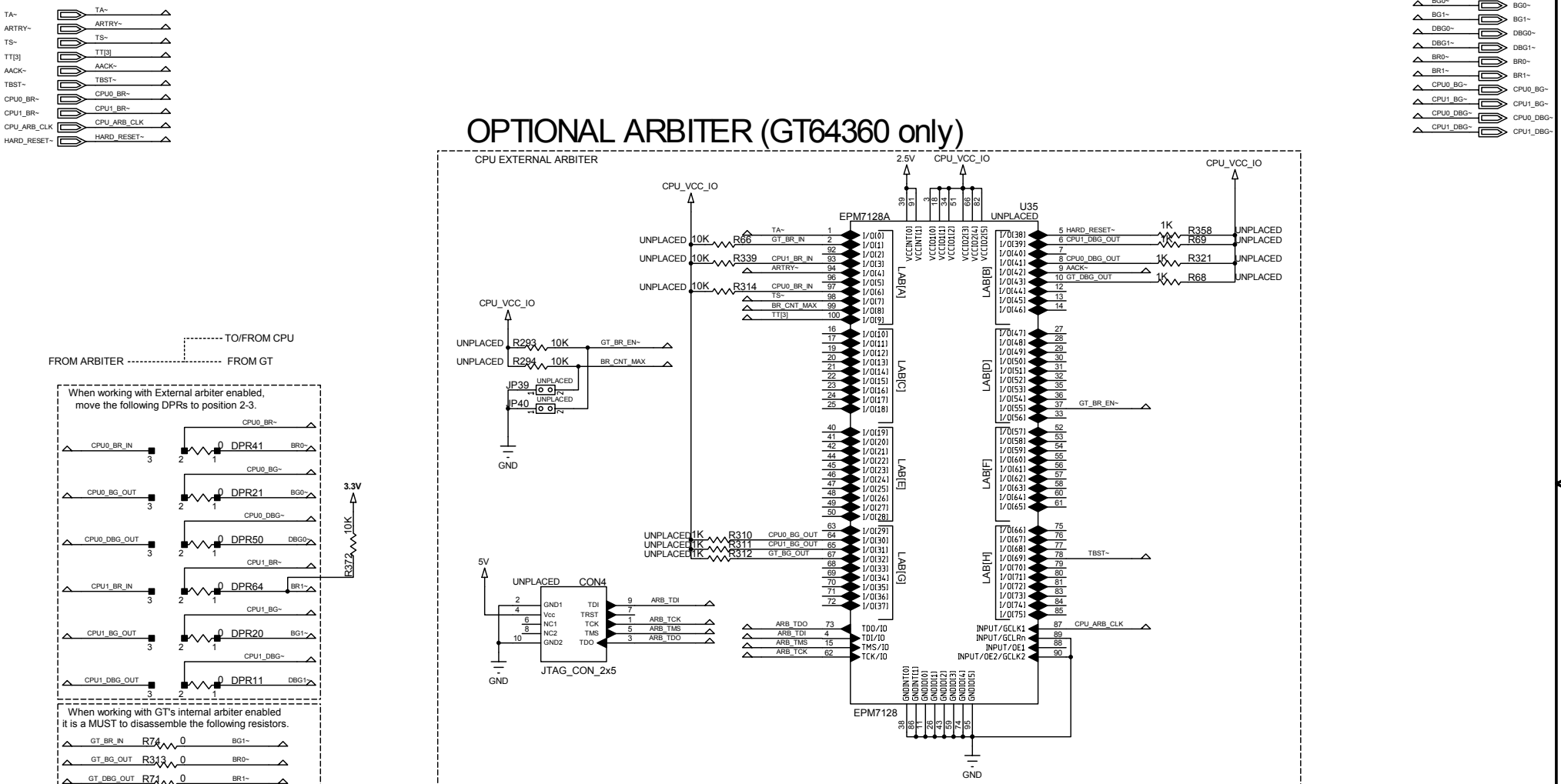
H=2LA; V=2LA


A[0..35]
DH[0..31]
DL[0..31]
DP[0..7]
AP[0..4]
TT[0..4]
DT[0..2]
TS~
TBST~
ABB~
TA~
DBB~
DBG1~
CPU_INT[0..1]~
GBL~
BG1~
AACK~
DBG0~
CPU0_SYS_CLK[3..0]
CPU1_SYS_CLK[1..0]
BG0~
TBEN
GT_TDO
TCK
TRST~
TMS
H_CK0
H_CK0~
H_CK1
H_CK1~
H_CK2
H_CK2~
H_CK3
H_CK3~
HARD_RESET~
SOFT_RESET~
CPU_ARB_CLK
RS232_INTA~
RS232_INTB~
P0_INT_AC~
P0_INT_BD~
WDNMI~
P1_INT_AC~
P1_INT_BD~
I2C_SDA
I2C_SCL
CPU0_PAL[1..0]
CPU1_PAL[1..0]
G0_INT~
G1_INT~
Address, Data and Controls.
GT CONFIG
I2C
JTAG BETWEEN CPUs
CLOCKS
RESETs
Interrupts
BUS_ID[1..0]
MULTI_GT_0
HSTL_EN~
CPU0_VCC_SEL[4..0]
CPU0_VCC_SEL_LOW[5..0]
CPU0_TDI
CPU0_TDO
SHD[0..1]~
CI~
TEA~
BCPU[4..0]
RES0[2..0]
COP_RESET_0~
CPU_MODULE_0
MULTI_GT_1
CPU1_VCC_SEL[4..0]
CPU1_VCC_SEL_LOW[5..0]
CPU1_TDI
CPU1_TDO
CPU1_PRESENT~
RES1[2..0]
COP_RESET_1~
CPU_MODULE_1
COP_RESET_0~
COP_RESET_1~
HIT0~
HIT1~
BR0~
BR1~
ARTRY~
DRDY0~
DRDY1~
MULTI_GT
HSTL_EN~
Optional CPU Interrupt
Driven to Socket-1
INT[9]~
TP13
RES1[2..0]
RES1[0]
RES1[1]
RES1[2]
TP19
TP15
TP14
RES0[2..0]
RES0[0]
RES0[1]
RES0[2]
TP24
TP23
TP18
SSTL_VTT_SOCKET_0
GT_TDO
DPR22
CPU0_TDI
GT_TDO_1
GT_TDO_2
DPR23
JTAG BYPASSING
(WHEN SOCKET#1 NOT POPULATED)
CPU1_TDI
GT_TDO_3
DPR12
DPR17
CPU_TDO
JTAG BYPASSING
(WHEN SOCKET#1 NOT POPULATED)
CON18
5V
GND
12V
CPU0_VCC_SEL[4]
CPU0_VCC_SEL[3]
CPU0_VCC_SEL[2]
CPU0_VCC_SEL[1]
CPU0_VCC_SEL[0]
CPU_VCC_INT_0
13 Pin High Voltage Male Con.
180 Deg.
CPU_0 VCC Internal
CON10
CPU1_VCC_SEL[4]
CPU1_VCC_SEL[3]
CPU1_VCC_SEL[2]
CPU1_VCC_SEL[1]
CPU1_VCC_SEL[0]
CPU_VCC_INT_1
13 Pin High Voltage Male Con.
180 Deg.
CPU_1 VCC Internal
CPU_ARBITER
UNPLACED
CON15
Header 2x17
CPU_VCC_INT_0
CON9
CPU_VCC_INT_1
MULTI_GT
DPR44
MULTI_GT_1
MULTI_GT_0
The multi-GT configuration selection
Need to be assembeled 2-3
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
Board Name: EV64340_60BP
REV 2.1
File Name: CPU_MODULE
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA


A[0..35]
DH[0..31]
DL[0..31]
DP[0..7]
AP[0..4]
TT[0..4]
DT[0..2]
TS~
TBST~
ABB~
TA~
DBB~
CPU_INT[0]~
GBL~
AACK~
CPU0_DBG~
CPU0_SYS_CLK[3..0]
CPU0_BG~
TBEN
CPU0_TDI
TCK
TRST~
TMS
SHD[0..1]~
CI~
H_CK0
H_CK0~
H_CK1
H_CK1~
H_CK2
H_CK2~
H_CK3
H_CK3~
TEA~
BCPU[4..0]
RES0[2..0]
HARD_RESET~
SOFT_RESET~
RS232_INTA~
RS232_INTB~
P0_INT_AC~
P0_INT_BD~
P1_INT_AC~
P1_INT_BD~
G0_INT~
G1_INT~
CPU_INT[1]~
WDNMI~
I2C_SDA
I2C_SCL
CPU0_PAL[1..0]
Place Capacitors as close as possible to
Socket-7 pins.
2.5V
1.5V
R315 100
R322 100
R340 100
R341 100
C409 0.1uF
C423 0.1uF
C450 0.22uF
C442 0.01uF
C474 0.1uF
C467 0.1uF
C466 0.22uF
C459 0.01uF
R324 0
R335 0
SVREF_SOCKET_0
HVREF_SOCKET_0
GND
HIT0~
CPU0_VCC_SEL[4..0]
BUS_ID[1..0]
CPU0_BR~
ARTRY~
TSIZ[0..2]
MULTI_GT_0
CPU0_TDO
HSTL_EN~
DRDY0~
COP_RESET_0~
CPU0_VCC_SEL_LOW[5..0]
CON13
DL[0..31]
DH[0..31]
A[0..35]
TSIZ[0..2]
DT[0..2]
DP[0..7]
AP[0..4]
TT[0..4]
SHD[0..1]~
SOFT_RESET~
HARD_RESET~
TEA~
COP_RESET~
S_RESET
H_RESET
SHD[0]
SHD[1]
CI
TEA
COP_RESET
PGA-321-916057_CPU_Module
BCPU[4..0]
BUS_ID[1..0]
Reserved
3.3V
I2C_SDA
I2C_SCL
I2C_AD[0]
I2C_AD[1]
I2C_AD[2]
R273 4.7K
R274 4.7K
R281 4.7K
RES0[2..0]
RES0[0]
RES0[1]
RES0[2]
CPU0_PAL[0]
CPU0_PAL[1]
CPU0_SYS_CLK[3..0]
CPU0_SYS_CLK[0]
CPU0_SYS_CLK[1]
CPU0_SYS_CLK[2]
CPU0_SYS_CLK[3]
H_CK0
H_CK0~
H_CK1
H_CK1~
H_CK2
H_CK2~
H_CK3
H_CK3~
CPU0_VCC_SEL[0]
CPU0_VCC_SEL[1]
CPU0_VCC_SEL[2]
CPU0_VCC_SEL[3]
CPU0_VCC_SEL[4]
CPU0_VCC_SEL_LOW[0]
CPU0_VCC_SEL_LOW[1]
CPU0_VCC_SEL_LOW[2]
CPU0_VCC_SEL_LOW[3]
CPU0_VCC_SEL_LOW[4]
CPU_INT[0]~
RS232_INTA~
RS232_INTB~
P0_INT_AC~
P0_INT_BD~
P1_INT_AC~
P1_INT_BD~
G0_INT~
G1_INT~
CPU_INT[1]~
WDNMI~
R757 49.9ohms
R756 49.9ohms
R755 49.9ohms
R754 49.9ohms
R753 49.9ohms
R752 49.9ohms
R751 49.9ohms
R750 49.9ohms
CPU0_PRESENT~
R264 4.7K
SSTL VTT for the RM9000 only.
SVTT_2
CPU_PRESENT
CPU0_VCC_SEL_LOW[5]
PGA-321-916057_CPU_Module
1.5V
1.8V
2.5V
3.3V
5V
12V
CPU_VCC_IO
CPU_VCC_INT_0
HVTT
HVREF_SOCKET_0
SVREF_SOCKET_0
PGA-321-916057_CPU_Module
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
File Name: CPU_MODULE_0
Notes
REV 2.1
Board Name: EV64340_60BP
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

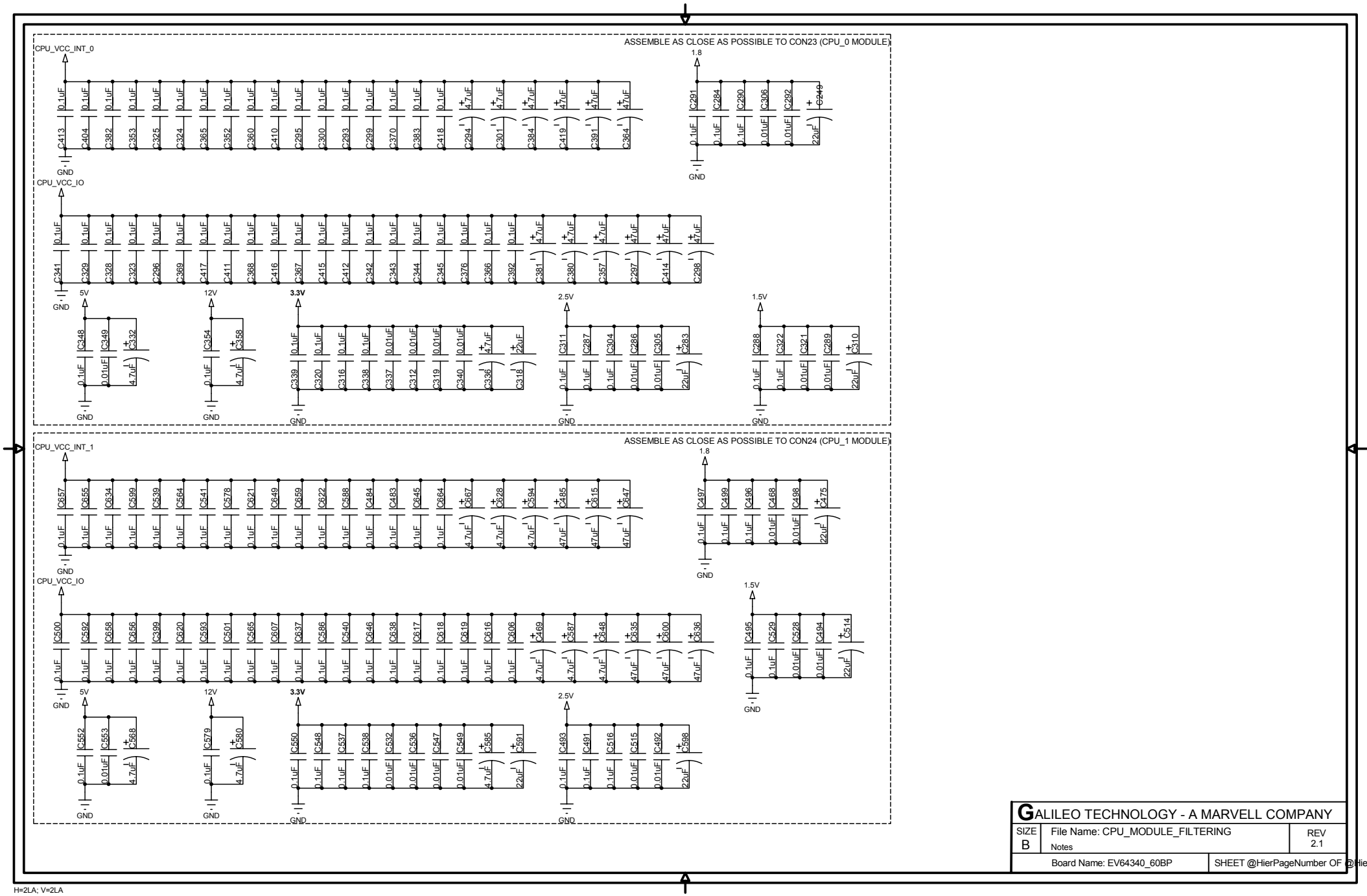

A[0..35]
DH[0..31]
DL[0..31]
DP[0..7]
AP[0..4]
TT[0..4]
DTI[0..2]
TS~
TBST~
ABB~
TA~
DBB~
CPU_INT[1]~
GBL~
AACK~
CPU1_DBG~
CPU1_SYS_CLK[1..0]
CPU1_BG~
TBEN
CPU1_TDI
TCK
TRST~
TMS
SHD[0..1]~
CI~
TEA~
BCPU[4..0]
RES1[2..0]
HARD_RESET~
SOFT_RESET~
RS232_INTA~
RS232_INTB~
P0_INT_AC~
P0_INT_BD~
P1_INT_AC~
P1_INT_BD~
G0_INT~
G1_INT~
INT[9]~
WDNMI~
I2C_SDA
I2C_SCL
CPU1_PAL[1..0]
Place Capacitors as close as possible to Socket-7 pins.
2.5V
1.5V
R532
R523
R526
R506
R522
R521
C677
C676
C673
C674
C666
C670
C672
C671
0.22uF
0.01uF
100
0
GND
SVREF_SOCKET_1
HVREF_SOCKET_1
When running in Single CPU Configuration thesr signals must be connected to pulls.
CPU1_BUS_ID[0]
CPU1_BUS_ID[1]
R407
R385
4.7K
HIT1~
DRDY1~
CPU1_BR~
ARTRY~
TSIZ[0..2]
CPU1_TDO
CPU1_VCC_SEL[4..0]
COP_RESET_1~
MULTI_GT_1
CPU1_PRESENT~
CPU1_BUS_ID[1..0]
CPU1_VCC_SEL_LOW[5..0]
CON11
PGA-321-916057_CPU_Module
Used Only by CPU_0 Socket
Used Only in CPU_0 Socket
3.3V
5V
12V
1.8V
2.5V
CPU_VCC_IO_1
CPU_VCC_IO
CPU_VCC_INT_1
HVTT
R370
R369
R368
R382
R427
ACK_PRESENT_TO_CPU
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
File Name: CPU_MODULE_1
Notes
REV 2.1
Board Name: EV64340_60BP
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

OPTIONAL ARBITER (GT64360 only)



GALILEO TECHNOLOGY - A MARVELL COMPANY	
SIZE B	File Name: CPU_ARBITER
Notes	REV 2.1
Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal

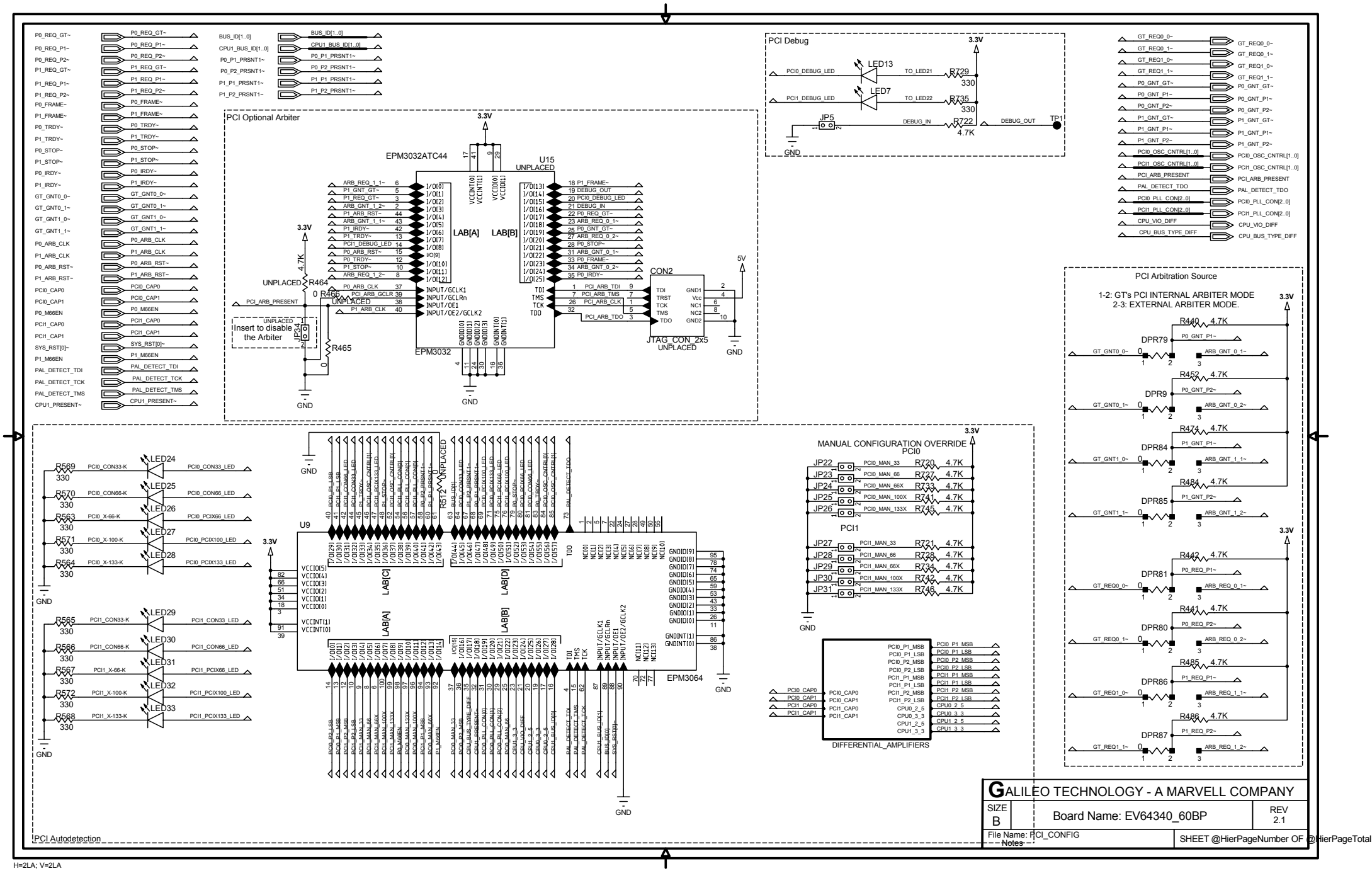
H=2LA; V=2LA

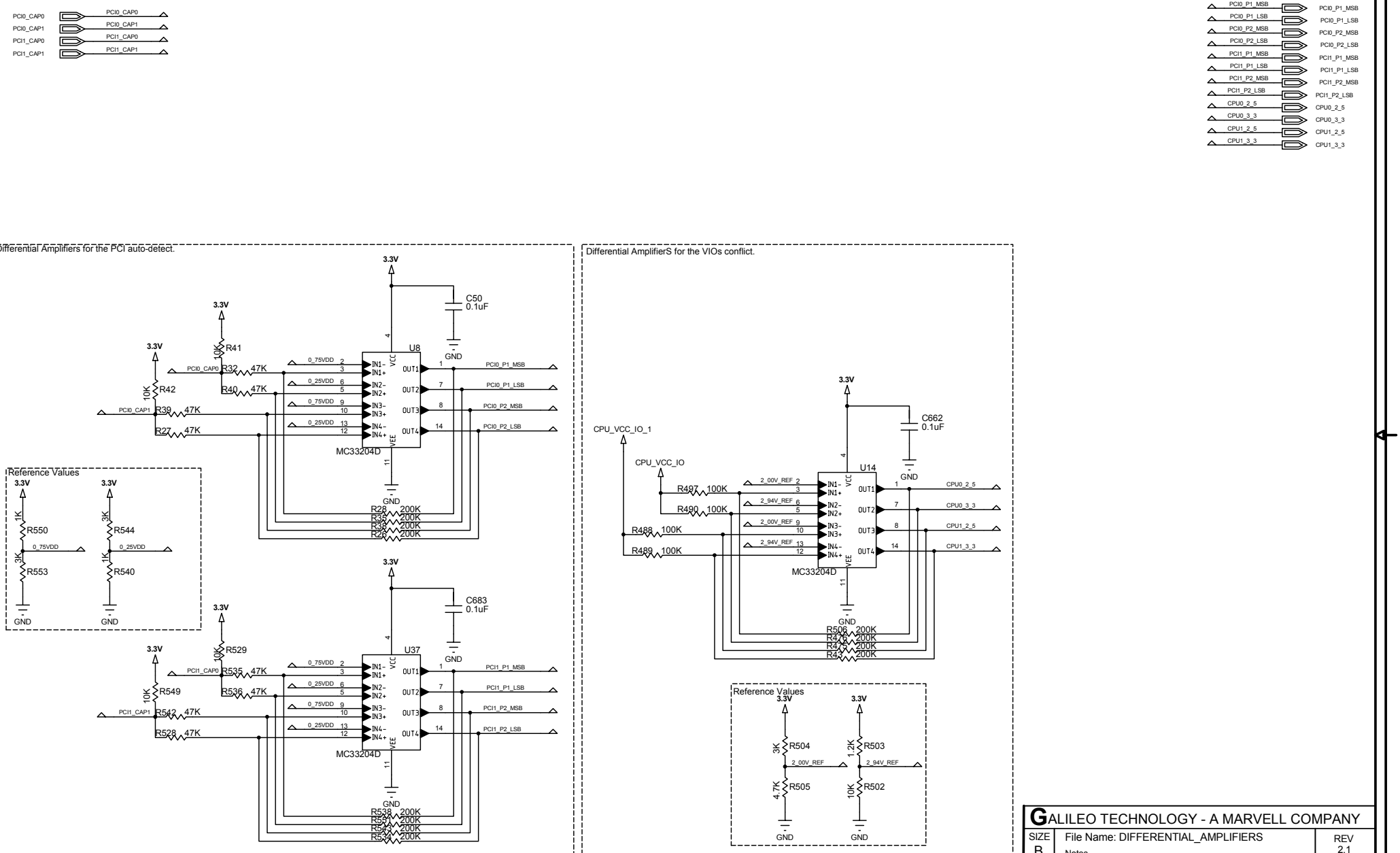


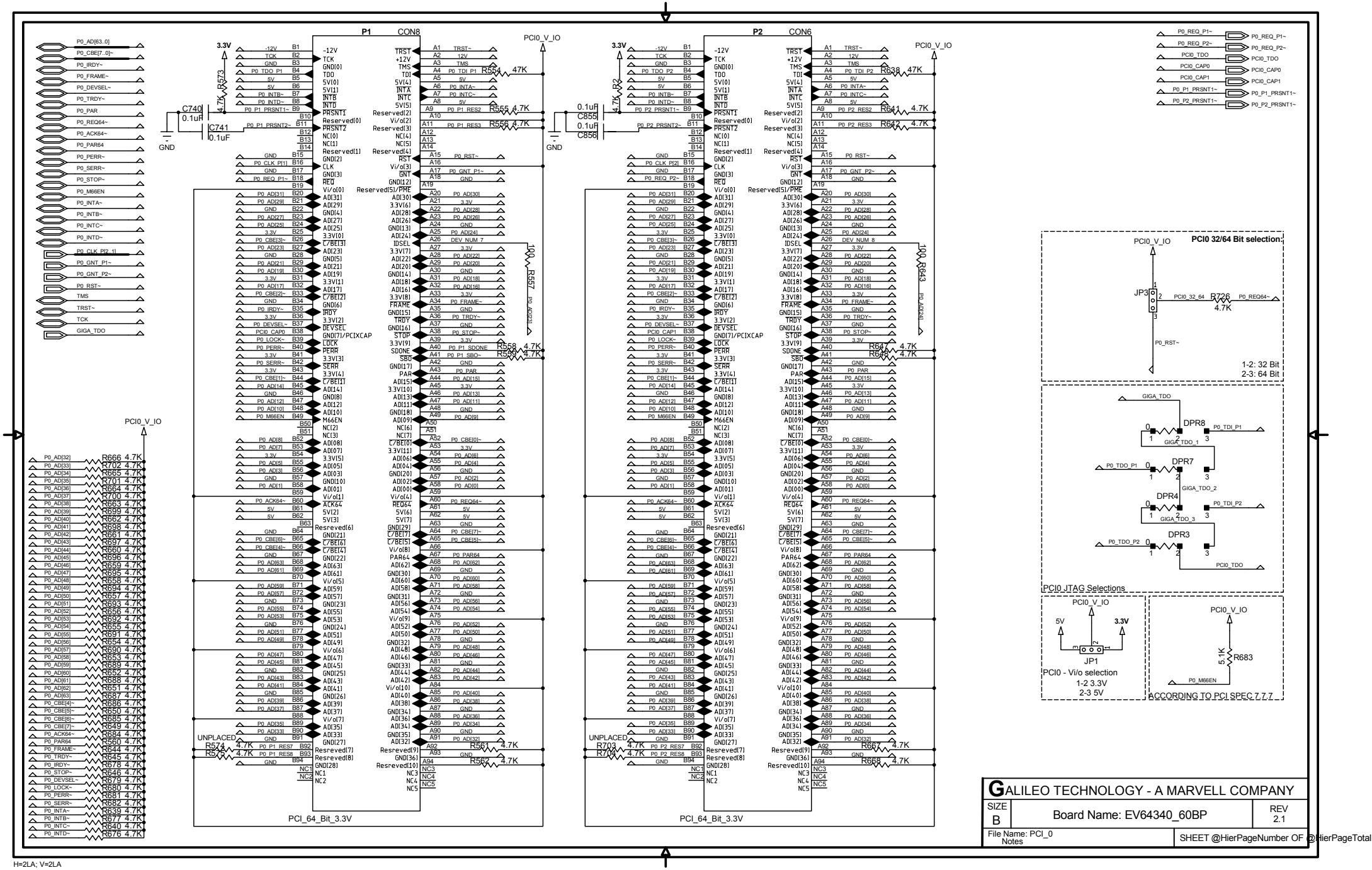
GALILEO TECHNOLOGY - A MARVELL COMPANY

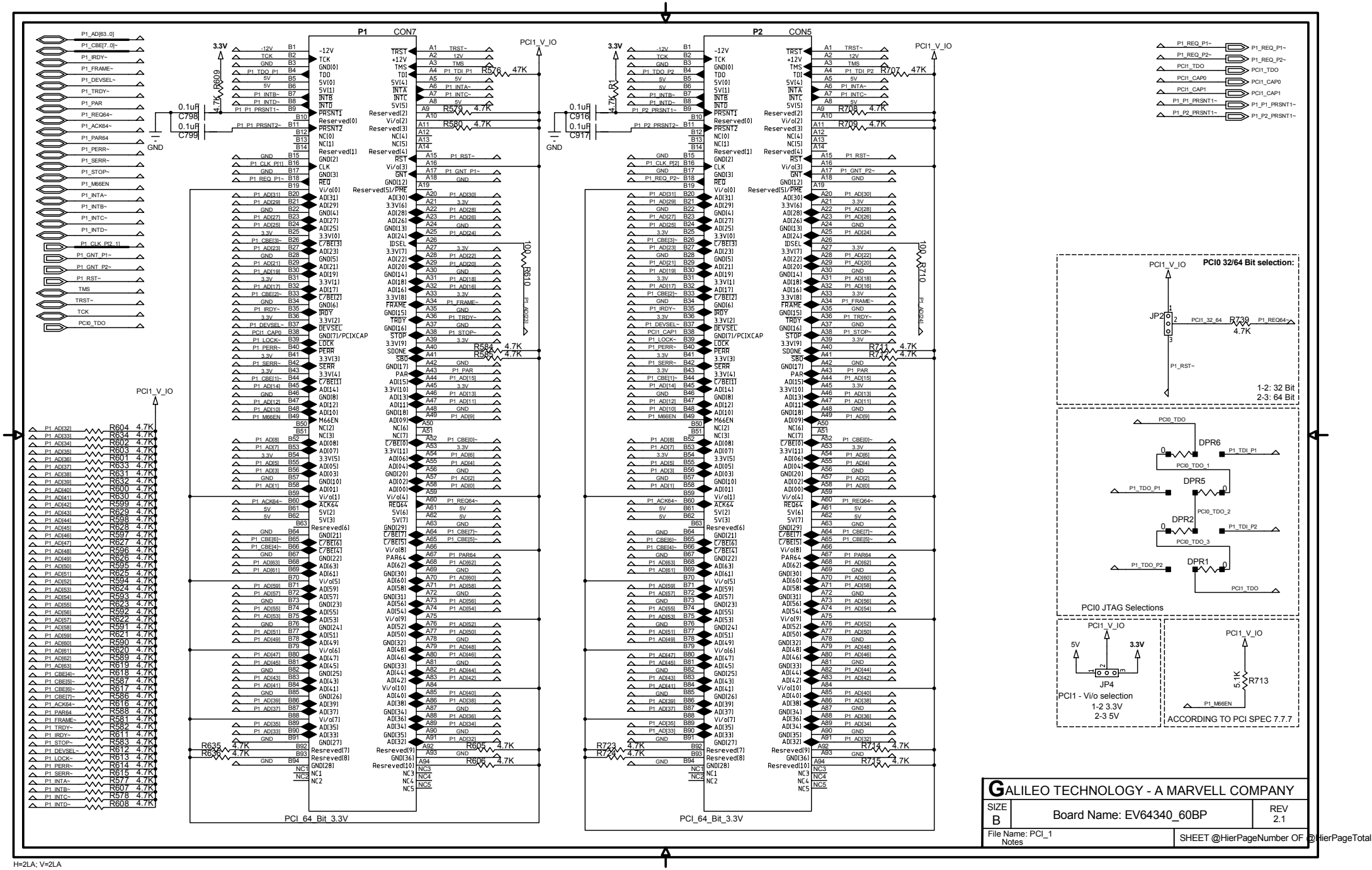
SIZE	File Name: CPU_MODULE_FILTERING	REV
B	Notes	2.1
	Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal

H=2LA; V=2LA

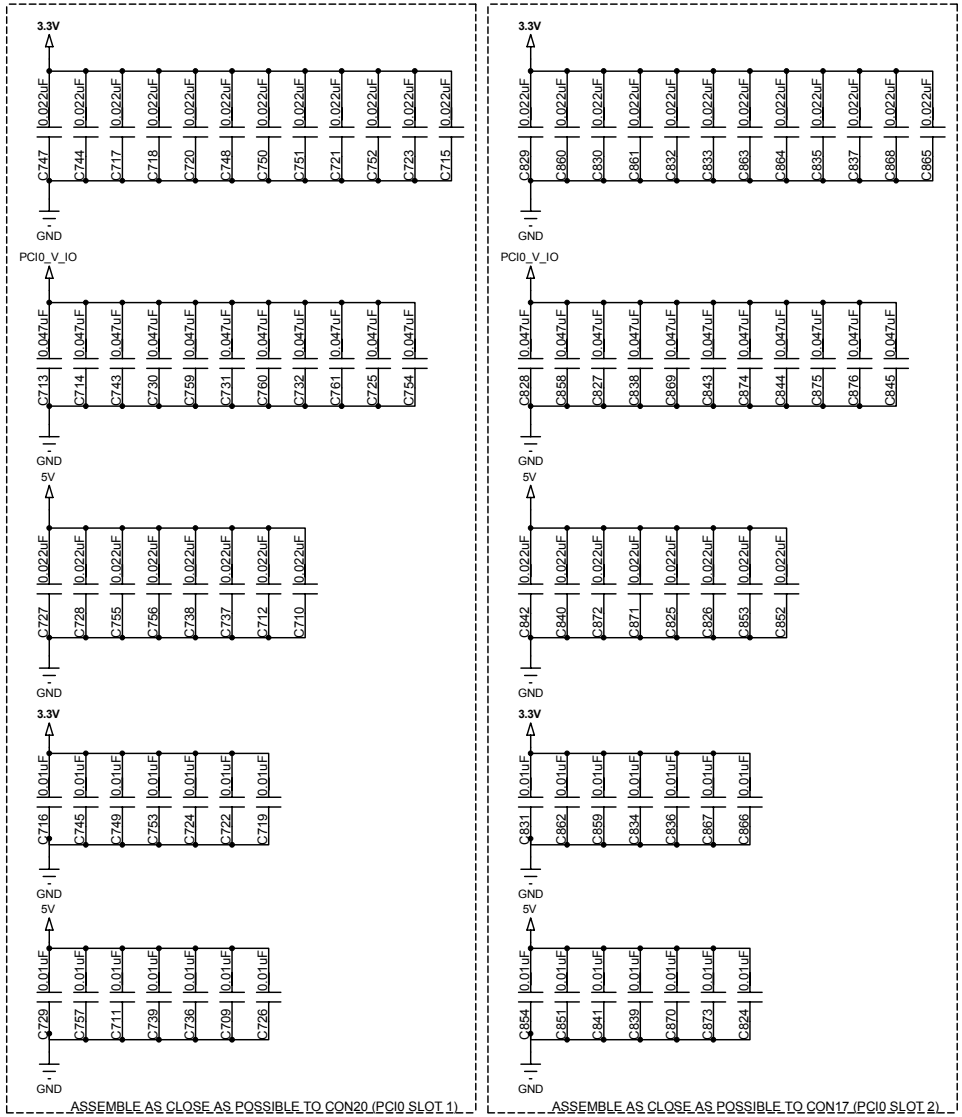

PCI Optional Arbiter
EPM3032ATC44
U15
UNPLACED
LAB[A]
LAB[B]
EPM3032
CON2
JTAG_CON_2x5
UNPLACED
Insert to disable the Arbiter
PCI Debug
LED13
LED7
PCI Arbitration Source
1-2: GT's PCI INTERNAL ARBITER MODE
2-3: EXTERNAL ARBITER MODE.
MANUAL CONFIGURATION OVERRIDE
PCI0
PCI1
U9
EPM3064
LAB[C]
LAB[D]
DIFFERENTIAL_AMPLIFIERS
PCI Autodetection
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
SIZE B
REV 2.1
File Name: PCI_CONFIG
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA


PCI0_CAP0
PCI0_CAP1
PCI1_CAP0
PCI1_CAP1
PCI0_P1_MSB
PCI0_P1_LSB
PCI0_P2_MSB
PCI0_P2_LSB
PCI1_P1_MSB
PCI1_P1_LSB
PCI1_P2_MSB
PCI1_P2_LSB
CPU0_2_5
CPU0_3_3
CPU1_2_5
CPU1_3_3
Differential Amplifiers for the PCI auto-detect.
Differential AmplifierS for the VIOs conflict.
3.3V
C50
0.1uF
U8
MC33204D
R41
R42
R32
R40
R39
R27
47K
10K
0_75VDD
0_25VDD
R28
R35
R36
R26
200K
Reference Values
R550
R553
R544
R540
1K
3K
C683
0.1uF
U37
R529
R549
R535
R536
R542
R528
C662
0.1uF
U14
CPU_VCC_IO_1
CPU_VCC_IO
R497
R490
R488
R489
100K
2_00V_REF
2_94V_REF
R506
R504
R503
R505
R502
1.2K
4.7K
GND
VCC
VEE
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE
B
File Name: DIFFERENTIAL_AMPLIFIERS
Notes
REV
2.1
Board Name: EV64340_60BP
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA


P1 CON8
P2 CON6
PCI_64_Bit_3.3V
PCI_64_Bit_3.3V
PCI0_V_IO
3.3V
GND
UNPLACED
PCI0 32/64 Bit selection:
1-2: 32 Bit
2-3: 64 Bit
PCI0 JTAG Selections
PCI0 - Vi/o selection
1-2 3.3V
2-3 5V
ACCORDING TO PCI SPEC 7.7.7
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
REV 2.1
SIZE B
File Name: PCI_0
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA


P1
CON7
P2
CON5
PCI_64_Bit_3.3V
PCI_64_Bit_3.3V
PCI1_V_IO
3.3V
GND
PCI0 32/64 Bit selection:
1-2: 32 Bit
2-3: 64 Bit
PCI0 JTAG Selections
PCI1 - Vi/o selection
1-2 3.3V
2-3 5V
ACCORDING TO PCI SPEC 7.7.7
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
REV 2.1
SIZE B
File Name: PCI_1
Notes
SHEET @HierPageNumber OF @HierPageTotal

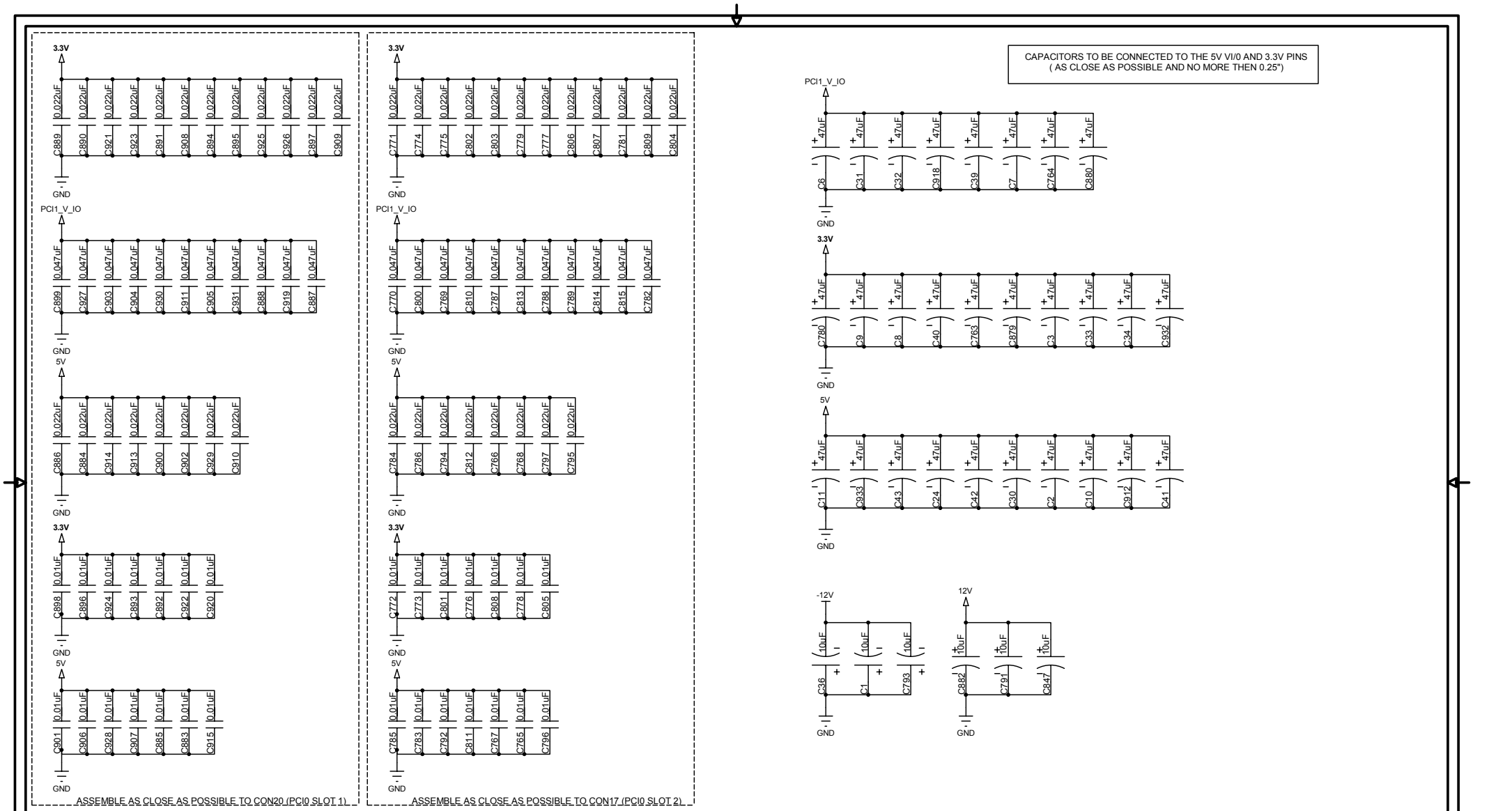
H=2LA; V=2LA



GALILEO TECHNOLOGY - A MARVELL COMPANY

SIZE	File Name: PCI_0_FILTERING	REV
B	Notes	2.1
	Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal

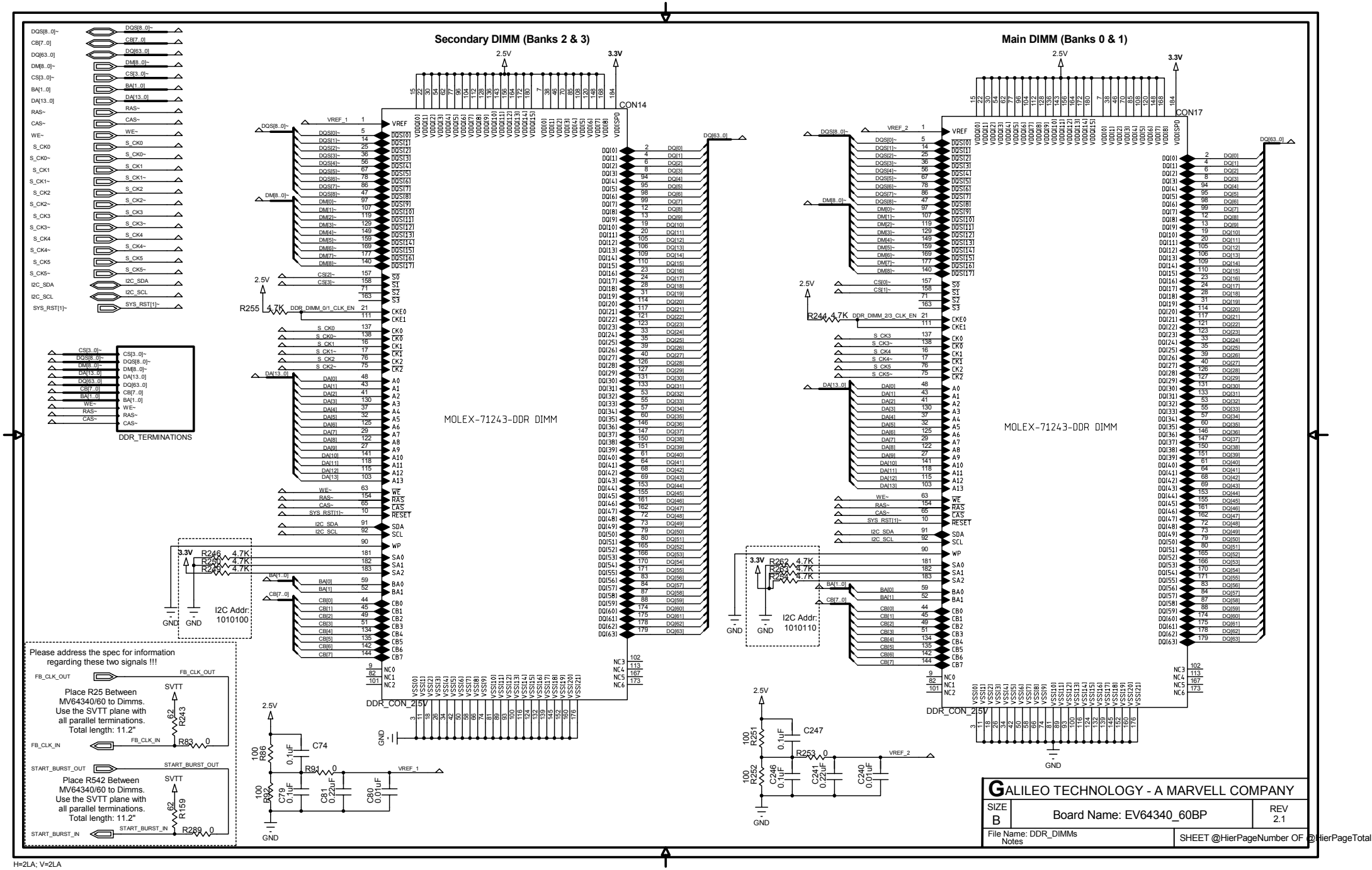
H=2LA; V=2LA



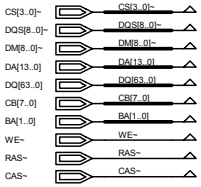
GALILEO TECHNOLOGY - A MARVELL COMPANY

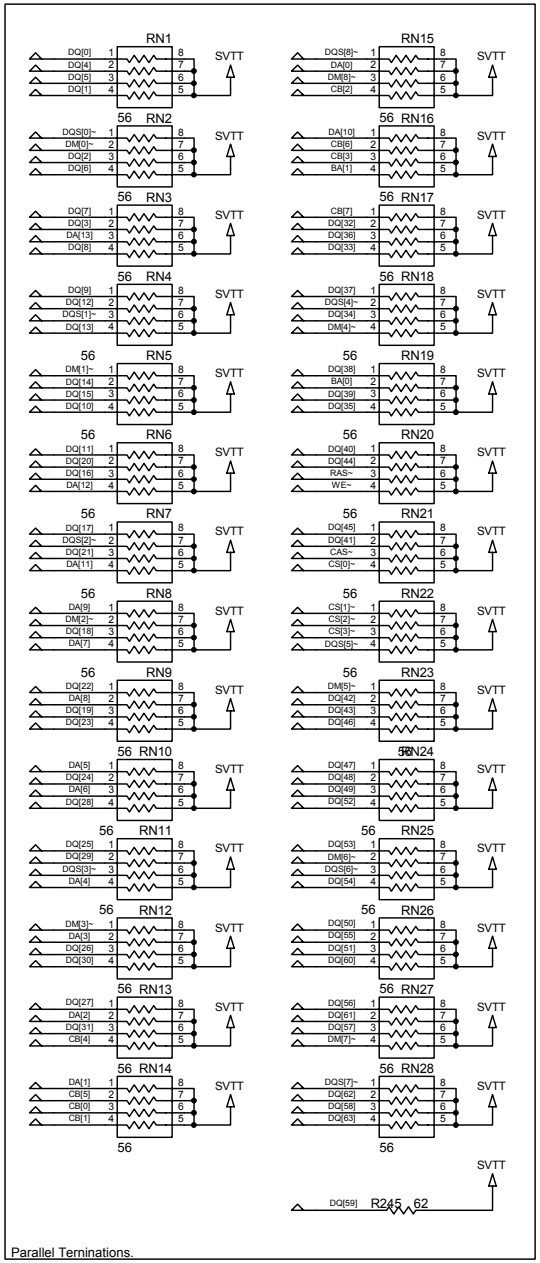
SIZE	File Name: PCI_1_FILTERING	REV
B	Notes	2.1
	Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal

H=2LA; V=2LA

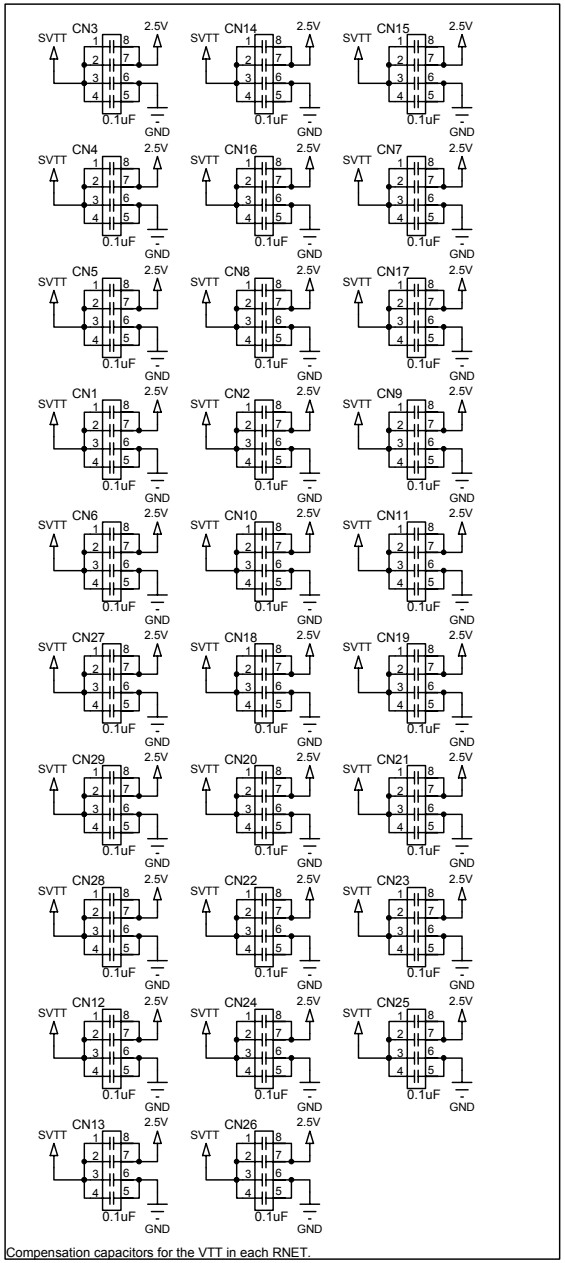

Secondary DIMM (Banks 2 & 3)
Main DIMM (Banks 0 & 1)
MOLEX-71243-DDR DIMM
DDR_TERMINATIONS
DDR_CON_25V
CON14
CON17
I2C Addr: 1010100
I2C Addr: 1010110
Please address the spec for information regarding these two signals !!!
Place R25 Between MV64340/60 to Dimms. Use the SVTT plane with all parallel terminations. Total length: 11.2"
Place R542 Between MV64340/60 to Dimms. Use the SVTT plane with all parallel terminations. Total length: 11.2"
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
REV 2.1
File Name: DDR_DIMMs
Notes
SHEET @HierPageNumber OF @HierPageTotal

H=2LA; V=2LA





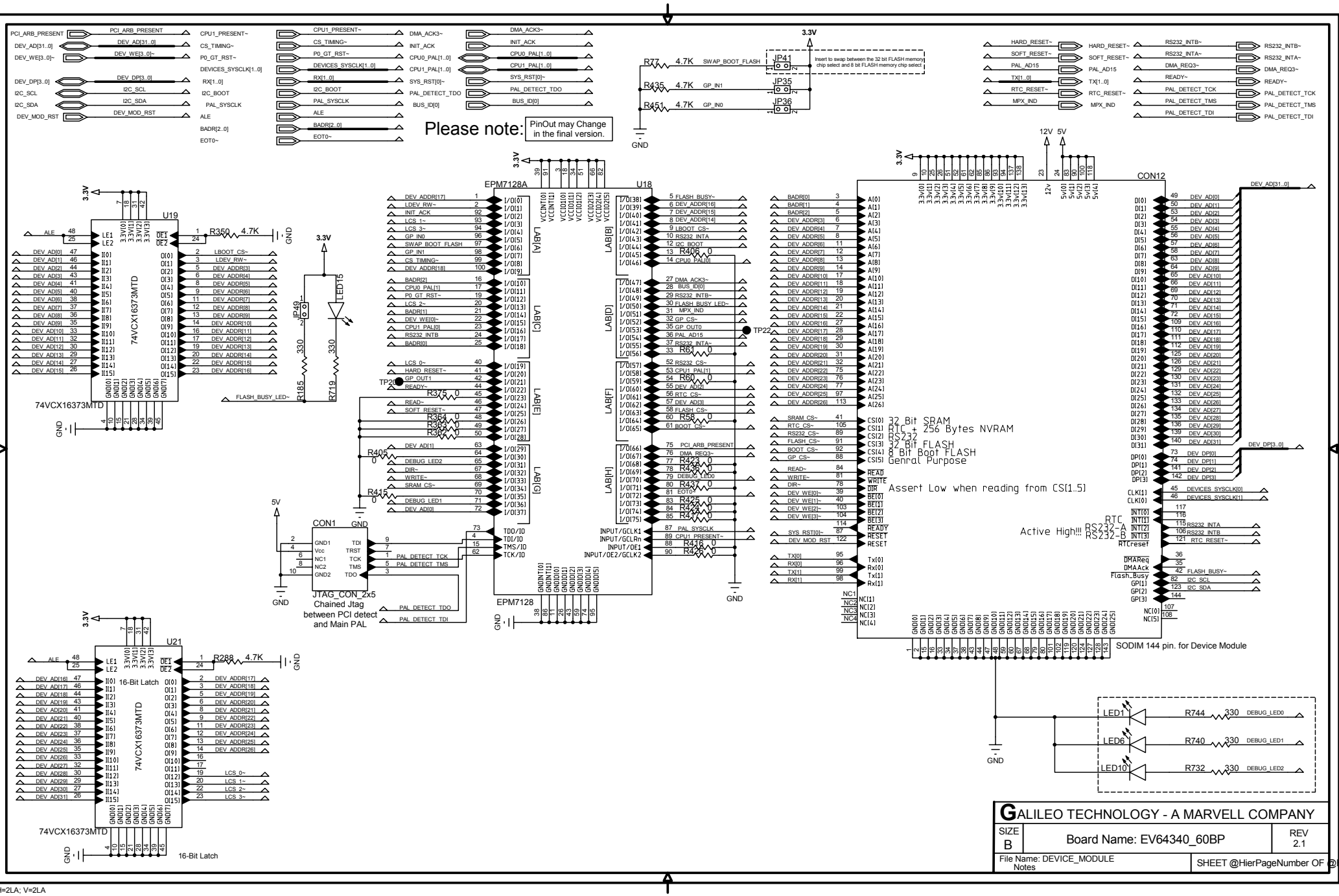
Parallel Terminations.

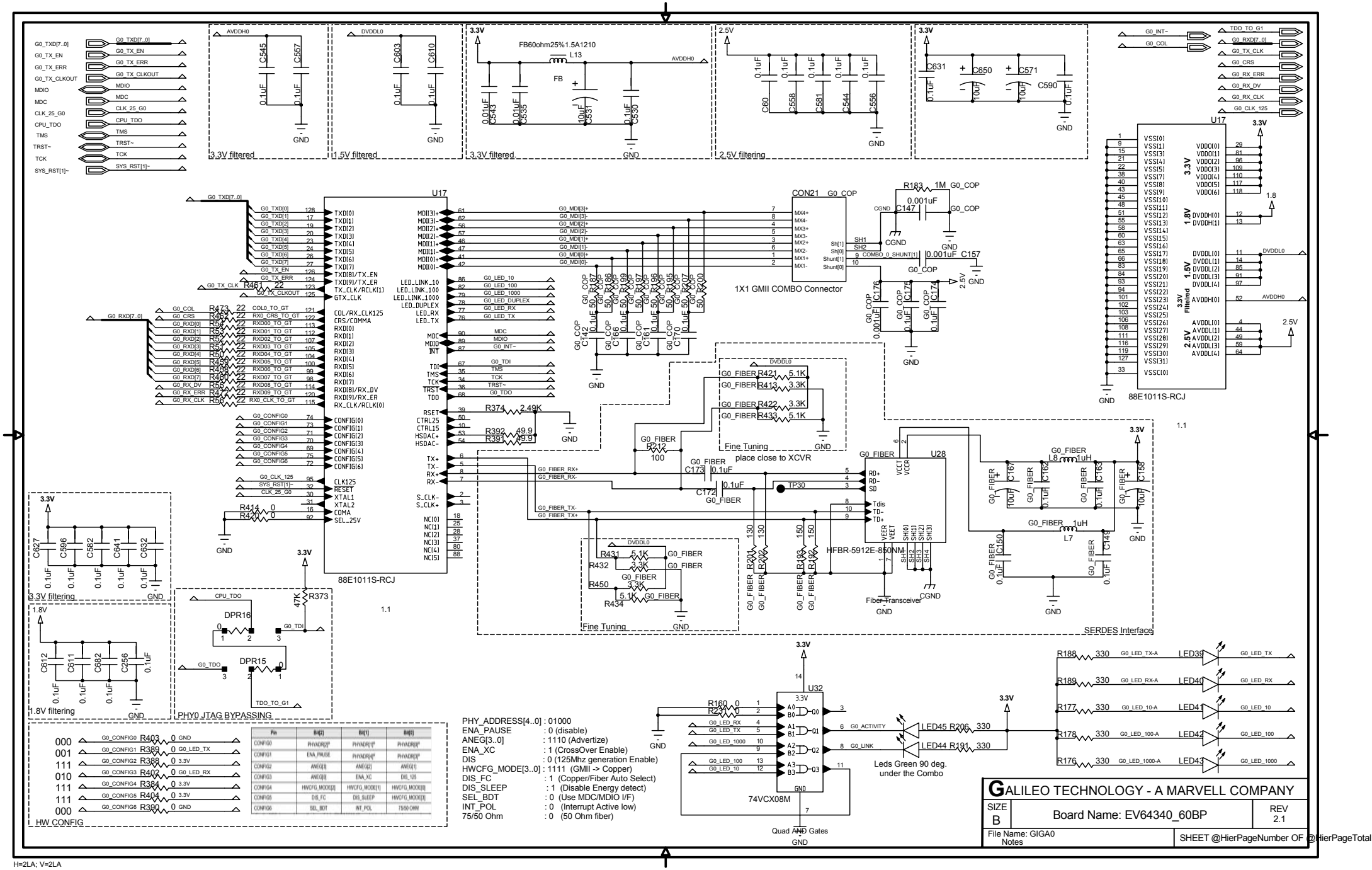


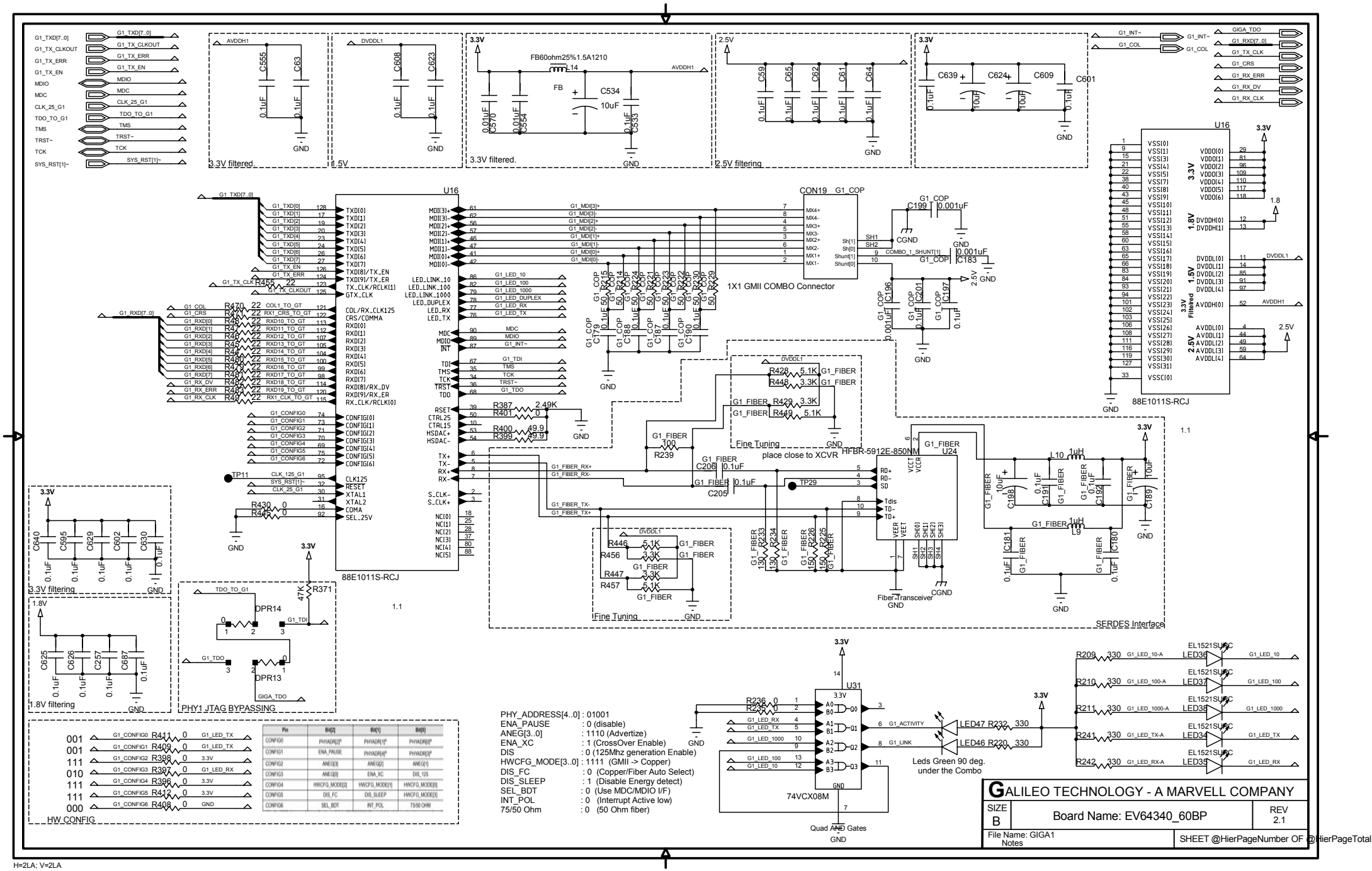
Compensation capacitors for the VTT in each RNET.

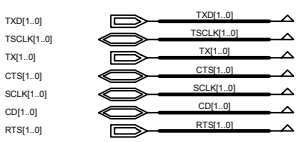
GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	File Name: DDR_TERMINATIONS Notes	REV 2.1
Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal	

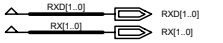
H=2LA; V=2LA

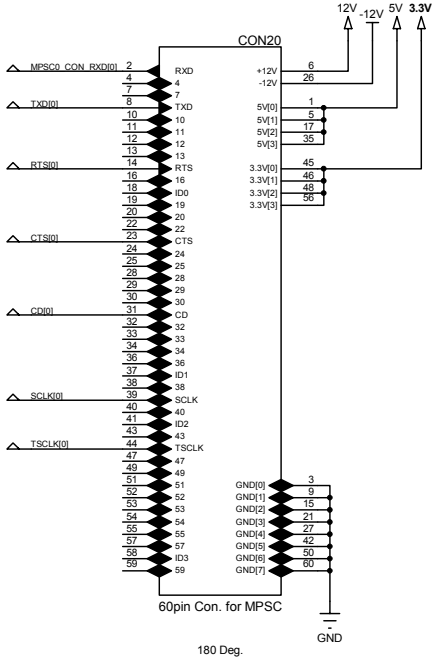

Please note:
PinOut may Change in the final version.
EPM7128A
EPM7128
74VCX16373MTD
74VCX16373MTD
74VCX16373MTD
JTAG_CON_2x5
Chained Jtag between PCI detect and Main PAL
16-Bit Latch
32 Bit SRAM
RTC + 256 Bytes NVRAM
RS232
32 Bit FLASH
8 Bit Boot FLASH
Genral Purpose
Assert Low when reading from CS[1..5]
RTC
Active High!!! RS232-A
RS232-B
SODIM 144 pin. for Device Module
Insert to swap between the 32 bit FLASH memory chip select and 8 bit FLASH memory chip select
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
REV 2.1
File Name: DEVICE_MODULE Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

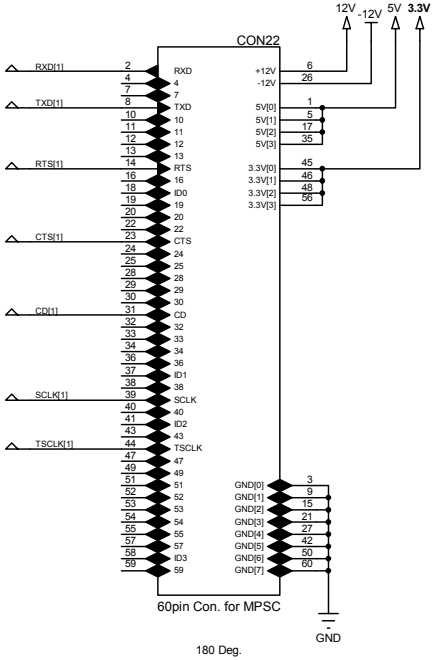

3.3V filtered
1.5V filtered
3.3V filtered
2.5V filtering
1X1 GMII COMBO Connector
88E1011S-RCJ
88E1011S-RCJ
HFBR-5912E-850NM
Fiber-Transceiver
SERDES Interface
Fine Tuning
Fine Tuning
place close to XCVR
3.3V filtering
1.8V filtering
PHY0 JTAG BYPASSING
HW CONFIG
74VCX08M
Quad AND Gates
Leds Green 90 deg. under the Combo
PHY_ADDRESS[4..0] : 01000
ENA_PAUSE : 0 (disable)
ANEG[3..0] : 1110 (Advertize)
ENA_XC : 1 (CrossOver Enable)
DIS : 0 (125Mhz generation Enable)
HWCFG_MODE[3..0] : 1111 (GMII -> Copper)
DIS_FC : 1 (Copper/Fiber Auto Select)
DIS_SLEEP : 1 (Disable Energy detect)
SEL_BDT : 0 (Use MDC/MDIO I/F)
INT_POL : 0 (Interrupt Active low)
75/50 Ohm : 0 (50 Ohm fiber)
GALILEO TECHNOLOGY - A MARVELL COMPANY
Board Name: EV64340_60BP
SIZE B
REV 2.1
File Name: GIGA0
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

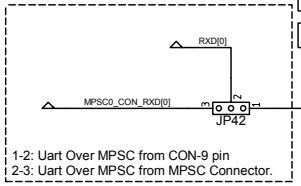

G1_TXD[7..0]
G1_TX_CLKOUT
G1_TX_ERR
G1_TX_EN
MDIO
MDC
CLK_25_G1
TDO_TO_G1
TMS
TRST~
TCK
SYS_RST[1]~
AVDDH1
DVDDL1
3.3V filtered.
1.5V
FB60ohm25%1.5A1210
3.3V filtered.
2.5V filtering
G1_INT~
G1_COL
GIGA_TDO
G1_RXD[7..0]
G1_TX_CLK
G1_RX_ERR
G1_RX_DV
G1_RX_CLK
U16
88E1011S-RCJ
1X1 GMII COMBO Connector
CON19 G1_COP
Fine Tuning
place close to XCVR
HFBR-5912E-850NM
Fiber-Transceiver
SERDES Interface
3.3V filtering
1.8V filtering
PHY1 JTAG BYPASSING
HW CONFIG
74VCX08M
Quad AND Gates
Leds Green 90 deg.
under the Combo
PHY_ADDRESS[4..0] : 01001
ENA_PAUSE : 0 (disable)
ANEG[3..0] : 1110 (Advertize)
ENA_XC : 1 (CrossOver Enable)
DIS : 0 (125Mhz generation Enable)
HWCFG_MODE[3..0] : 1111 (GMII -> Copper)
DIS_FC : 0 (Copper/Fiber Auto Select)
DIS_SLEEP : 1 (Disable Energy detect)
SEL_BDT : 0 (Use MDC/MDIO I/F)
INT_POL : 0 (Interrupt Active low)
75/50 Ohm : 0 (50 Ohm fiber)
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
Board Name: EV64340_60BP
REV 2.1
File Name: GIGA1
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

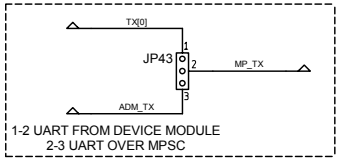


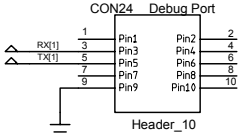


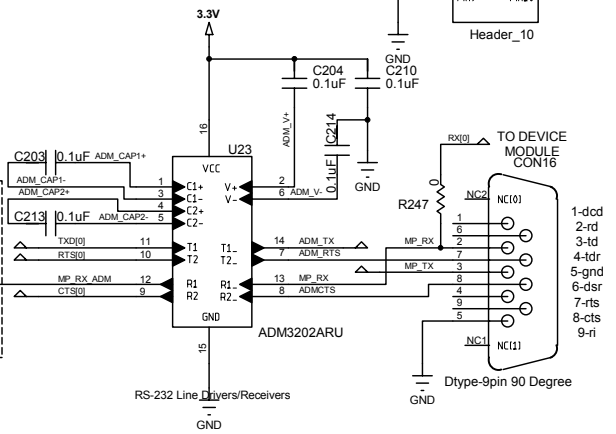






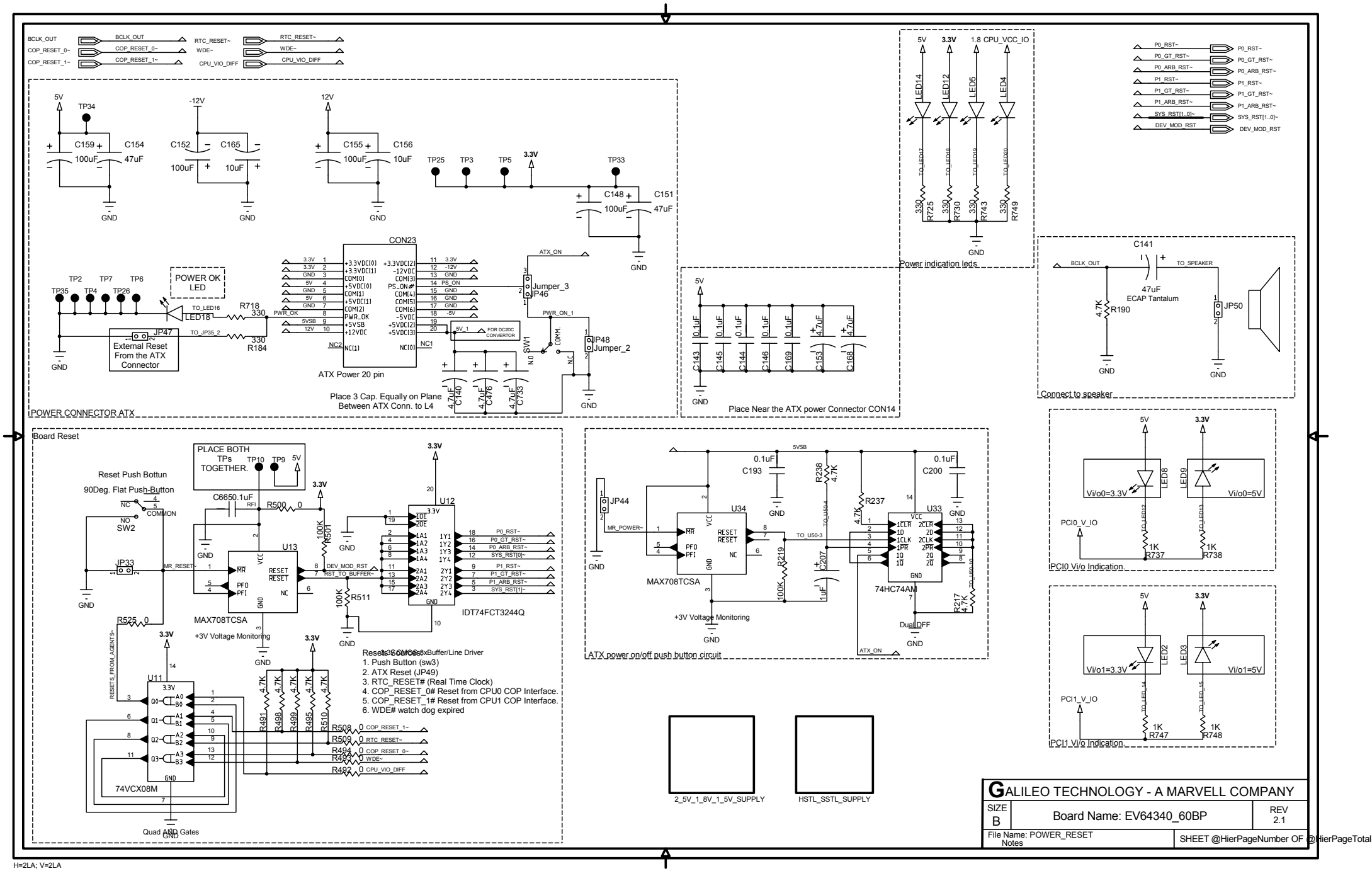


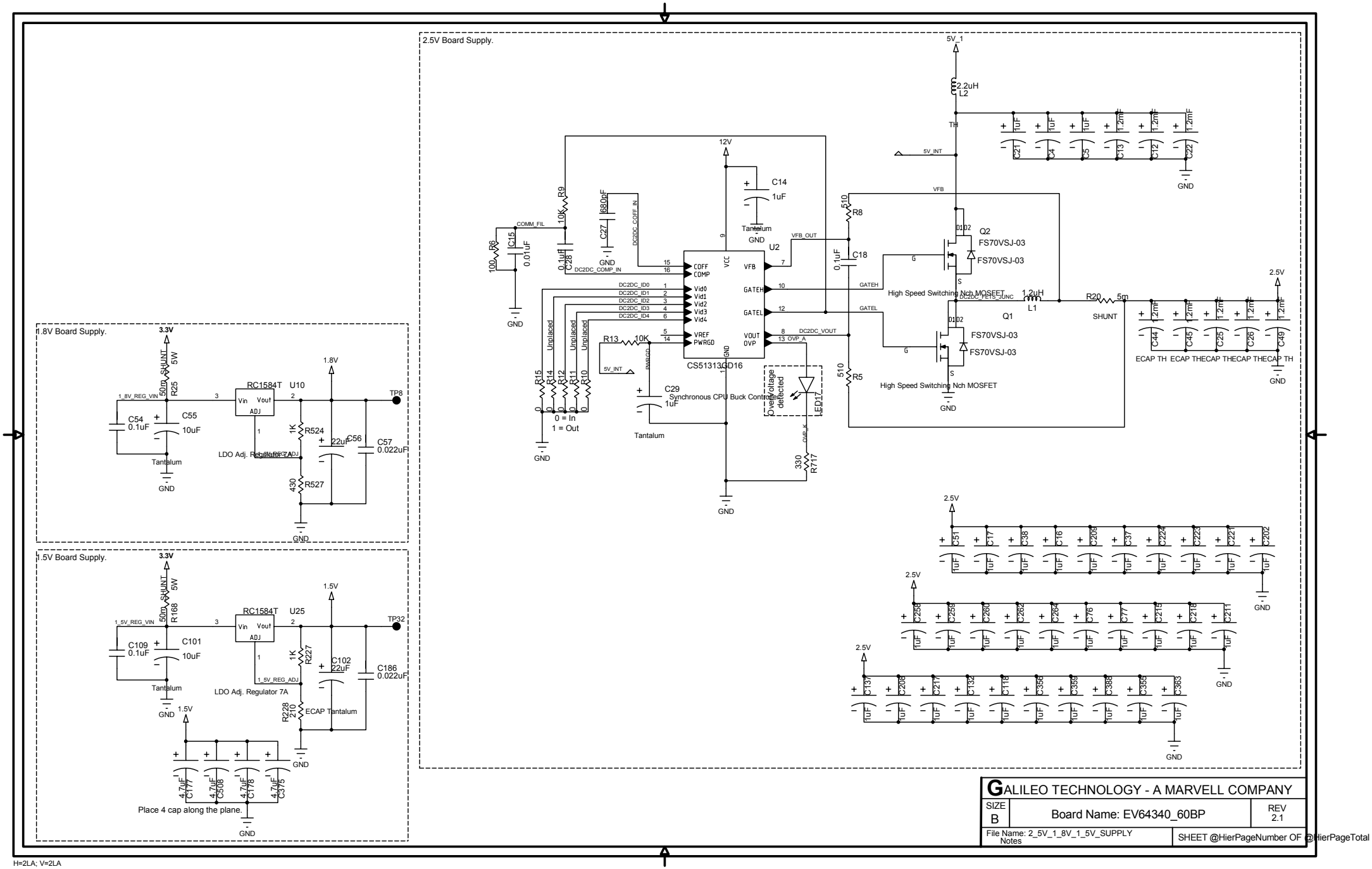




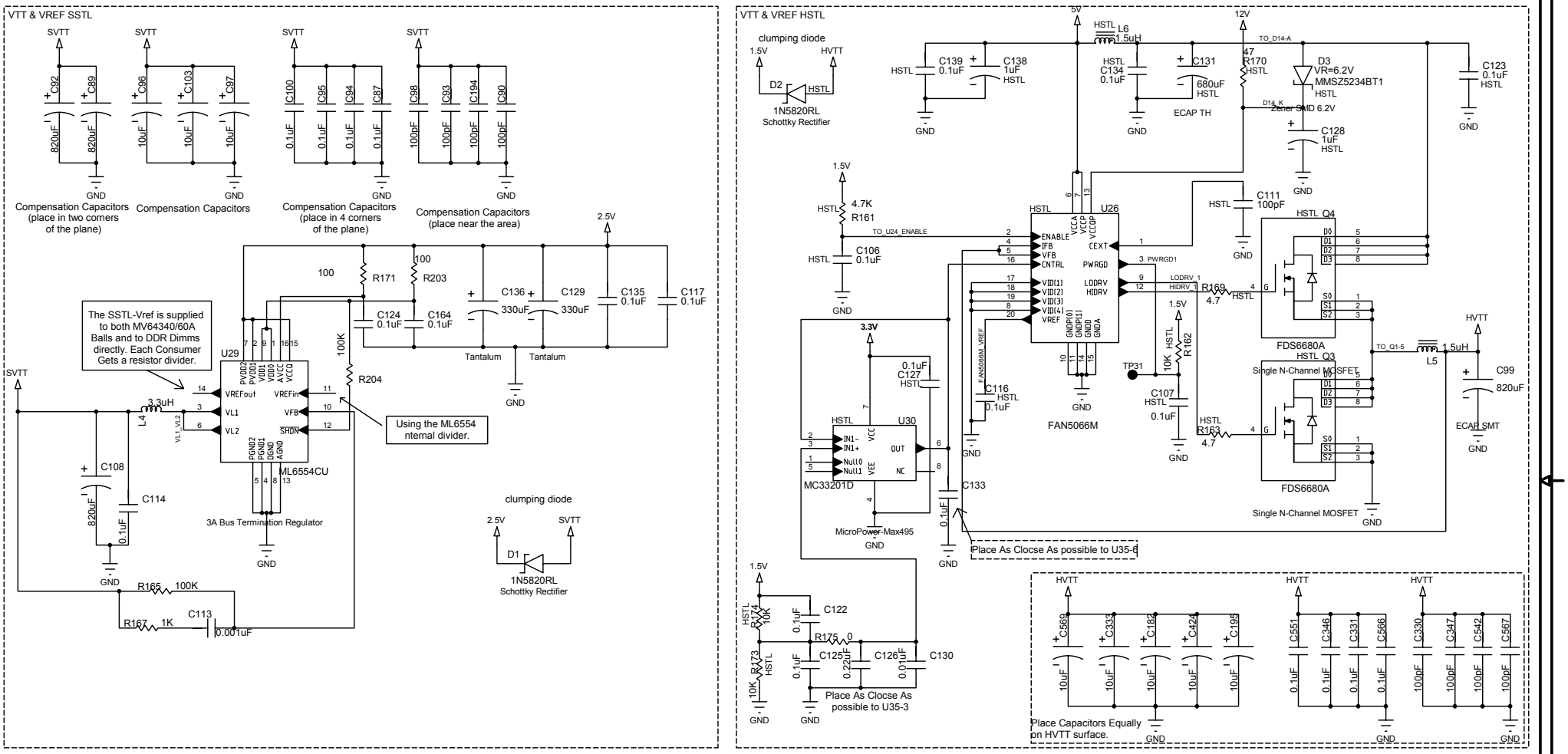
GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	Board Name: EV64340_60BP	REV 2.1
File Name: 2_MPSC_CONNECTORS_UART Notes	SHEET @HierPageNumber OF @HierPageTotal	

H=2LA; V=2LA


BCLK_OUT
COP_RESET_0~
COP_RESET_1~
RTC_RESET~
WDE~
CPU_VIO_DIFF
POWER CONNECTOR ATX
5V
-12V
12V
3.3V
TP34
TP25
TP3
TP5
TP33
C159
C154
C152
C165
C155
C156
C148
C151
100uF
47uF
10uF
GND
CON23
ATX Power 20 pin
Place 3 Cap. Equally on Plane
Between ATX Conn. to L4
ATX_ON
Jumper_3
JP46
PWR_ON_1
JP48
Jumper_2
SW1
FOR DC2DC CONVERTOR
TP2
TP7
TP6
TP35
TP4
TP26
POWER OK LED
LED18
TO_LED16
R718
330
PWR_OK
JP47
External Reset From the ATX Connector
TO_JP35_2
R184
C140
C476
C733
Power indication leds
LED14
LED12
LED5
LED4
TO_LED17
TO_LED18
TO_LED19
TO_LED20
R725
R730
R743
R749
1.8 CPU_VCC_IO
Place Near the ATX power Connector CON14
C143
C145
C144
C146
C169
C153
C168
0.1uF
4.7uF
C141
BCLK_OUT
TO_SPEAKER
47uF
ECAP Tantalum
4.7K
R190
JP50
Connect to speaker
P0_RST~
P0_GT_RST~
P0_ARB_RST~
P1_RST~
P1_GT_RST~
P1_ARB_RST~
SYS_RST[1..0]~
DEV_MOD_RST
Board Reset
PLACE BOTH TPs TOGETHER.
TP10
TP9
Reset Push Bottun
90Deg. Flat Push-Button
NC
COMMON
NO
SW2
JP33
MR_RESET~
C665
0.1uF
RFI
R500
0
100K
R501
U13
MAX708TCSA
+3V Voltage Monitoring
DEV_MOD_RST
RST_TO_BUFFER~
R511
U12
IDT74FCT3244Q
P0_RST~
P0_GT_RST~
P0_ARB_RST~
SYS_RST[0]~
P1_RST~
P1_GT_RST~
P1_ARB_RST~
SYS_RST[1]~
R525
RESETS_FROM_AGENTS~
U11
74VCX08M
Quad AND Gates
R491
R498
R499
R495
R510
4.7K
R508
R509
R494
R492
COP_RESET_1~
RTC_RESET~
COP_RESET_0~
WDE~
CPU_VIO_DIFF
Reset Control
1. Push Button (sw3)
2. ATX Reset (JP49)
3. RTC_RESET# (Real Time Clock)
4. COP_RESET_0# Reset from CPU0 COP Interface.
5. COP_RESET_1# Reset from CPU1 COP Interface.
6. WDE# watch dog expired
ATX power on/off push button circuit
JP44
MR_POWER~
5VSB
C193
C200
R238
4.7K
R237
U34
U33
MAX708TCSA
74HC74AM
Dual DFF
+3V Voltage Monitoring
R219
100K
C207
1uF
R217
TO_U50-3
TO_U50-4
TO_U50-10
ATX_ON
PCI0_V_IO
Vi/o0=3.3V
Vi/o0=5V
LED8
LED9
TO_LED12
TO_LED13
R737
R738
1K
PCI0 Vi/o Indication
PCI1_V_IO
Vi/o1=3.3V
Vi/o1=5V
LED2
LED3
TO_LED_14
TO_LED_15
R747
R748
PCI1 Vi/o Indication
2_5V_1_8V_1_5V_SUPPLY
HSTL_SSTL_SUPPLY
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE
B
Board Name: EV64340_60BP
REV
2.1
File Name: POWER_RESET
Notes
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA

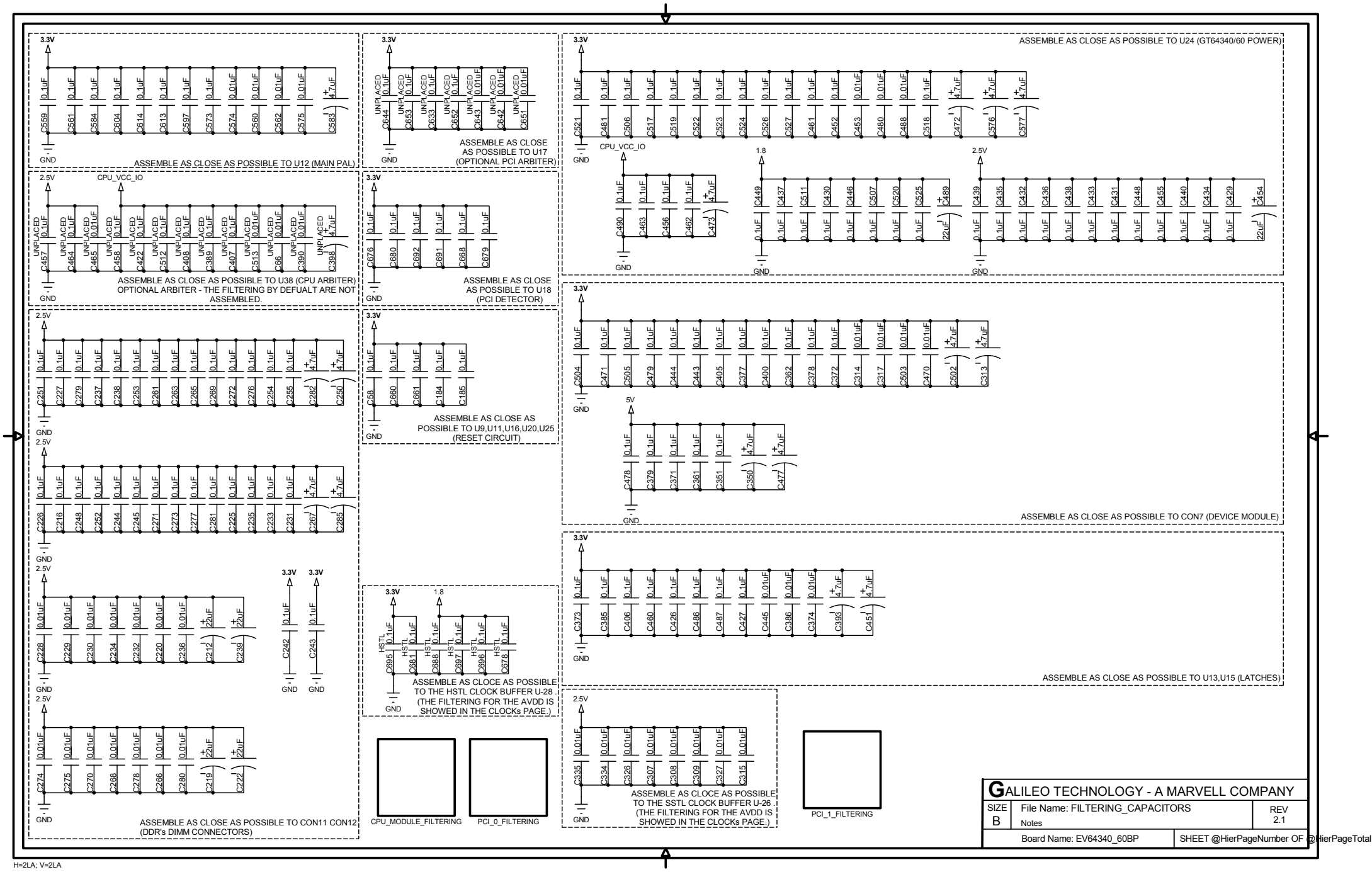

2.5V Board Supply.
1.8V Board Supply.
1.5V Board Supply.
3.3V
1.8V
1.5V
12V
5V_1
2.2uH
L2
1.2uH
L1
CS51313GD16
Synchronous CPU Buck Controller
High Speed Switching Nch MOSFET
FS70VSJ-03
RC1584T
LDO Adj. Regulator 7A
ECAP Tantalum
Tantalum
GND
SHUNT
Place 4 cap along the plane.
0 = In
1 = Out
Overvoltage detected
ECAP TH
THECAP
Board Name: EV64340_60BP
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
REV 2.1
File Name: 2_5V_1_8V_1_5V_SUPPLY
Notes
SHEET @HierPageNumber OF @HierPageTotal

H=2LA; V=2LA

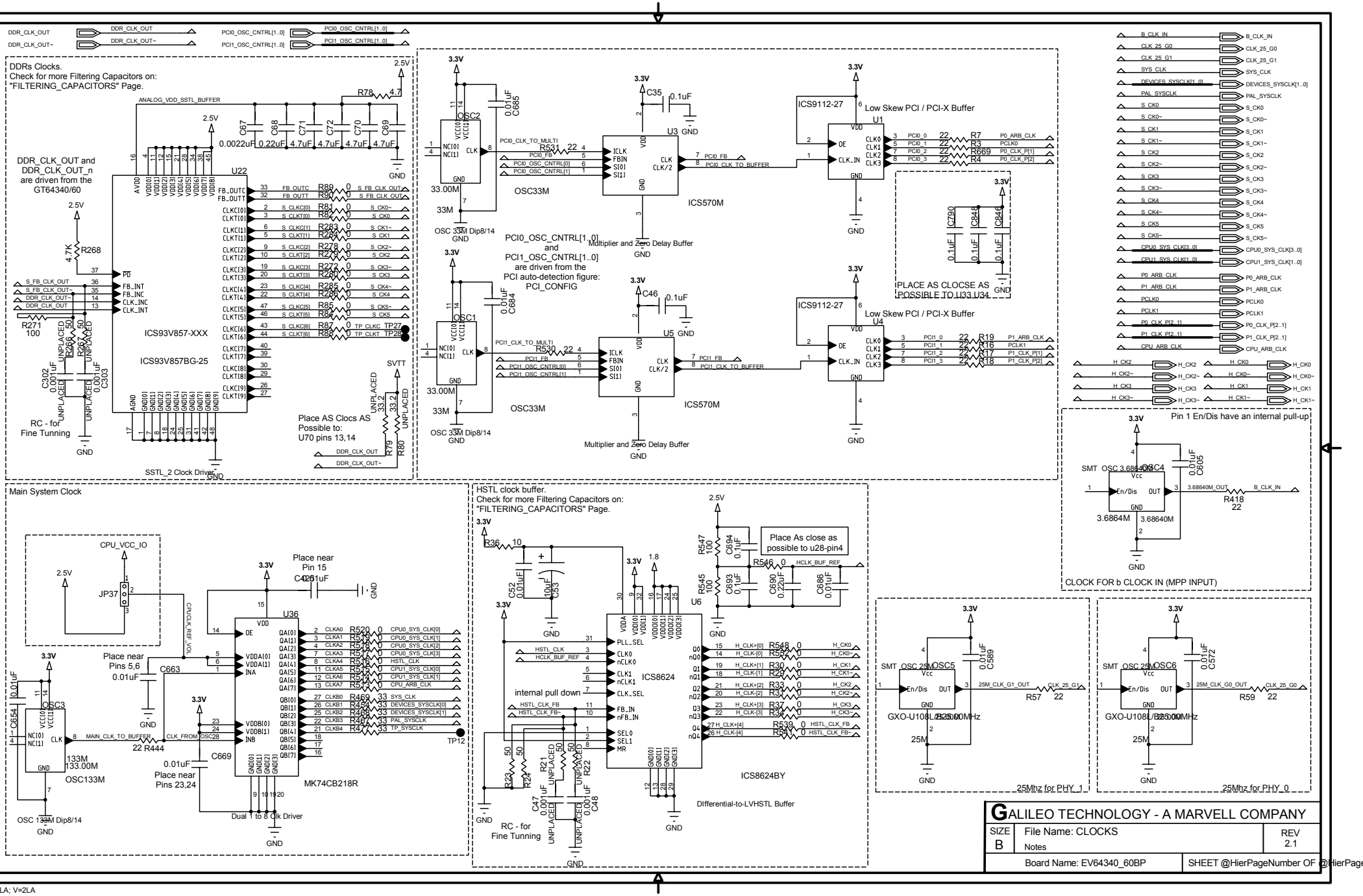


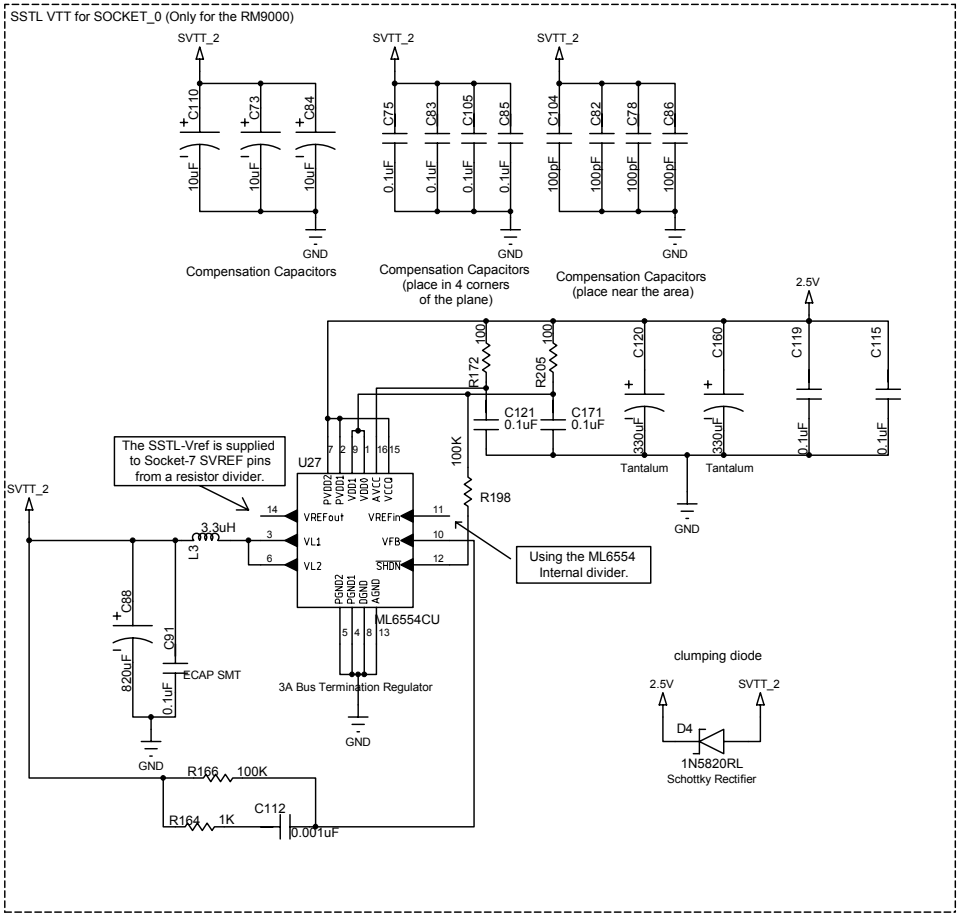
GALILEO TECHNOLOGY		
SIZE B	Board Name: EV64340_60BP	REV 2.1
File Name: HSTL_SSTL_SUPPLY Notes	SHEET @HierPageNumber OF @HierPageTotal	

H=2LA; V=2LA


3.3V
0.1uF
C559
C561
C584
C604
C614
C613
C597
C573
C574
C560
C562
C575
0.01uF
4.7uF
C583
GND
ASSEMBLE AS CLOSE AS POSSIBLE TO U12 (MAIN PAL)
UNPLACED
C644
C653
C633
C652
C643
C642
C651
ASSEMBLE AS CLOSE AS POSSIBLE TO U17 (OPTIONAL PCI ARBITER)
ASSEMBLE AS CLOSE AS POSSIBLE TO U24 (GT64340/60 POWER)
C521
C481
C506
C517
C519
C522
C523
C524
C526
C527
C461
C452
C453
C480
C488
C518
C472
C576
C577
CPU_VCC_IO
C490
C463
C456
C462
C473
1.8
C449
C437
C511
C430
C446
C507
C520
C525
C489
22uF
2.5V
C439
C435
C432
C436
C438
C433
C431
C448
C455
C440
C434
C429
C454
2.5V
CPU_VCC_IO
C457
C464
C465
C458
C422
C512
C408
C389
C407
C513
C66
C390
C398
ASSEMBLE AS CLOSE AS POSSIBLE TO U38 (CPU ARBITER)
OPTIONAL ARBITER - THE FILTERING BY DEFUALT ARE NOT ASSEMBLED.
C676
C680
C692
C691
C668
C679
ASSEMBLE AS CLOSE AS POSSIBLE TO U18 (PCI DETECTOR)
C504
C471
C505
C479
C444
C443
C405
C377
C400
C362
C378
C372
C314
C317
C503
C470
C502
C313
5V
C478
C379
C371
C361
C351
C350
C477
ASSEMBLE AS CLOSE AS POSSIBLE TO CON7 (DEVICE MODULE)
C251
C227
C279
C237
C238
C253
C261
C263
C265
C269
C272
C276
C254
C255
C282
C250
C58
C660
C661
C184
C185
ASSEMBLE AS CLOSE AS POSSIBLE TO U9,U11,U16,U20,U25 (RESET CIRCUIT)
C226
C216
C248
C252
C244
C245
C271
C273
C277
C281
C225
C235
C233
C231
C267
C285
C228
C229
C230
C234
C232
C220
C236
C212
C239
C242
C243
C274
C275
C270
C268
C278
C266
C280
C219
C222
ASSEMBLE AS CLOSE AS POSSIBLE TO CON11 CON12 (DDR's DIMM CONNECTORS)
1.8
HSTL
C695
C681
C688
C697
C696
C678
ASSEMBLE AS CLOCE AS POSSIBLE TO THE HSTL CLOCK BUFFER U-28 (THE FILTERING FOR THE AVDD IS SHOWED IN THE CLOCKs PAGE.)
C373
C385
C406
C460
C426
C486
C487
C427
C445
C386
C374
C393
C451
ASSEMBLE AS CLOSE AS POSSIBLE TO U13,U15 (LATCHES)
C335
C334
C326
C307
C308
C309
C327
C315
ASSEMBLE AS CLOCE AS POSSIBLE TO THE SSTL CLOCK BUFFER U-26 (THE FILTERING FOR THE AVDD IS SHOWED IN THE CLOCKs PAGE.)
CPU_MODULE_FILTERING
PCI_0_FILTERING
PCI_1_FILTERING
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
File Name: FILTERING_CAPACITORS
Notes
REV 2.1
Board Name: EV64340_60BP
SHEET @HierPageNumber OF @HierPageTotal

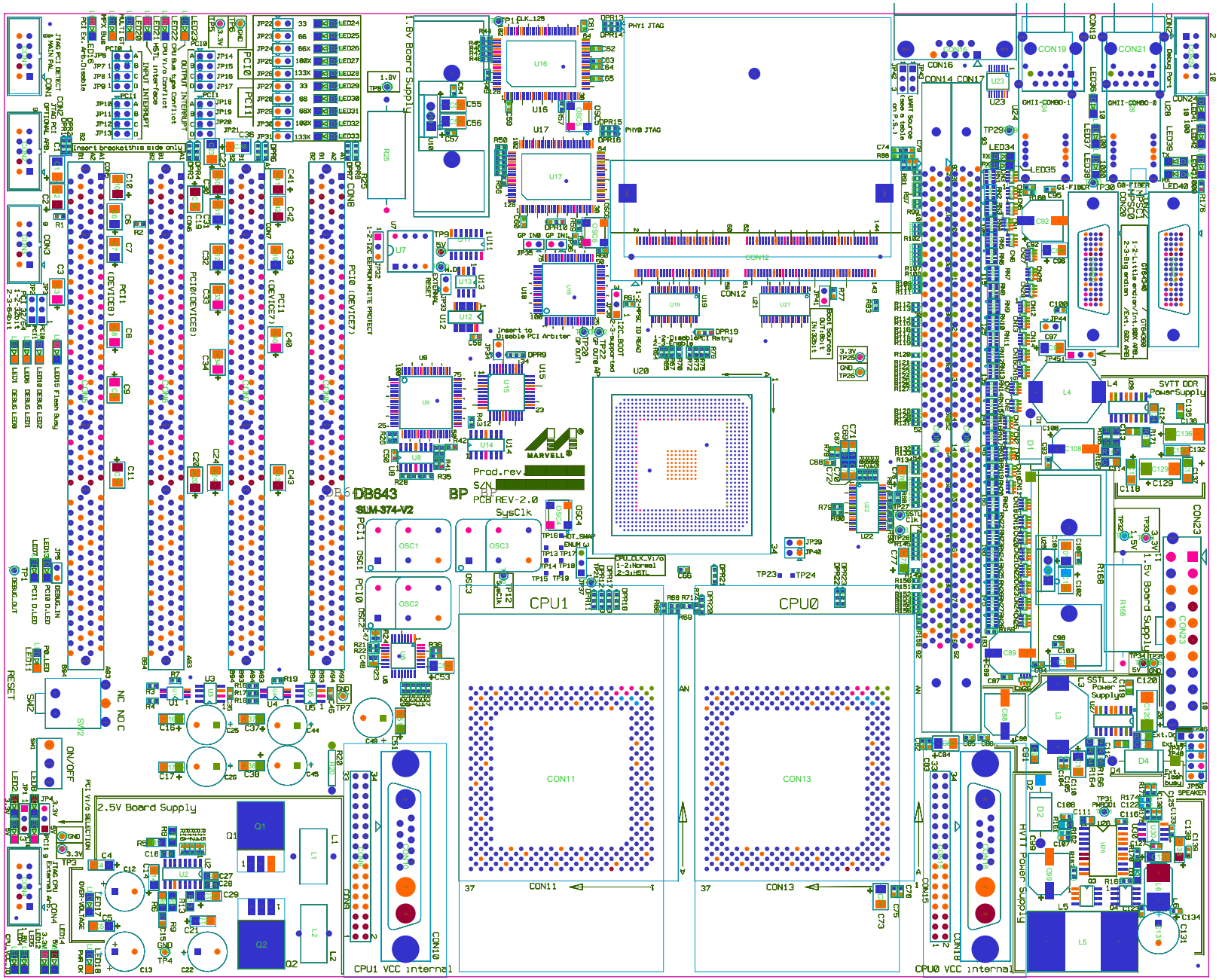
H=2LA; V=2LA


DDR_CLK_OUT
DDR_CLK_OUT~
PCI0_OSC_CNTRL[1..0]
PCI1_OSC_CNTRL[1..0]
DDRs Clocks.
Check for more Filtering Capacitors on:
"FILTERING_CAPACITORS" Page.
ANALOG_VDD_SSTL_BUFFER
DDR_CLK_OUT and
DDR_CLK_OUT_n
are driven from the
GT64340/60
ICS93V857-XXX
ICS93V857BG-25
SSTL_2 Clock Driver
Place AS Clocs AS
Possible to:
U70 pins 13,14
RC - for
Fine Tunning
OSC2
OSC1
OSC33M
OSC 33M Dip8/14
ICS9112-27
Low Skew PCI / PCI-X Buffer
ICS570M
Multiplier and Zero Delay Buffer
PCI0_OSC_CNTRL[1..0]
and
PCI1_OSC_CNTRL[1..0]
are driven from the
PCI auto-detection figure:
PCI_CONFIG
PLACE AS CLOCSE AS
POSSIBLE TO U33,U34
B_CLK_IN
CLK_25_G0
CLK_25_G1
SYS_CLK
DEVICES_SYSCLK[1..0]
PAL_SYSCLK
S_CK0
S_CK0~
S_CK1
S_CK1~
S_CK2
S_CK2~
S_CK3
S_CK3~
S_CK4
S_CK4~
S_CK5
S_CK5~
CPU0_SYS_CLK[3..0]
CPU1_SYS_CLK[1..0]
P0_ARB_CLK
P1_ARB_CLK
PCLK0
PCLK1
P0_CLK_P[2..1]
P1_CLK_P[2..1]
CPU_ARB_CLK
Pin 1 En/Dis have an internal pull-up
SMT OSC 3.6864
OSC4
3.6864M
3.68640M
3.68640M_OUT
CLOCK FOR b CLOCK IN (MPP INPUT)
Main System Clock
CPU_VCC_IO
JP37
Place near
Pins 5,6
Place near
Pin 15
MK74CB218R
Dual 1 to 8 Clk Driver
133M
133.00M
OSC133M
HSTL clock buffer.
Check for more Filtering Capacitors on:
"FILTERING_CAPACITORS" Page.
Place As close as
possible to u28-pin4
internal pull down
ICS8624
ICS8624BY
DIfferential-to-LVHSTL Buffer
SMT OSC 25M
OSC5
OSC6
GXO-U108L/25.000MHz
25M
25Mhz for PHY_1
25Mhz for PHY_0
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE
B
File Name: CLOCKS
Notes
REV
2.1
Board Name: EV64340_60BP
SHEET @HierPageNumber OF @HierPageTotal
H=2LA; V=2LA



GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	File Name: SSTL_VTT_SOCKET_0 Notes	REV 2.1
	Board Name: EV64340_60BP	SHEET @HierPageNumber OF @HierPageTotal

H=2LA; V=2LA


DB643
SLM-374-V2
PCB REV-2.0
BP
CPU1
CPU0
MARVELL
2.5V Board Supply
1.5V Board Supply
SVTT DDR PowerSupply
HVTT Power Supply
SSTL-2 Power Supply
CPU1 VCC internal
CPU0 VCC internal
RESET
ON/OFF
SysClk
PHY1 JTAG
PHY0 JTAG
CON11
CON13
CON10
CON18
CON23