SC SV Group - April 29 2002

DB-IBM750FX-S7 Schematic

Revision 1.0 29/04/2002

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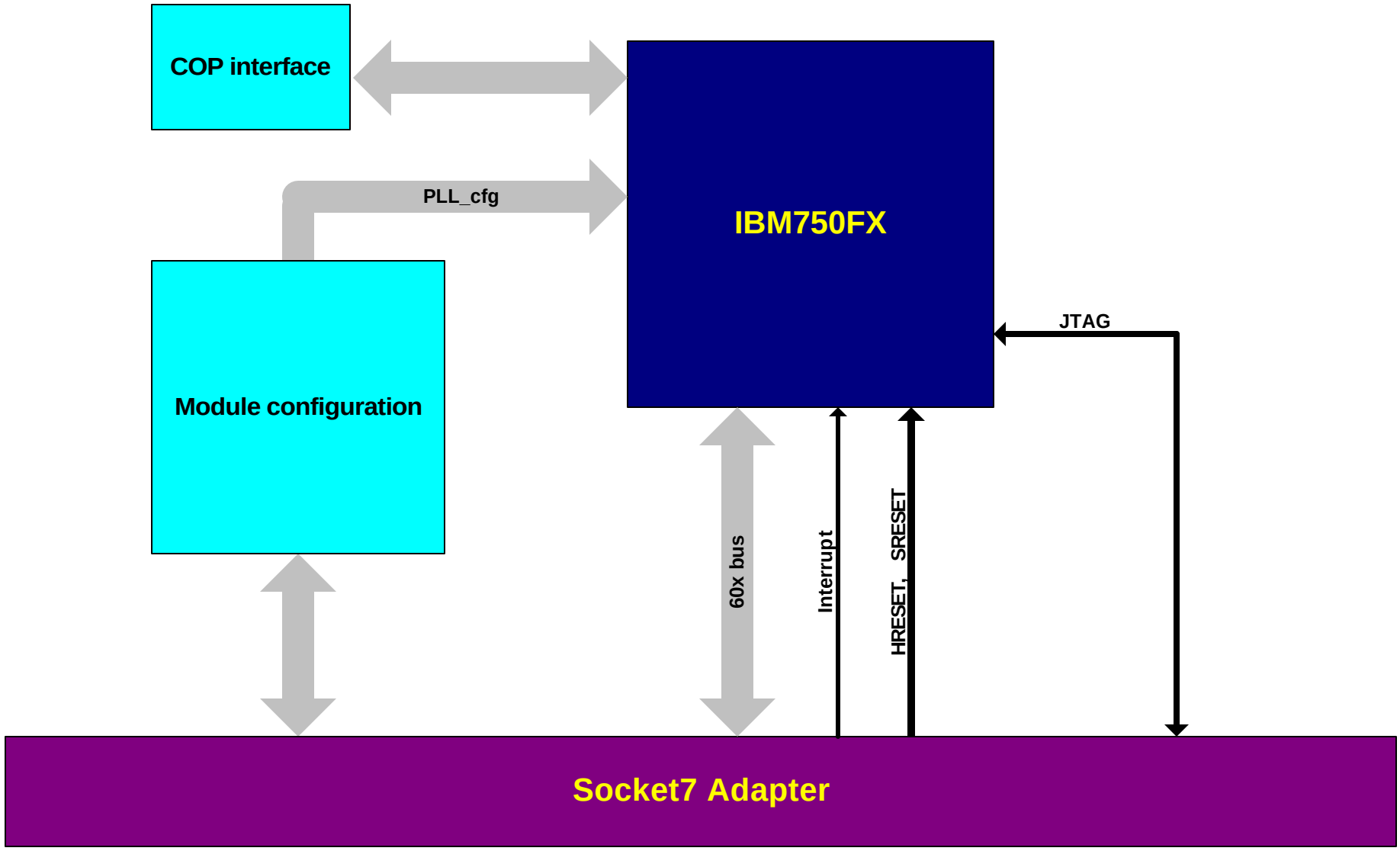
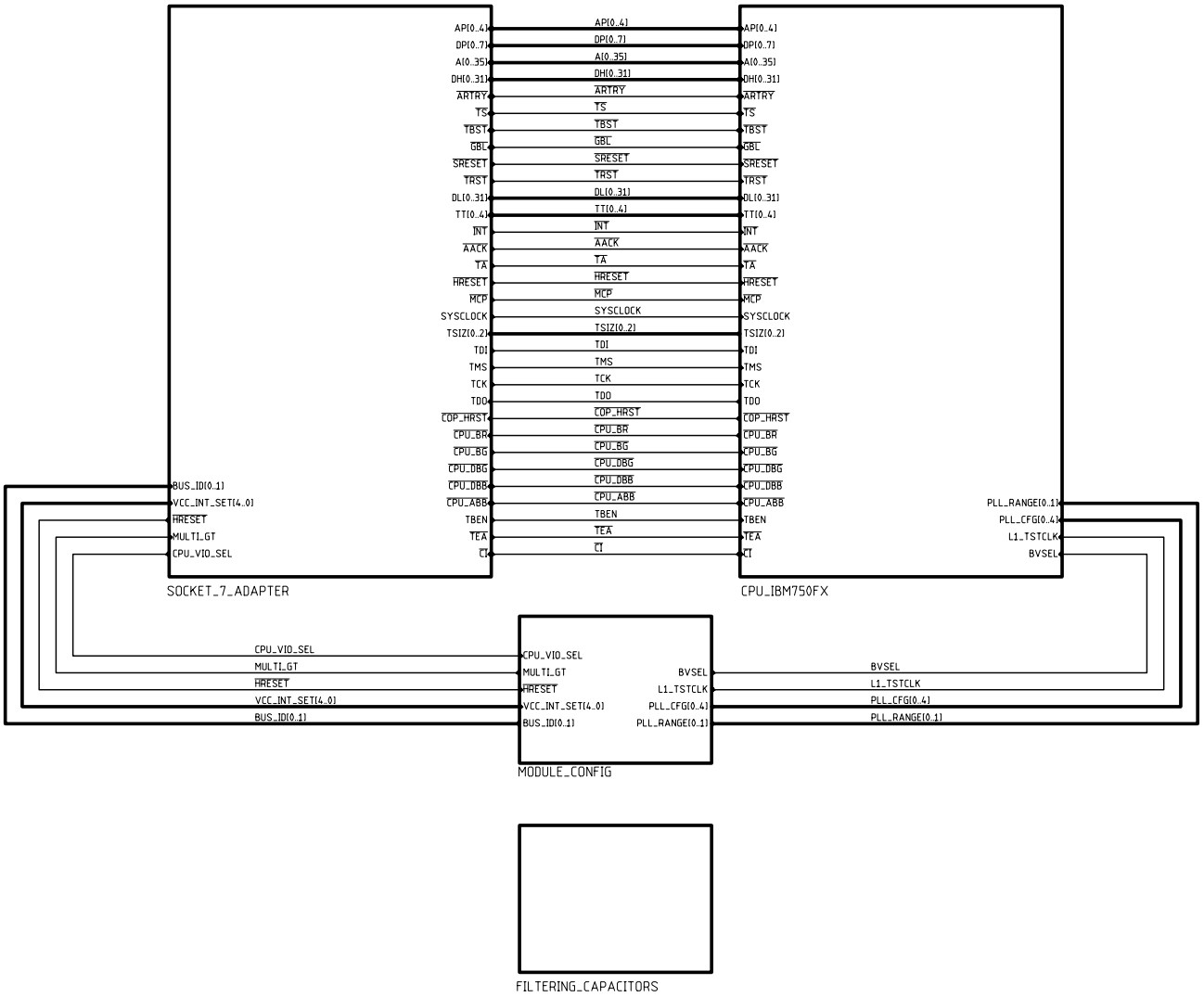
DB-IBM750FX-S7

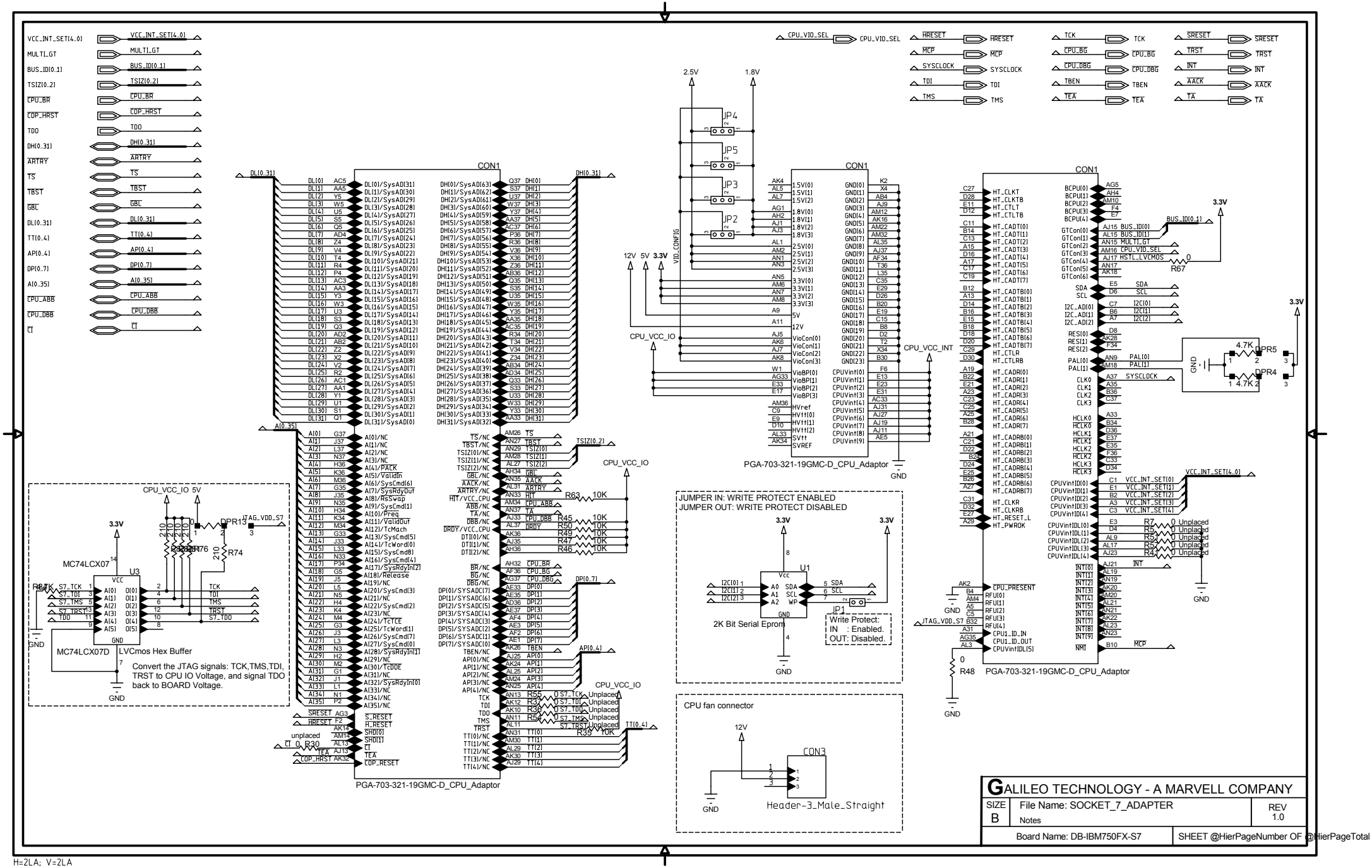




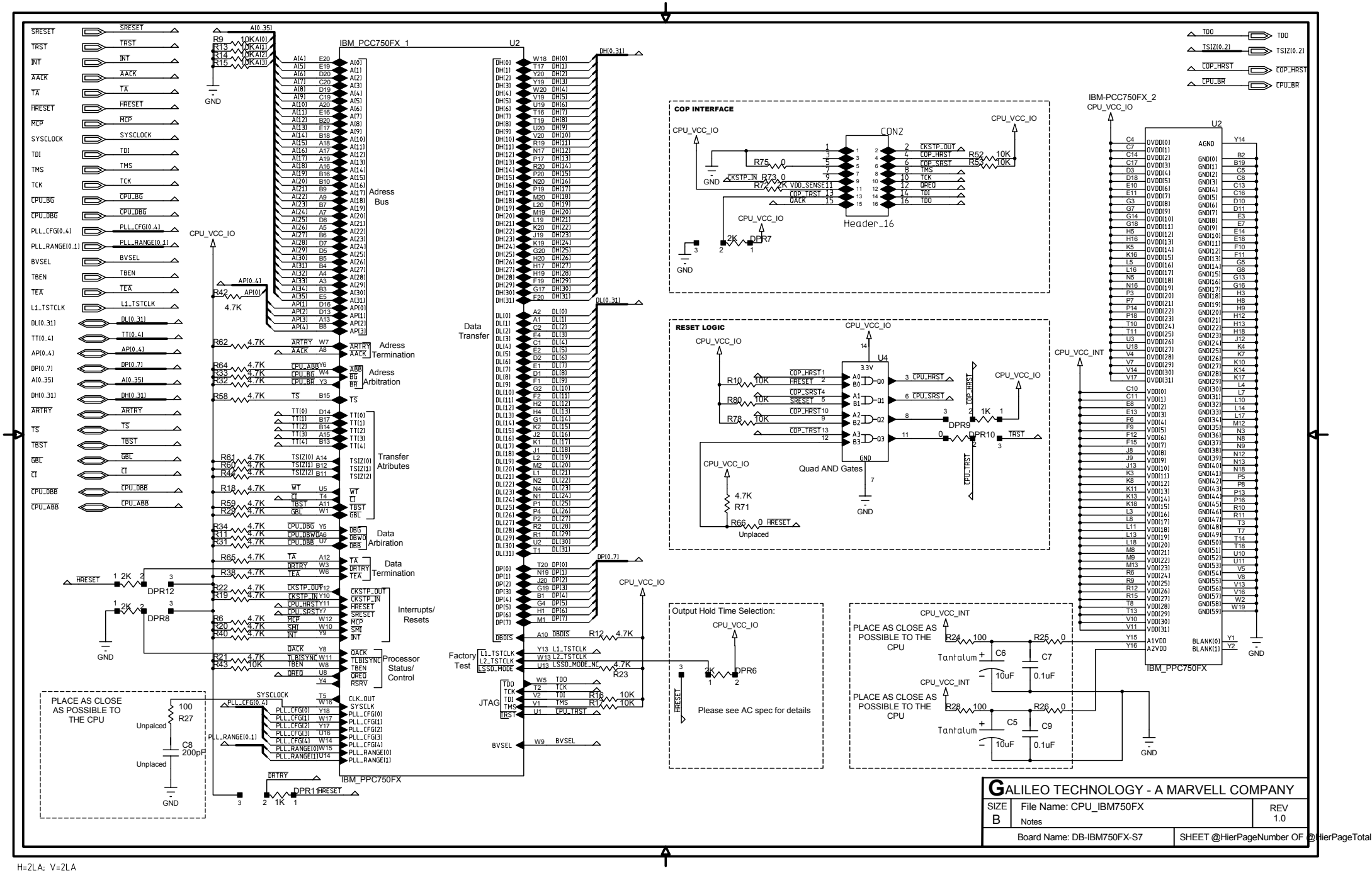
GALILEO TECHNOLOGY - A MARVELL COMPANY

SIZE	File Name: top	REV
B	Notes	1.0
Board Name: DB-IBM750FX-S7	SHEET @HierPageNumber OF @HierPageTotal	

H=2LA; V=2LA


VCC_INT_SET[4..0]
MULTI_GT
BUS_ID[0..1]
TSIZ[0..2]
CPU_BR
COP_HRST
TDO
DH[0..31]
ARTRY
TS
TBST
GBL
DL[0..31]
TT[0..4]
AP[0..4]
DP[0..7]
A[0..35]
CPU_ABB
CPU_DBB
CI
CPU_VIO_SEL
HRESET
MCP
SYSCLOCK
TDI
TMS
TCK
CPU_BG
CPU_DBG
TBEN
TEA
SRESET
TRST
INT
AACK
TA
CON1
PGA-703-321-19GMC-D_CPU_Adaptor
JP4
JP5
JP3
JP2
VID_CONFIG
2.5V
1.8V
12V
5V
3.3V
CPU_VCC_IO
CPU_VCC_INT
JUMPER IN: WRITE PROTECT ENABLED
JUMPER OUT: WRITE PROTECT DISABLED
2K Bit Serial Eprom
Write Protect:
IN : Enabled.
OUT: Disabled.
CPU fan connector
Header-3_Male_Straight
MC74LCX07
MC74LCX07D
LVCmos Hex Buffer
Convert the JTAG signals: TCK,TMS,TDI, TRST to CPU IO Voltage, and signal TDO back to BOARD Voltage.
JTAG_VDD_S7
GND
R63 10K
R45 10K
R50 10K
R49 10K
R47 10K
R46 10K
R56 0 S7_TCK Unplaced
R57 0 S7_TDI Unplaced
R58 0 S7_TMS Unplaced
R54 S7_TRST Unplaced
R38 10K
R67 0
R48 0
R7 0 Unplaced
R5 0 Unplaced
R51 0 Unplaced
R52 0 Unplaced
R4 0 Unplaced
DPR5 4.7K
DPR4 4.7K
R30 0 unplaced
GALILEO TECHNOLOGY - A MARVELL COMPANY
SIZE B
File Name: SOCKET_7_ADAPTER
Notes
REV 1.0
Board Name: DB-IBM750FX-S7
SHEET @HierPageNumber OF @HierPageTotal

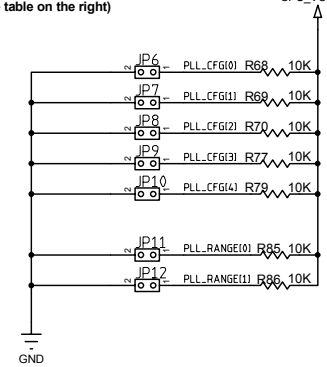
H=2LA; V=2LA


IBM_PCC750FX_1
U2
IBM-PCC750FX_2
IBM_PPC750FX
Adress Bus
Adress Termination
Adress Arbitration
Transfer Atributes
Data Arbiration
Data Termination
Interrupts/ Resets
Processor Status/ Control
Data Transfer
Factory Test
JTAG
COP INTERFACE
CON2
Header_16
RESET LOGIC
Quad AND Gates
Output Hold Time Selection:
Please see AC spec for details
PLACE AS CLOSE AS POSSIBLE TO THE CPU
PLACE AS CLOSE AS POSSIBLE TO THE CPU
PLACE AS CLOSE AS POSSIBLE TO THE CPU
GALILEO TECHNOLOGY - A MARVELL COMPANY
File Name: CPU_IBM750FX
Notes
REV 1.0
Board Name: DB-IBM750FX-S7
SHEET @HierPageNumber OF @HierPageTotal

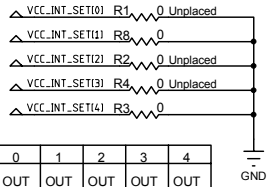
H=2LA; V=2LA

VCC_INT_SET[4..0] VCC_INT_SET[4..0]
HRESET HRESET
CPU_VIO_SEL CPU_VIO_SEL

750FX PLL configuration (see table on the right)

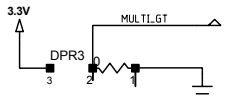


CPU internal Voltage selection (VccInt)



VccInt	0	1	2	3	4
1.2V	OUT	OUT	OUT	OUT	OUT
1.3V	OUT	OUT	OUT	OUT	IN
1.4V	OUT	IN	OUT	OUT	IN

GT's multi GT selection:



1-2: Multi GT disabled
2-3: Multi GT enabled

Table 5-2. 750FX Microprocessor PLL Configuration

PLL_CFG [0:4]		Processor to Bus Frequency Ratio	Frequency Range Supported by VCO having an example range of VCO_{MIN} = 1000 to VCO_{MAX} = 2400MHz[6]			
			SYSCLK		Core	
bin	dec		Min	Max	Min	Max
00000	0	OFF	N/A	N/A	Off	Off
00001	1	OFF	N/A	N/A	Off	Off
00010	2	PLL Bypass[3]	N/A	N/A	N/A	N/A
00011	3	PLL Bypass[3]	N/A	-	N/A	N/A
00100	4	2x[1]	-	-	-	-
00101	5	2.5x[1]	-	-	-	-
00110	6	3x[1]	-	-	-	-
00111	7	3.5x	143	150[5]	500	525
01000	8	4x	125	150[5]	500	600
01001	9	4.5x	111	150[5]	500	675
01010	10	5x	100	150[5]	500	750
01011	11	5.5x	91	150[5]	500	825
01100	12	6x	83	150[5]	500	900
01101	13	6.5x	77	150[5]	500	975
01110	14	7x	71	142	500	1000
01111	15	7.5x	66	133	500	1000
10000	16	8x	63	125	500	1000
10001	17	8.5x	59	118	500	1000
10010	18	9x	55	111	500	1000
10011	19	9.5x	52	105	500	1000
10100	20	10x	50	100	500	1000
10101	21	11x	45[2]	91	500	1000
10110	22	12x	41[2]	83	500	1000
10111	23	13x	38[2]	77	500	1000
11000	24	14x	35[2]	71	500	1000
11001	25	15x	33[2]	66	500	1000
11101	29	19x	26[2]	52	500	1000
11110	30	20x	25[2]	50	500	1000
11111	31	Off[4]	N/A	N/A	N/A	N/A

Notes:

1. The 2X- 3X Processor to Bus Ratios are currently not supported.
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see Table 6, "Clock AC Timing Specifications" on page 17 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock - off mode, no clocking occurs inside the 750FX regardless of the SYSCLK input.
5. The SYSCLK limit is 150MHz, as specified in Table 3-6 on page 10. Applications requiring SYSCLK over 150MHz will be investigated by application conditions.
6. The VCO to core clock ratio is 2X for the 750FX. VCO_{MAX} is specified in this table by the maximum core processor speed. The VCO maximum of 2400MHz reflects a processor core speed of 1200MHz, which is not currently supported.

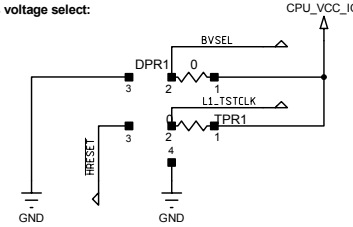
PLL_RANGE[0..1] PLL_RANGE[0..1]
PLL_CFG[0..4] PLL_CFG[0..4]
BVSEL BVSEL
BUS_ID[0..1] BUS_ID[0..1]
L1_TSTCLK L1_TSTCLK
MULTI_GT MULTI_GT

Table 5-1. 750FX Microprocessor PLL Range [0:1] Definitions

PLL_RNG[0:1]	PLL Frequency Range	Notes
10	below 500 MHz	1
00	**500-750 MHz**	
01	750-1200 MHz	1
11	Reserved	1

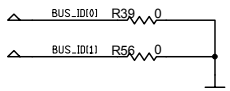
Note:
1. Not supported for DD1.X. **The range bits for DD1.X must be set to 00.**

Bus voltage select:



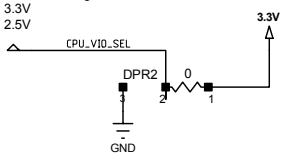
Voltage selection	BVSEL	L1_TSTCLK
Reserved	0	0
1.2, 1.5 or 1.8V	0	1
2.5V	1	1
3.3V	1	0

GT's CPU interface bus mode:



BUS_ID[1..0] selection:
00 - 60x bus
01 - Reserved

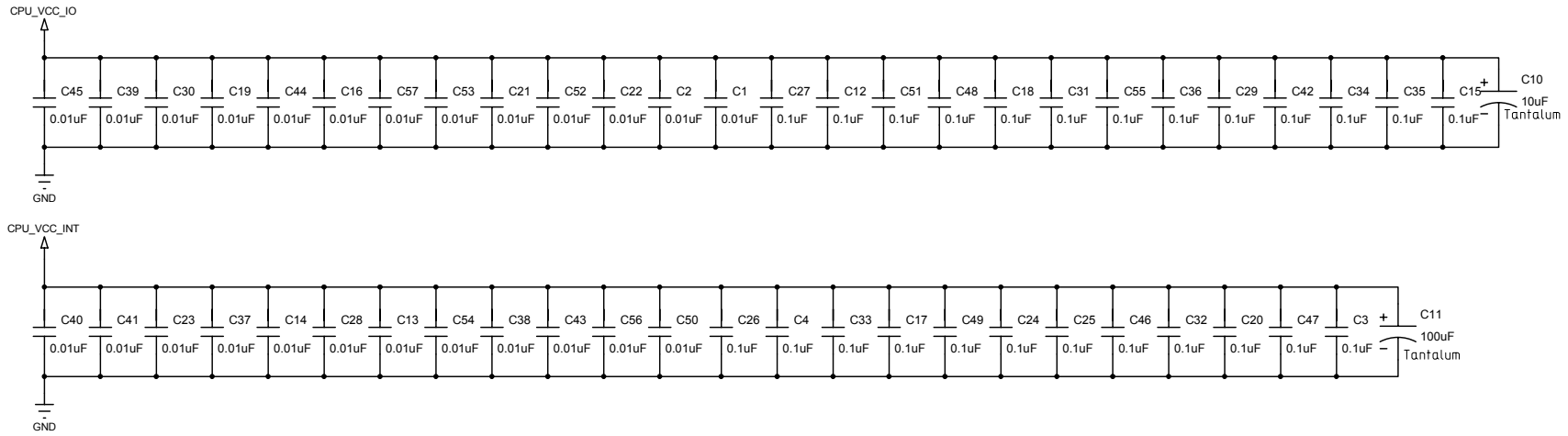
CPU interface voltage select:
1-2: 3.3V
2-3: 2.5V



GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	File Name: MODULE_CONFIG Notes	REV 1.0
Board Name: DB-IBM750FX-S7	SHEET @HierPageNumber OF @HierPageTotal	

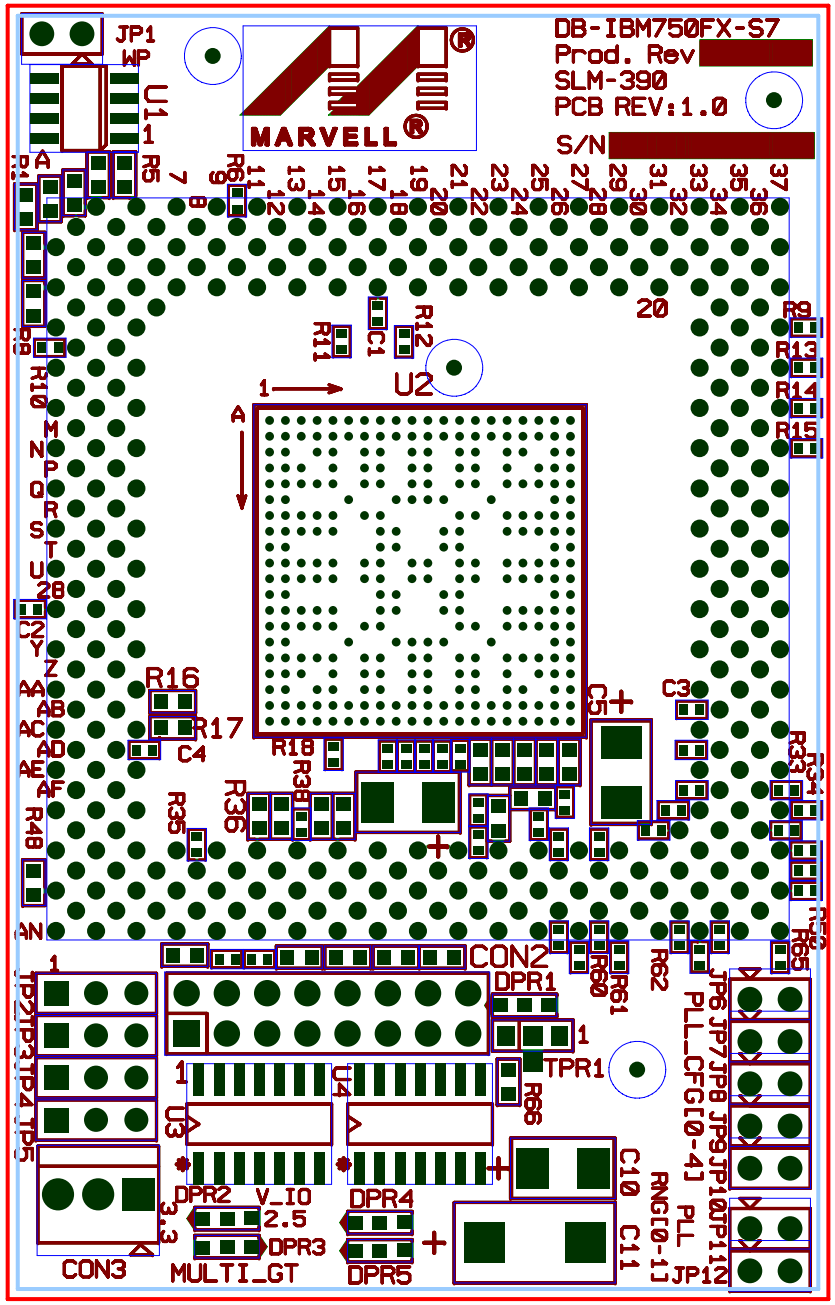
H=2LA; V=2LA

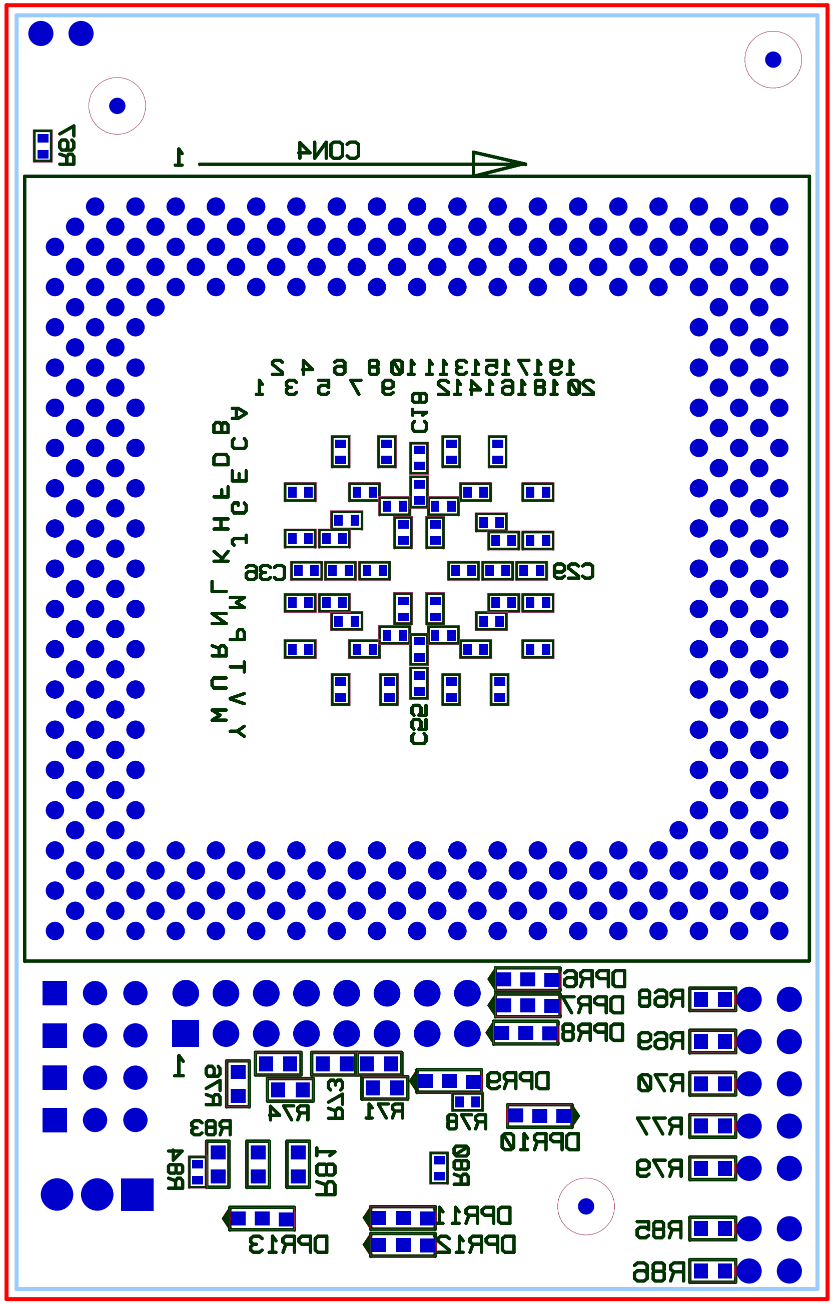
CPU decoupling capacitors, place as close as possible to the CPU



GALILEO TECHNOLOGY - A MARVELL COMPANY		
SIZE B	File Name: FILTERING_CAPACITORS Notes	REV 1.0
Board Name: DB-IBM750FX-S7	SHEET @HierPageNumber OF @HierPageTotal	

H=2LA; V=2LA


DB-IBM750FX-S7
Prod. Rev
SLM-390
PCB REV:1.0
S/N
MARVELL
JP1
WP
U1
R5
R9
R10
R11
C1
R12
R13
R14
R15
U2
R16
R17
C4
R18
C5
C3
R33
R34
R35
R36
R38
R48
CON2
DPR1
TPR1
R60
R61
R62
R65
R66
JP6
JP7
JP8
JP9
JP10
JP11
JP12
PLL_CFG[0-4]
PLL RNG[0-1]
U3
U4
C10
C11
TP2
TP3
TP4
TP5
CON3
DPR2
V_IO
2.5
3.3
DPR3
MULTI_GT
DPR4
DPR5


CON4
R87
C18
C29
C36
C55
DPR6
DPR7
DPR8
DPR9
DPR10
DPR11
DPR12
DPR13
R68
R69
R70
R77
R79
R85
R86
R71
R73
R74
R76
R78
R80
R81
R83
R84