MARVELL®

Marvell SLOT1 CPU Modules
User Guide

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Advanced Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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TABLE OF CONTENTS

List of Tables

List of Figures

1. Introduction

The EV-64240/60-BP and the EV-96132/3 Marvell® Development Boards have a SLOT1 socket that can accommodate various CPU modules.

This document describes the following SLOT 1 CPU modules:

- EV-RM7000A-S1: Section 2
- EV-MPC7400/750-S1: Section 3
- EV-2xMPC7450-S1: Section 4
- EV-IBM750CX-S1: Section 5
- DB-IBM750FX-S1: Section 6
- EV-SR71010A-S1: Section 7

Each module has its own configuration settings when connected to the different Marvell development boards (backplanes).

1.1 Documentation Updates

Marvell may have updated the documentation or software (if any) that was shipped with these modules. See our secure web-site, http://www.marvell.com, for the following information:

- PLD equations
- Assembly map drawings
- Block diagram
- Errata
- Module schematics
- BOM
- Gerber files

1.2 Technical Support

If you have questions or problems with your Marvell boards and devices, contact your local sales representative or FAE. For additional information, see http://www.marvell.com.

2. EV-RM7000A-S1 Module

2.1 Overview

The EV-RM7000A-S1 is a CPU and L3 cache module. This module enables Marvell devices to operate with QED's RM5271 and RM7000A CPUs. The module is designed to plug into the SLOT1 connector designed for it.

Warning

- Make sure you insert the module tightly into the SLOT1 connector. Failure to insert the module correctly could lead to damage to both the module and the board.
- Do not install the EV-RM7000A-S1 into a SLOT1 that is not designated for it.

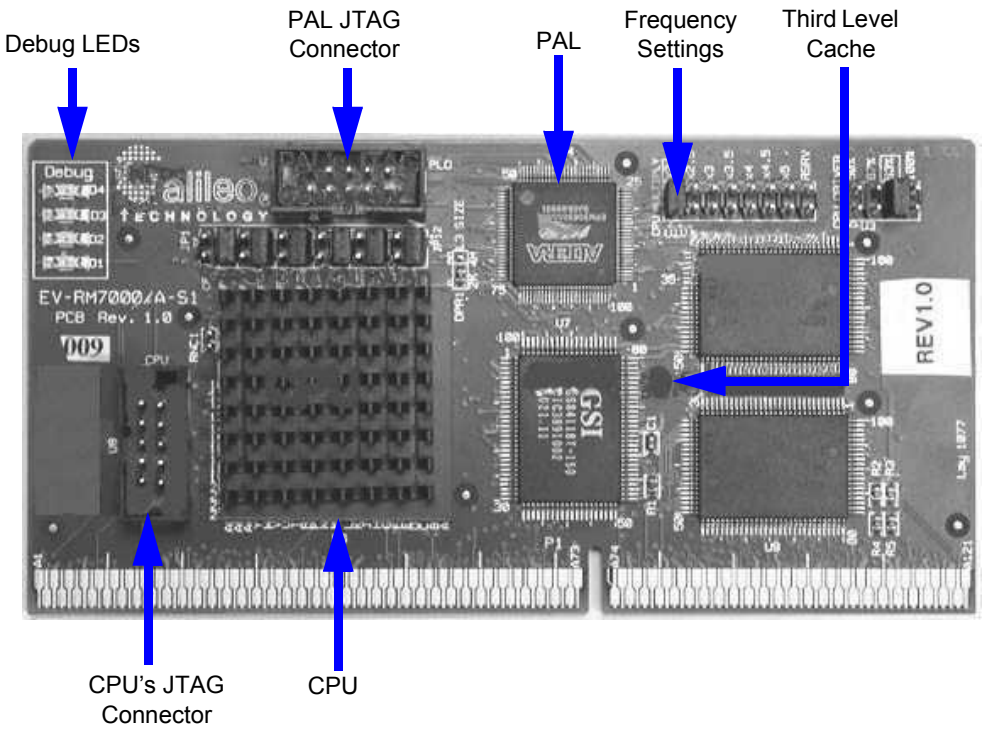
The EV-RM7000A-S1 includes the following features:

- Up to 125 MHz CPU bus frequency
- Optional CPU
  - QED RM7000A
- Onboard L3 cache
  - Supports up to 4 MB of L3 cache
- Configurable jumpers for logic reset
- Reference power supply circuit
  - Support for different CPU voltages

2.2 Description

The EV-RM7000A-S1 module components are illustrated in Figure 1.

Figure 1: EV-RM7000A-S1 Module Components



2.3 EV-RM7000A-S1 Module Jumpers

Table 1 details the EV-RM7000A-S1 module jumpers.

Table 1: EV-RM7000A-S1 Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1 (CFG8)	Out	CPU in Big Endian ordering mode	EndBit: Specifies byte ordering. Logically ordered with the Big Endian signal: In - Little Endian ordering Out - Big Endian ordering
JP2 (CFG10)	In	CPU is R4000 compatible	Determines how non-block writes are handled: In - R4000 compatible Out - Pipelined non-block writes

Table 1: EV-RM7000A-S1 Module Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
JP3 (CFG11)	Out **NOTE**: In – only when using VxWorks.	CPU Timer Interrupt Disabled	TmrIntEn: Disables Timer Interrupt on Int*[5]: In - Timer Interrupt Enabled Out - Timer Interrupt Disabled
JP4 (CFG12)	Out	Enable tertiary cache	Tertiary Cache Interface: In - Disable tertiary cache Out - Enable tertiary cache
JP5 (CFG25)	Out	Enable cache	Enable integrated secondary cache: In - Disable cache Out - Enable cache
JP6 (CFG26)	In	Enable	Enable two outstanding reads with out-of-order return: In - Disable Out - Enable
JP7 (Type)	Out	RM7000A family	CPU Type: In - Reserved Out - RM7000A family
JP8 (WB)	In	DDDD	64-bit Write-back data rate: In - DDDD Out - DxDxDxDx
JP9 (RSRV)	Out	Reserved	Reserved for internal use. Must be OUT.
JP10 (SV)	In **NOTE**: This is Out when using VxWorks.	Reserved	Reserved for internal use.
JP11 (VxWorks)	Out **NOTE**: In – only when working with VxWorks. When JP10 or JP12 is In, then this is set to "Don't Care".	Interrupts default routing	VxWorks interrupt lines routing: In - routing for VxWorks Out - default routing
JP12 (MASK)	In **NOTE**: This is Out when using VxWorks.	No interrupts to the CPU are masked	Mask all interrupt to CPU: In - all interrupts not masked Out - all interrupts are masked

Table 1: EV-RM7000A-S1 Module Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
U2 (CPU Multiplier)	Depends on the CPU's frequency	CPU internal frequency multiplier is 3	CPU internal frequency multiplier: x2, x2.5, x3, x3.5, x4, x4.5 and x5. If jumper is not inserted, the default value is x2. If more than one jumper is inserted, the lowest value is used. Maximum frequency is limited to the CPU device capabilities; refer to the respective CPU specification.
U3 (CPU Driver)	83%	CPU output drive slow rate control is 83%	CPU output drive slow rate control: 50%, 67%, 83% and 100%. If jumper is not inserted, the default value is 83%. If more than one jumper is inserted, the lowest value is used.

2.4 Interrupt Routing and Masking

The module receives six interrupt inputs from the PLD. The interrupt line routing to the CPU is configured by the PLD and can be changed by jumpers JP9–JP12. All the interrupts to the CPU can be hardware masked by JP12.

Table 2 describes the default interrupt routing.

Table 2: Default Interrupt Routing

Interrupt signal	VxWorks (JP11)	SV Monitor (JP10)	RSRV (JP9)
PCI_Int_	Int0	Masked	Reserved
CPUInt_1	Int1	Masked	Reserved
CPUInt_0	Int2	Masked	Reserved
Interrupt_	Int3	Masked	Reserved
SerIntA_	Int4	Masked	Reserved
SerIntB_	Int6	Masked	Reserved

3. EV-MPC7400/750-S1 Module

3.1 Overview

The EV-MPC7400/750-S1 is a CPU and L2 cache module that enables Marvell devices to operate with Motorola's MPC750 and 7400 CPUs (PowerPC family). This module is designed to plug into the SLOT1 connector designed for it.

The EV-MPC7400/750-S1 provides developers with a convenient platform to begin system development prior to hardware availability.

The EV-MPC7400/750-S1 module includes the following features:

- Up to 100 MHz CPU bus frequency (Except for the MPC7410 which runs at 133 MHz.)
- Optional CPUs:
  - Motorola's PowerPC 7400
  - Motorola's PowerPC 7410
  - Motorola's PowerPC 750
  - Motorola's PowerPC 755
  - IBM's PowerPC 750
- Onboard L2 cache
  - Supports up to 4MB L2 cache
- Debug interface
  - COP interface standard header
  - COP/JTAG interface connectors
- Reference power supply circuit
  - Support for different CPU voltages

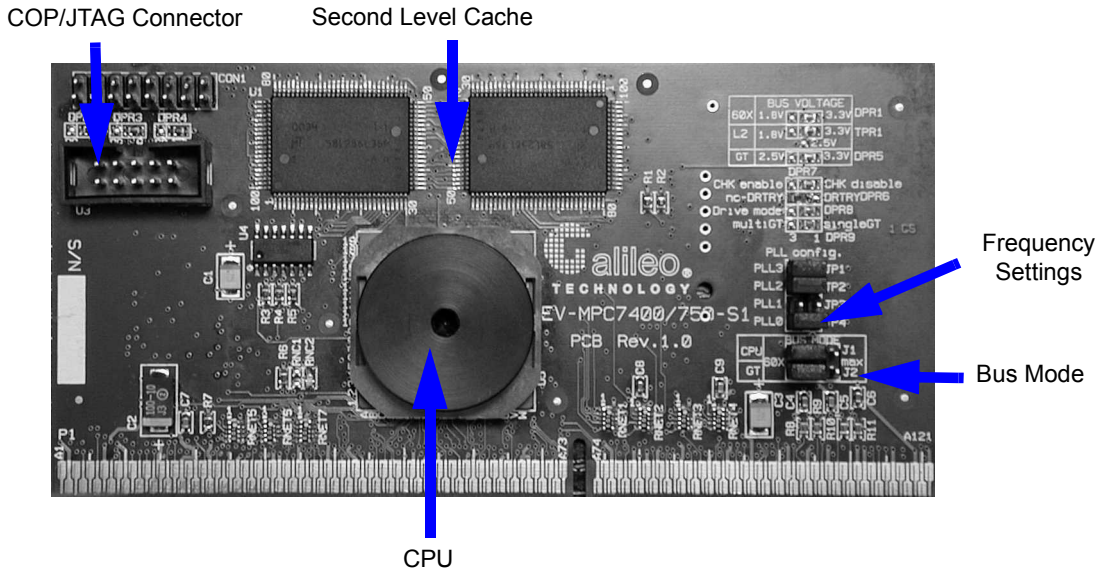
Notes

- When working with the PowerPC 7410, confirm that the voltage supplied by the backplane is 2.5V.
- When working with the PowerPC 7400 or 750, confirm that the voltage supplied by the backplane is 3.3V. See the respective backplane manual for additional details.
- The following does not apply for the EV-MPC7400/750-S1 Rev 2.0 (and above) modules. The EV-MPC7400/750-S1 Revision 1.x module contains a 16-pin header COP/JTAG interface as defined in the Motorola specification. To operate with the COP/JTAG interface, move DPR4 to position C (Connect,1&2). This prevents the JTAG state machine from resetting by means of the push button reset. This is because the COP_TRST# signal was not merged with the HRESET# on the module in order to generate the CPU_TRST#. When using the COP/JTAG interface, make sure that the COP/JTAG interface resets the JTAG state machine or powers down the system. In addition, the COP interface must not exceed
  6 MHz.

3.2 Description

The components of the EV-MPC7400/750-S1 module are illustrated in Figure 2.

Figure 2: EV-MPC7400/750-S1 Module Components



3.3 EV-MPC7400/750-S1 Jumpers

Table 3 details the EV-MPC7400/750-S1 jumpers.

Note

The CPU and the Marvell device must be configured to the same bus mode via J1 and J2.

Table 3: EV-MPC7400/750-S1 Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1	Depends on the CPU's frequency	CPU's PLL Configuration bit 3	See the PowerPC user manual
JP2	Depends on the CPU's frequency	CPU's PLL Configuration bit 2	See the PowerPC user manual
JP3	Depends on the CPU's frequency	CPU's PLL Configuration bit 1	See the PowerPC user manual
JP4	Depends on the CPU's frequency	CPU's PLL Configuration bit 0	See the PowerPC user manual

Table 3: EV-MPC7400/750-S1 Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
J1	60x bus mode	The CPU is configured to 60x bus mode.	CPU Bus Mode: 1 & 2 - 60x mode (default) 2 & 3 - MAX mode
J2	60x bus mode	Marvell Technology device is configured to 60x bus mode.	Marvell Device/CPU Bus Interface Bus Mode: 1 & 2 - MAX mode 2 & 3 - 60x mode (default)

4. EV-2xMPC7450-S1 Module

4.1 Overview

The EV-2xMPC7450-S1 is a multiple CPU and L3 cache module that enables Marvell devices to operate with a single or dual MPC7450 CPUs (PowerPCs). The EV-2xMPC7450-S1 is designed to plug into the SLOT1 connector designed for it.

The EV-2xMPC7450-S1 module includes the following features:

- Optional CPUs
  - Single Motorola PowerPC 7450
  - Double Motorola PowerPC 7450
- Onboard L3 cache
  - Supports up to 2MB L3 cache for each CPU
- 60x bus arbiter
  - Onboard 60x bus Arbiter
  - Supports Marvell's internal 60x bus arbiter or any other arbiter placed on the backplane
- Debug interface
  - Two separate COP/JTAG interface standard headers for each CPU
- Reference power supply circuit
  - Supports for different CPU voltages

Note

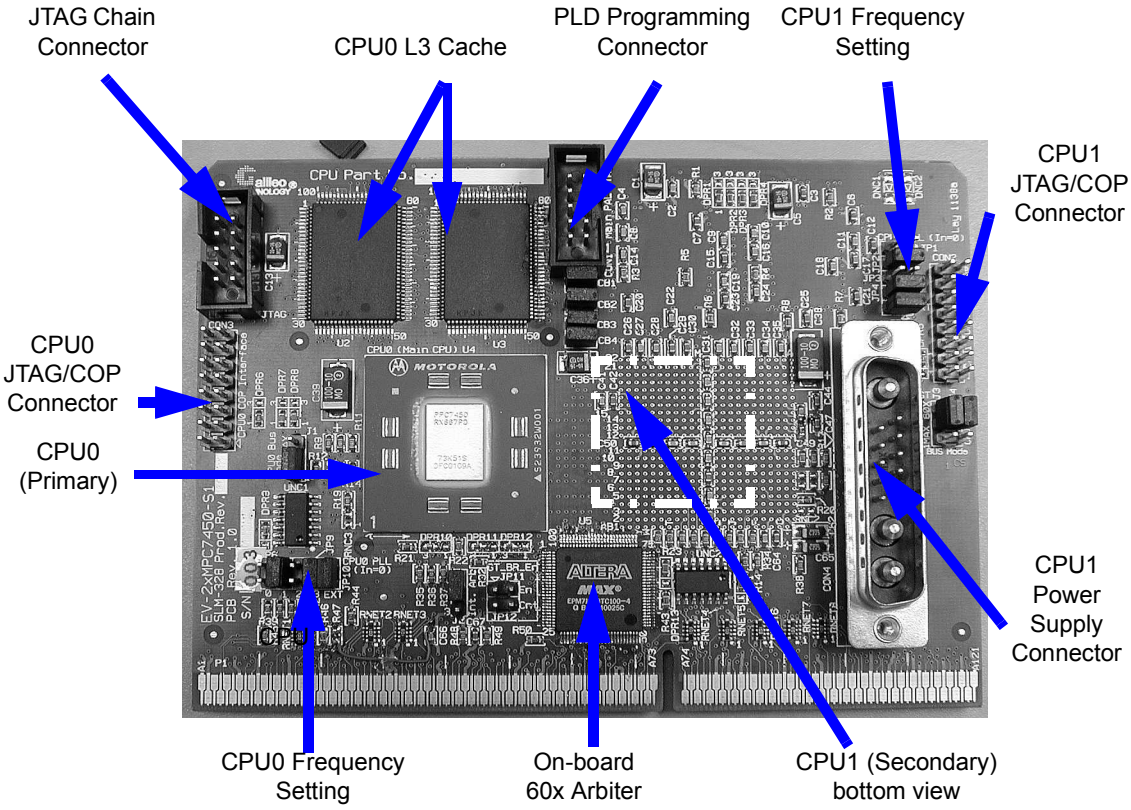
Make sure that the voltage supplied by the backplane is 2.5V. See the respective backplane manual for additional details.

- Power supply circuit connector
  - Power supply connector for the secondary CPU power supply

4.2 Description

The EV-2xMPC7450-S1 module components are shown in Figure 3.

Figure 3: EV-2xMPC7450-S1 Module Components



4.3 Onboard 60x Bus Arbiter

The EV-2xMPC7450-S1 provides an onboard 60x bus arbiter. This arbiter can be enabled/disabled via jumper J2 (see Section 4.4).

Notes

- The onboard 60x bus arbiter PLD is not assembled when shipped with the EV-64260A-BP. In this case, the GT-64260A internal arbiter must be enabled.
- When the onboard 60x arbiter is disabled, DPR10 - DPR13, DPR32 and DPR36 must be set to position 2&3.

The onboard 60x arbiter supports the following features:

- Three 60x bus masters (2xMPC7450 and the Marvell device's 60x bus master)
- Reset sequence logic:
  - Single CPU system; only CPU0 (Primary) is assembled

- Single CPU system; both CPUs are assembled (CPU0 active)
- Double CPU system; both CPUs are active

- Up to five transaction pipeline depth
- Address-only transactions and memory coherency protocol
- Non-requested bus grants to the GT-64260-B-0 device's 60x bus master

4.3.1 Reset Sequence for the Double CPU System

The onboard 60x bus arbiter includes logic for the reset sequence. After reset, both of the CPUs request the 60x bus. The arbiter grants the bus to CPU0 (the primary CPU) in order to enable the CPU to initialize the system. CPU0 must relay a signal to the onboard 60x arbiter indicating that the system was initialized via the CPU1_BG_EN_N signal. This functionality is enabled via one of the device's MPP pins connected to the SLOT1 connector. At this point, the onboard 60x bus arbiter grants the 60x bus to CPU1 (the secondary CPU) for the first time. The onboard 60x bus arbiter now operates in a fixed, round-robin scheme. An example is provided in the EV-64260BP, Rev 2.0 User Manual, Section 4.6 "SMP Support".

4.3.2 Reset Sequence for a Single CPU System

The EV-2xMPC7450-S1 can operate in single CPU mode when both of the CPUs are assembled, or only when CPU0 is assembled. When operating with one CPU, while both CPUs are assembled, the CPU1_BG_EN_N signal of the device's MPP pins must not be enabled by the software. As a result, CPU0 is active and CPU1 is inactive.

CPU1 can also be disabled (inactive), when both CPU's are assembled, by disassembling R132 on the EV-2xMPC7450-S1 module. As a result, the CPU1_BG_EN_N signal is disconnected from the onboard 60x arbiter of the SLOT1 connector (P1).

4.3.3 Non-requested Bus Grant Support

The non-requested bus grant support enables the EV-2xMPC7450-S1 to operate with the GT-64260-B-0. This device cannot request 60x bus access (See the GT-64260-B-0 errata document for more information). To avoid performance loss, Marvell recommends disabling this bus request feature when operating with devices that may request the bus or if the 60x bus is not requested by the GT-64260-B-0 (indicates no master activity).

The non-requested bus grant feature is enabled via jumper JP11, and when enabled, it can be configured to grant the 60x bus to the device's 60x bus master every 64 or 256 system clock cycles via JP12. See Section 4.4 for further details about these jumper settings.

4.3.4 Onboard 60x Arbiter Restrictions and Performance Loss

The following restrictions must be taken into consideration when the onboard 60x arbiter is enabled.

- The external arbiter requires a minimum of one clock cycle delay between the TS# signal assertion and the AACK# signal assertion. (AACK delay enabled).
- The external arbiter requires a minimum of one clock cycle delay between the AACK# signal assertion and the TA# signal assertion. (TA delay enabled).
- The maximum frequency is 100 MHz.
- The FIFO depth was reduced to 4+1 transactions so that it fits into the PLD device and can operate at a 100 MHz system clock frequency.
- Each switch from one master to another includes one idle clock cycle. During this time, no master receives the bus grant.
- If the non-requested bus granted to the Marvell device is enabled (see Section 4.3.3), the bus request logic in the arbiter is enabled and the arbiter will assert the GT_BG_OUT_ signal to the Marvell device every given number of cycles. The given number of cycles is determined by the BR_CNT_MAX signal. If the BR_CNT_MAX is high, the number of cycles will be 0xFF (256), otherwise, it will be 0x3F (64).

4.3.5 Onboard 60x AC Timings

Table 4 provides the onboard 60x AC Timing specifications.

Table 4: AC Timing

Signal	Description	Value	Units
CPU0_BR_IN_	Setup time	3.7	ns
CPU1_BR_IN_	Setup time	2.9	ns
GT_BR_IN_	Setup time	3.3	ns
TS_IN_	Setup time	3.1	ns
TT_IN3	Setup time	3	ns
AACK_IN	Setup time	3	ns
ARTRY_IN_	Setup time	4.2	ns
TBST_IN_	Setup time	1.9	ns
TA_IN_	Setup time	4.3	ns
CPU0_BG_OUT_	Output delay	3.3	ns
CPU1_BG_OUT_	Output delay	3.3	ns
GT_BG_OUT_	Output delay	6	ns
CPU0_DBG_OUT_	Output delay	6	ns
CPU1_DBG_OUT_	Output delay	3.3	ns
GT_DBG_OUT_	Output delay	3.3	ns
ARTRY_IN_,TS_IN_,TT_IN3, TBST_IN	Hold time	0.1	ns
All inputs (except –ARTRY_IN_,TS_IN_,TT_IN3, TBST_IN)	Hold time	0	ns

4.4 EV-2xMPC7450-S1 Jumpers

Table 5 details the EV-2xMPC7450-S1 jumpers.

Table 5: EV-2xMPC7450-S1 Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1-JP5	Depends on the CPU's frequency	CPU1's PLL Configuration [0:3], PLL_EXT (x 6.5)	See the PowerPC 7450 user manual.

Table 5: EV-2xMPC7450-S1 Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
JP6, JP7, JP8, JP9, JP10	Depends on the CPU's frequency	CPU0's PLL Configuration [0:3], PLL_EXT (x 6.5)	See the PowerPC 7450 user manual
JP11 (En), JP12 (Cnt)	Out, In	Enable non-requested bus grant to the Marvell device on the 60x bus every 256 system clock cycles	The device's 60x non-requested bus grant configuration (see Section 4.3): In, In - The device's 60x bus master receives the bus every 64 system clock cycles when requested. In, Out -The device's 60x bus master receives the bus every 256 system clock cycles. Out, In - Reserved. Out, Out - The device's 60x bus master receives the bus only when requested.
J1	60x	CPU0 is configured to 60x bus mode.	CPU0 (Primary) Bus Mode: 1 & 2 - 60x mode 2 & 3 - MPX mode
J2	2 & 3	The onboard 60x arbiter is enabled.	The 60x bus arbiter selection (see Section 4.3): 1 & 2 - The Marvell device's internal 60x bus arbiter is enabled 2 & 3 - The Marvell device's internal arbiter is disabled.
J3	60x	The GT CPU interface is configured to 60x bus mode.	GT CPU Bus Interface Bus Mode: 1 & 2 - MPX mode 2 & 3 - 60x mode
J4	60x	CPU1 is configured to 60x bus mode.	CPU1 Bus Mode: 1 & 2 - 60x mode 2 & 3 - MPX mode
CB1,CB2, CB3	All Out	The CPU1 core power supply from the power connector.	CPU1 core power source: In - Connected to CPU0 core power supply. Out - From power connector (CON4).

Warning

- Do not connect CB1-CB3 when the power module on CON4 is connected.
- The power module must be connected to a power supplier.

4.5 SMP Support on EV-64260-BP, Rev 2.0

Symmetric Multi-processing (SMP) support is provided by the EV-2xMPC7450-S1 module on EV-64260-BP Rev 2.0 boards.

Table 6 details the system configurations on the EV-64260-BP to enable SMP support.

Table 6: SMP Support

SMP Signal name	GT-64260 system controller Signal Name	EV-64260-BP Signal Name	EV-64260-BP Configuration
CPU0_to_CPU1_Int	MPP23 → MPP4	TCEcnt0 → TCEcnt1	R225 assembled (0 Ohm)
CPU1_to_CPU0_Int	MPP24 → MPP10	CPU_Int0 → WDNMI_n	RNC7 assembled (0 Ohm)
CPU0_Int	Interrupt#	Interrupt_n	N/A
CPU1_Int	INT0* (connected to MPP27)	PCI0IntOption PCI0_INTA/B/C/D	MPP is not used as an output. It must be configured to High-Z (input). INTA - JP5 and JP13 In INTB - JP6 and JP14 In INTC - JP7 and JP15 In INTD - JP8 and JP16 In
GT-to_CPU1_BG_En	MPP25	CPU_Int1	N/A
CPU0_MCP_n	MPP22	RS232IntBorPCI1int_n (SerIntB_n)	J4 must be connected in position 1&2

5. EV-IBM750CX-S1 Module

5.1 Overview

The EV-IBM750CX-S1 is a CPU module that enables Marvell devices to operate with IBM PowerPC750CX and IBM PowerPC750CXe CPUs. The EV-IBM750CX-S1 is designed to plug into the SLOT1 connector designed for it.

The EV-IBM750CX-S1 module includes the following features:

- Optional CPUs
  - IBM PowerPC750CX or PowerPC750CXe
- 60x bus arbiter
  - Onboard 60x bus arbiter
  - Supports Marvell's internal 60x bus arbiter or any other arbiter placed on the backplane
- Debug interface
  - COP/JTAG interface standard header
- Reference power supply circuit
  - Support for different CPU voltages

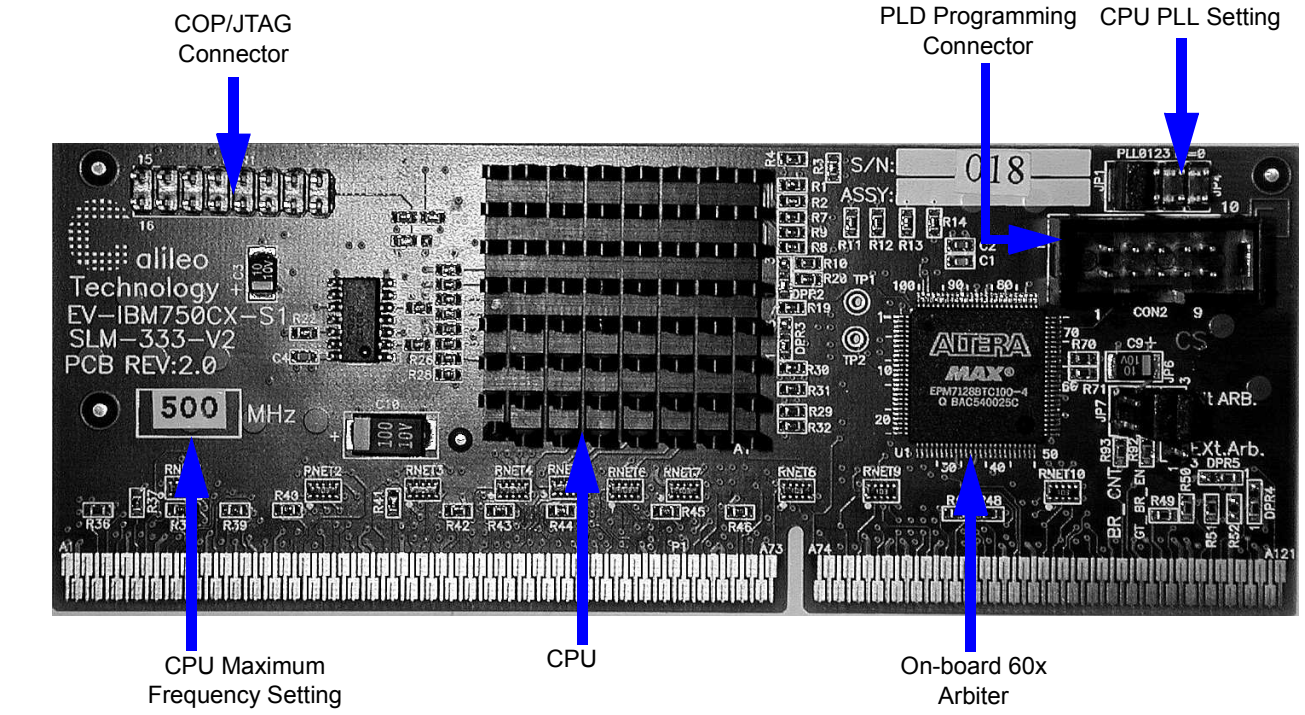
Note

Make sure that the voltage supplied by the backplane is 2.5V. See the respective backplane manual for additional information.

5.2 Description

The EV-IBM750CX-S1 module components are shown in Figure 4.

Figure 4: EV-IBM750CX-S1 Module Components



5.3 Onboard 60x Bus Arbiter

The EV-IBM750CX-S1 provides an onboard 60x bus arbiter. This arbiter can be enabled/disabled via jumper J1 (see Table 7).

Notes

- The on board 60x bus arbiter PLD is not assembled when shipped with the EV-64260A-BP. In this case the GT-64260A internal arbiter must be enabled.
- When the on board 60x arbiter is disabled, DPR2, DPR6 and DPR7 must be set to position 2&3.

The onboard 60x arbiter supports the following features:

- Two 60x bus masters (PowerPC 750CX/e and the Marvell device's 60x bus master)
- Up to a five transaction pipeline depth
- Address-only transactions and memory coherency protocol
- Non-requested bus grants to the GT-64260-B-0 device's 60x bus master

Note

The onboard 60x bus arbiter code supports an additional master on the 60x bus that is not used by this module. Moreover, it supports a reset sequence for double CPU systems. For more information about these features, see Section 4.3.

5.3.1 Non-requested Bus Grant Support

The non-requested bus grant support enables the EV-IBM750CX-S1 to operate with the GT-64260-B-0. This device cannot request the 60x bus (See the GT-64260-B-0 errata document for more information.) To prevent performance loss, Marvell recommends disabling this bus request feature when operating with devices that may request the bus, or if the 60x bus is not requested by the GT-64260-B-0 (indicates no GT-64260-B-0 master activity).

The non-requested bus grant feature is enabled via JP6. When enabled, it can be configured to grant the 60x bus to the device's 60x bus master every 64 or 256 system clock cycles via JP7. For more information about the jumpers settings, see Table 7.

5.3.2 Onboard 60x Arbiter Restrictions and Performance Loss

Refer to Section 4.3.4.

5.3.3 On-board 60x AC Timings

Refer to Section 4.3.5.

5.4 EV-IBM750CX-S1 Jumpers

Note

The final jumper setting might change depending on CPU's maximum frequency

Table 7 details the EV-IBM750CX-S1 jumpers.

Table 7: EV-IBM750CX-S1 Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1, JP2, JP3, JP4	Depends on the CPU's frequency	CPU's PLL Configuration [0:3] (x 4.5). Not necessarily the maximum CPU frequency. This will vary depending on the CPU used.	See the IBM PowerPC 750CX/E user manual
JP6 (En), JP7 (Cnt)	In, Out	Enable non-requested bus grant to the Marvell device on the 60x bus every 256 system clock cycles.	The device's 60x non-requested bus grant configuration (see Section 5.3.1): In, In - The device's 60x bus master receives the bus every 64 system clock cycles and when requested. In, Out -The device's 60x bus master receives the bus every 256 system clock cycles. Out, In - Reserved. Out, Out - The device's 60x bus master receives the bus only when requested.

Table 7: EV-IBM750CX-S1 Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
J1	2 & 3	The onboard 60x arbiter is enabled.	The 60x bus arbiter selection (see Section 4.3): 1 & 2 - The Marvell device's internal 60x bus arbiter is enabled 2 & 3 - The Marvell device's internal arbiter is disabled.

6. DB-IBM750FX-S1 Module

6.1 Overview

The DB-IBM750FX-S1 is a CPU module that enables Marvell devices to operate with IBM PowerPC 750FX CPUs. The DB-IBM750FX-S1 is designed to plug into the SLOT1 connector designed for it.

The DB-IBM750FX-S1 module includes the following features:

- Optional CPUs
  - IBM PowerPC750FX
- Debug interface
  - Two COP/JTAG interface standard headers

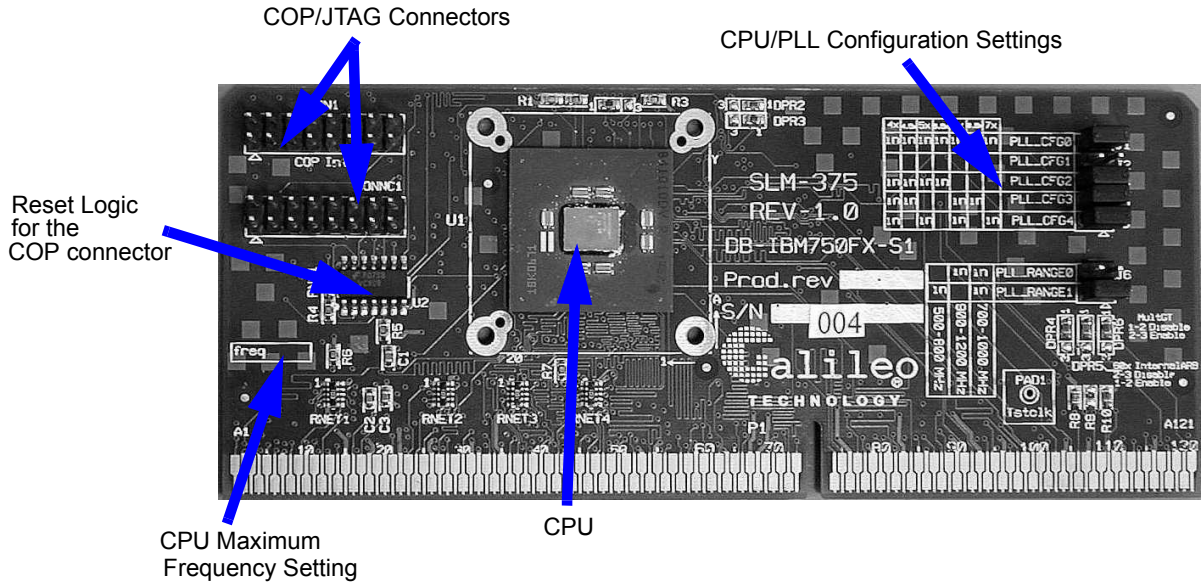
Note

Make sure that the CPU bus voltage supplied by the backplane is 2.5V. See the respective backplane manual for additional information.

6.2 Description

The DB-IBM750FX-S1 module components are shown in Figure 5.

Figure 5: DB-IBM750FX-S1 Module Components



6.3 DB-IBM750FX-S1 Jumpers

Table 8 details the DB-IBM750FX-S1 jumpers.

Table 8: DB-IBM750FX-S1 Jumpers

Jumper	Shipping Configuration	Assignment	Description
J1, J2, J3, J4, J5	Depends on the CPU's frequency	CPU's PLL Configuration [0..4]. Not necessarily the maximum CPU frequency. This will vary depending on the CPU used.	For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU frequency of operation as follows: '01000' => SYSCLK x 4 '01001' => SYSCLK x 4.5 '01010' => SYSCLK x 5 '01011' => SYSCLK x 5.5 '01100' => SYSCLK x 6 '01101' => SYSCLK x 6.5 '01110' => SYSCLK x 7
J6, J7	Depends on the CPU's frequency	CPU's PLL Range Configuration[0..1].	The PLL Range Configuration is as follows: '00' => 600 - 800 MHz '01' => 800 - 1000 MHz '10' => 400 - 600 MHz '11' => Reserved.

7. EV-SR71010A-S1 Module

7.1 Overview

The EV-SR71010A-S1 is a CPU and L3 cache module. This module enables Marvell devices to operate with Sandcraft's SR71010 CPU. The module is designed to plug into the SLOT1 connector designed for it.

Warning

- Make sure you insert the module tightly into the SLOT1 connector. Failure to insert the module correctly could lead to damage to both the module and the board.
- Do not install the EV-SR71010A-S1 into a SLOT1 that is not designated for it.

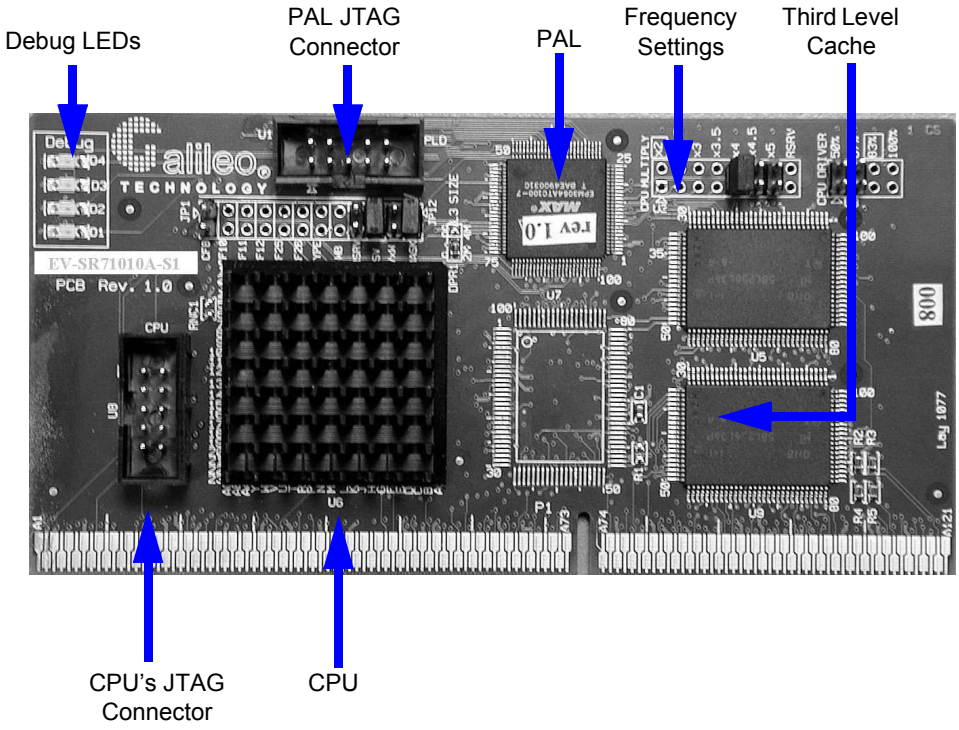
The EV-SR71010A-S1 includes the following features:

- Up to 133 MHz CPU bus frequency
- Optional CPU (Sandcraft's SR71010)
- Onboard L3 cache
  - Supports up to 4 MB of L3 cache
- Configurable jumpers for logic reset
- Reference power supply circuit
  - Support for different CPU voltages

7.2 Description

The EV-SR71010A-S1 module components are illustrated in Figure 6.

Figure 6: EV-SR71010A-S1 Module Components



7.3 SR71010A Module Jumpers

Table 9 details the SR71010A module jumpers.

Table 9: SR71010A Module Jumpers

Jumper	Shipping Configuration	Assignment	Description
JP1 (CFG8)	Out	CPU in Big Endian ordering mode	EndBit: Specifies byte ordering. Logically ordered with the Big Endian signal: In - Little Endian ordering Out - Big Endian ordering
JP9 (RSRV)	Out	Reserved	Reserved for internal use. Must be OUT.

Table 9: SR71010A Module Jumpers (Continued)

Jumper	Shipping Configuration	Assignment	Description
JP10 (SV)	In **NOTE**: This is Out when using VxWorks.	Reserved	Reserved for internal use.
JP11 (VxWorks)	Out **NOTE**: In – only when working with VxWorks. When JP10 or JP12 is In, then this is set to "Don't Care".	Interrupts default routing	VxWorks interrupt lines routing: In - routing for VxWorks Out - default routing
JP12 (MASK)	In **NOTE**: This is Out when using VxWorks.	No interrupts to the CPU are masked	Mask all interrupt to CPU: In - all interrupts not masked Out - all interrupts are masked
U2 (CPU Multiplier) JP17, 18, 19	Depends on the CPU's frequency	CPU internal frequency multiplier is 4.5.	CPU internal frequency multiplier: x4, x4.5 and x5. If jumper is not inserted, the default value is x2. If more than one jumper is inserted, the lowest value is used. Maximum frequency is limited to the CPU device capabilities; refer to the respective CPU specification.
U3 (CPU Driver) (50%) JP21 (67%) JP22	Out = "1", Fast In = "0", Slow Out Out	 CPU Output Drive CPU L3 Output Drive	CPU output drive slow rate control: 50% and 67%.

7.4 Interrupt Routing and Masking

The module receives six interrupt inputs from the PLD. The interrupt line routing to the CPU is configured by the PLD and can be changed by jumpers JP9–JP12. All the interrupts to the CPU can be hardware masked by JP12.

Table 10 describes the default interrupt routing.

Table 10: Default Interrupt Routing

Interrupt signal	VxWorks (JP11)	SV Monitor (JP10)	RSRV (JP9)
PCI_Int_	Int0	Masked	Reserved
CPUInt_1	Int1	Masked	Reserved
CPUInt_0	Int2	Masked	Reserved
Interrupt_	Int3	Masked	Reserved

Table 10: Default Interrupt Routing (Continued)

Interrupt signal	VxWorks (JP11)	SV Monitor (JP10)	RSRV (JP9)
SerIntA_	Int4	Masked	Reserved
SerIntB_	Int6	Masked	Reserved

8. Revision History

Table 11: Revision History

Revision Number	Date	Comments
Revision 1.0	December 5, 2000	First Release
Revision 1.1	December 18, 2000	1. Updated Figures 1 and 2. 2. Updated Tables 1, 2, and 3.
Revision 1.2	June 28, 2001	1. Table 1, “EV-RM7000A-S1 Module Jumpers,” on page 8, corrections to settings for jumpers: J4, JP11, JP12, U2, and U3. 2. In Section 3., added note regarding COP/JTAG interface connector. 3. Table 3, “EV-MPC7400/750-S1 Jumpers,” on page 12, corrections to settings for jumpers: JP3 and JP4. 4. Table 6, “SMP Support,” on page 19, modified configuration description for CPU1_Int /MPP27 signal in. 5. Added Section 4. 6. Added Section 5.
Rev. A	September 11, 2001	1. Added two notes about PowerPC voltage requirements to Section 3.1. 2. Added PowerPC 7410 option to Section 3. 3. Replaced "7400" with "7400/10" in Section 3. 4. Added a note about voltage requirements to Section 4.1. 5. Added two notes about the 60x bus arbiter PLD in Section 4.3. 6. Added a note about voltage requirements to Section 5.1. 7. Added two notes about the 60x bus arbiter PLD in Section 5.3.
Rev. B	October 30, 2001	1. Added the phrase “Depends on the CPU’s frequency” to the description of U2 (CPU Multiplier) in Table 1, “EV-RM7000A-S1 Module Jumpers,” on page 8. 2. Added the phrase “Except for the MPC7410 which runs at 133 MHz” to the “Up to 100 MHz CPU bus frequency” bullet in Section 3.1. 3. Added the phrase “Depends on the CPU’s frequency” to the description of JP1-JP4 in Table 3, “EV-MPC7400/750-S1 Jumpers,” on page 12. 4. Added the phrase “Depends on the CPU’s frequency” to the description of JP1-JP10 in Table 5, “EV-2xMPC7450-S1 Jumpers,” on page 17. 5. Added the phrase “Depends on the CPU’s frequency” to the description of JP1-JP4 in Table 7, “EV-IBM750CX-S1 Jumpers,” on page 22.
Rev. C.	March 19, 2002	Added Section 6. DB-IBM750FX-S1 Module.
Rev. D	June 24, 2002	1. Updated Section 2. EV-RM7000A-S1 Module by replacing RM7000 with RM7000A. 2. Added Section 7. EV-SR71010A-S1 Module.