

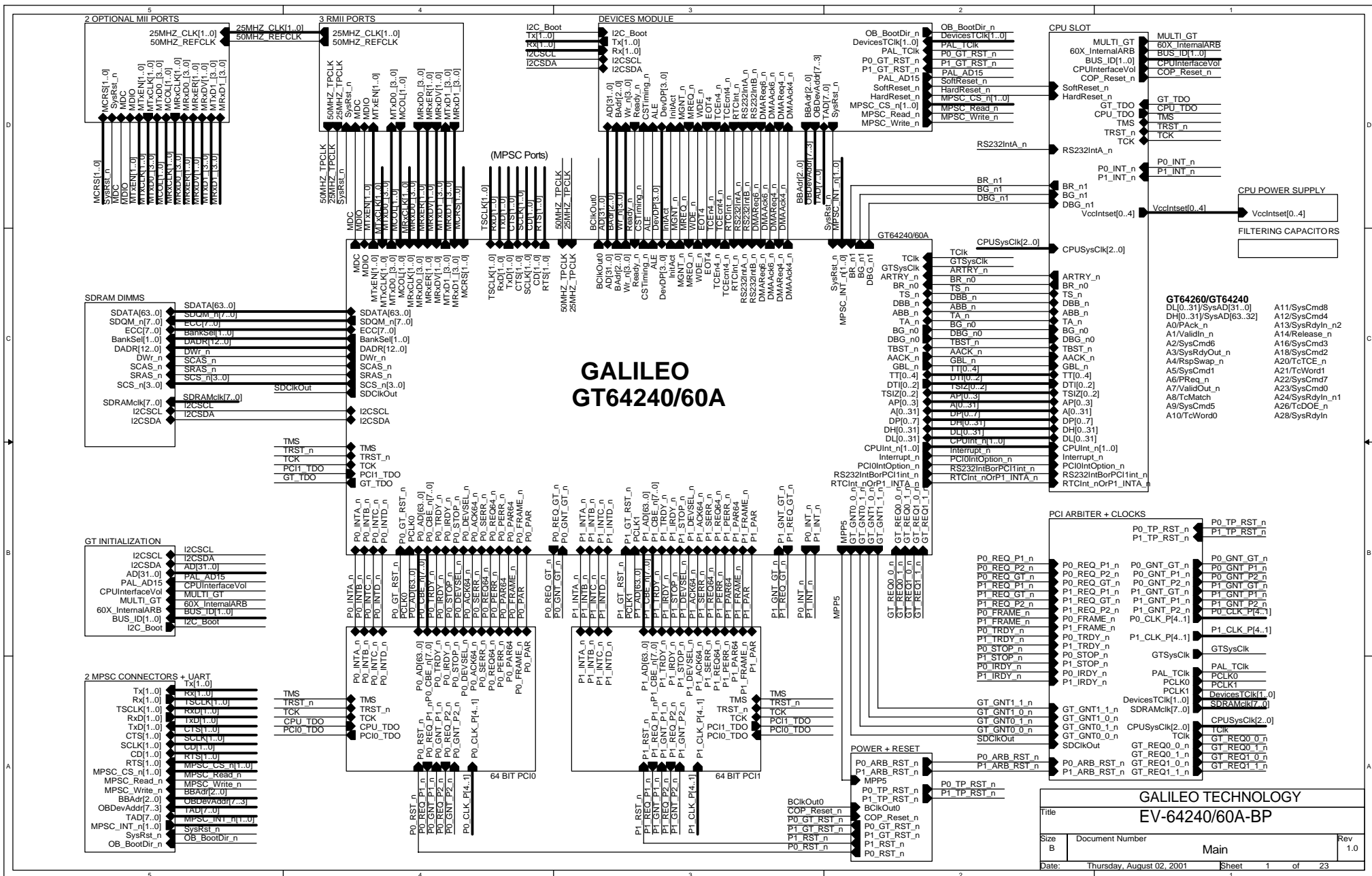
Block Diagram:
Available in a separate document

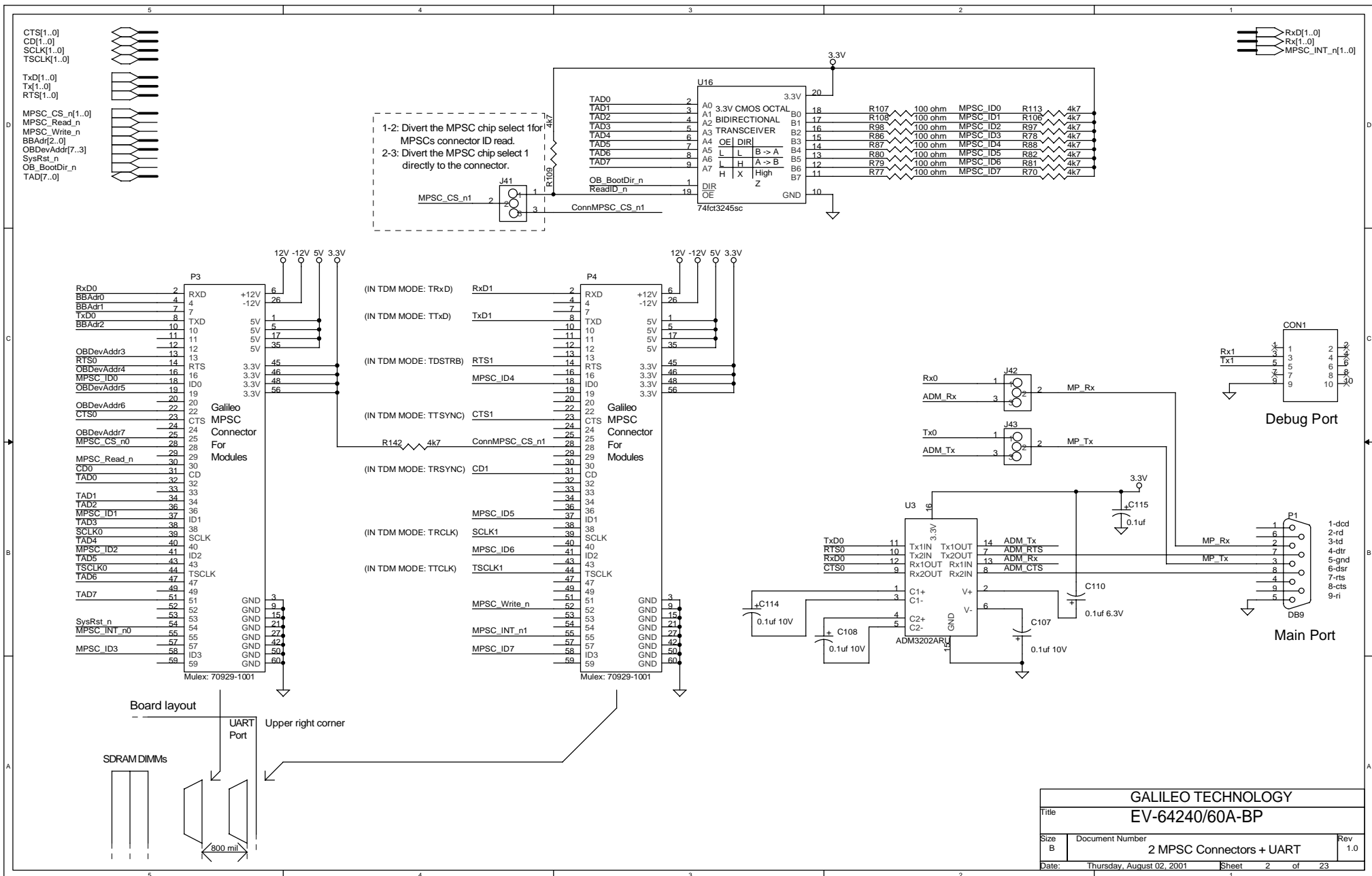
Sheet Number:	Content:
1	Top hierarchy.
2	MPSC connectors and serial ports
3	Two optional MII ports
4	Three RMII ports
5	64 Bit PCI0 and test points for PCI0's AD bus.
6	64 Bit PCI1
7	CPU's interface test points
8	CPU slot1 connector, power regulators for the GT's CPU interface IO and for the module's VCC internal CPU power protection circuit
9	Device's latches, on board boot FLASH and EEPROM, on board boot transceiver Device's and test PAL , SODIMM 144 connector
10	GT64260\60A's initialization and I2C.
11	GT64260\40A Part 1 (Power), 3.3V and 1.8 V regulators for the GT , power filtering and PLL filtering circuit.
12	GT64260\40A Part 2 (PCI interfaces)
13	GT64260\40A Part 3 (Devices, SDRAM, I2C and MPP interfaces) MPP ports test points.
14	GT64260\40A Part 4 (CPU interface), JTAG connector and JTAG map.
15	GT64260\40A Part 5 (Communication ports interfaces) Communication ports test points.
16	PLL filtering circuit layout application note
17	PCI Optional arbiters + tests points, arbitration source setup Clock sources (PCI, SDRAM and all the rest)
18	Main power supply (including the DC to DC circuit), power indication leds Optional speaker and reset source.
19	SDRAM DIMM connectors
20	Filtering capacitors
21	Filtering capacitors for PCI0
22	Filtering capacitors for PCI1

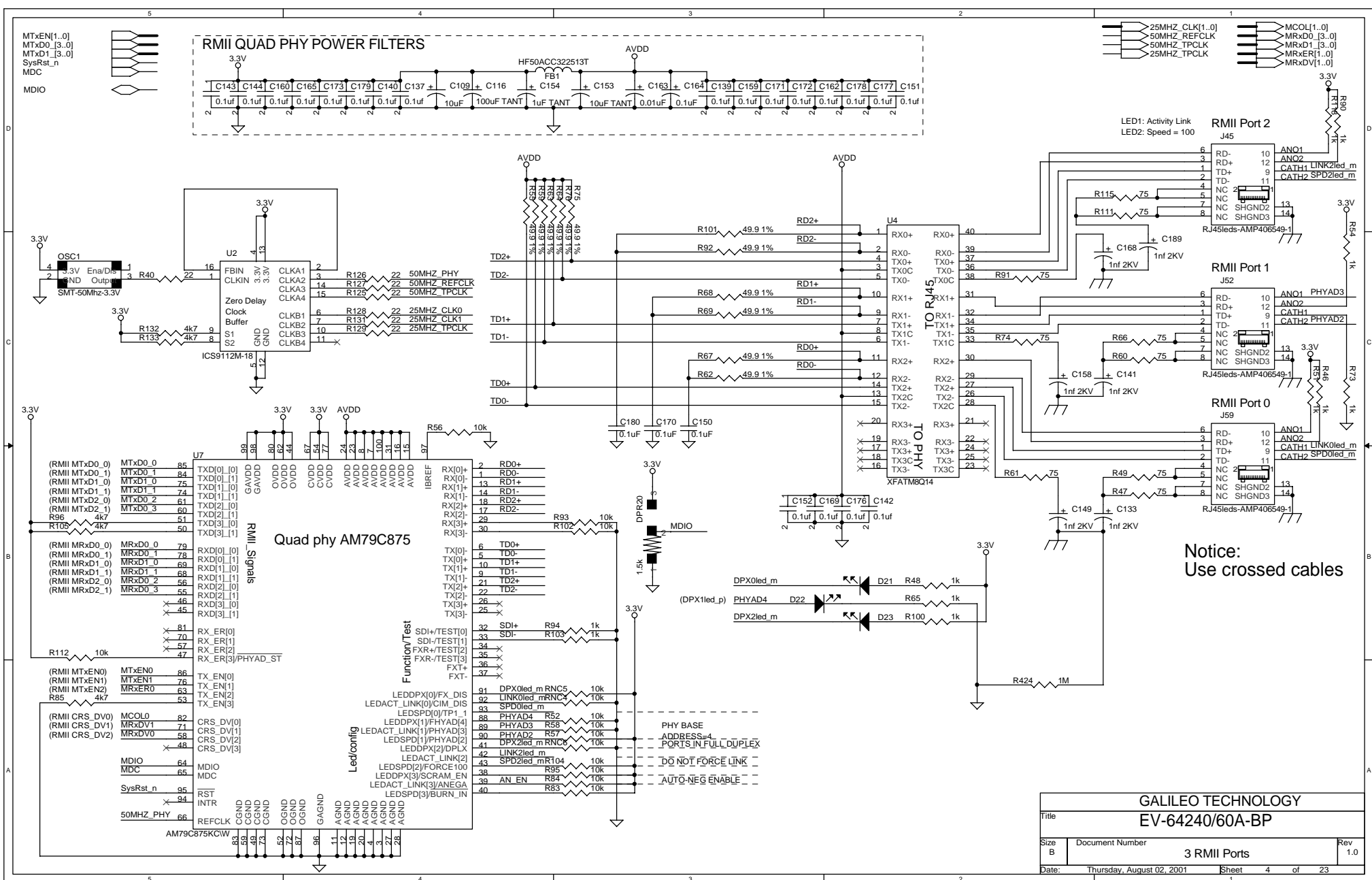
Rev Number	Remarks
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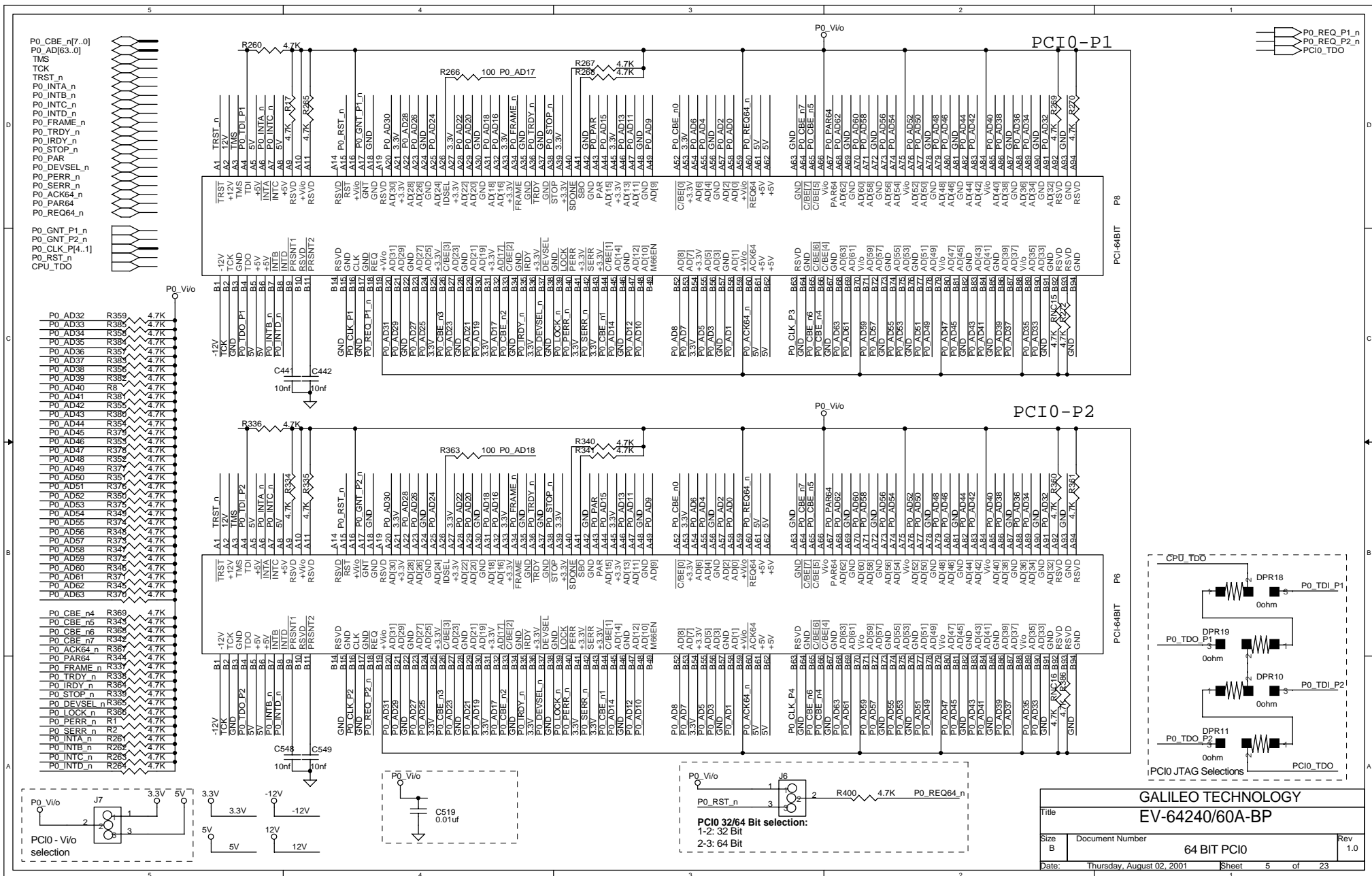
These schematic serves Galileo's GT64240A and GT64260A.
The difference is in the CPU interface, please note:
On the CPU's interface signals the name on the left is for PPC (GT64260A) and the one on the right is for MIPS (GT64240A).
For example: DL0\SysAD31.

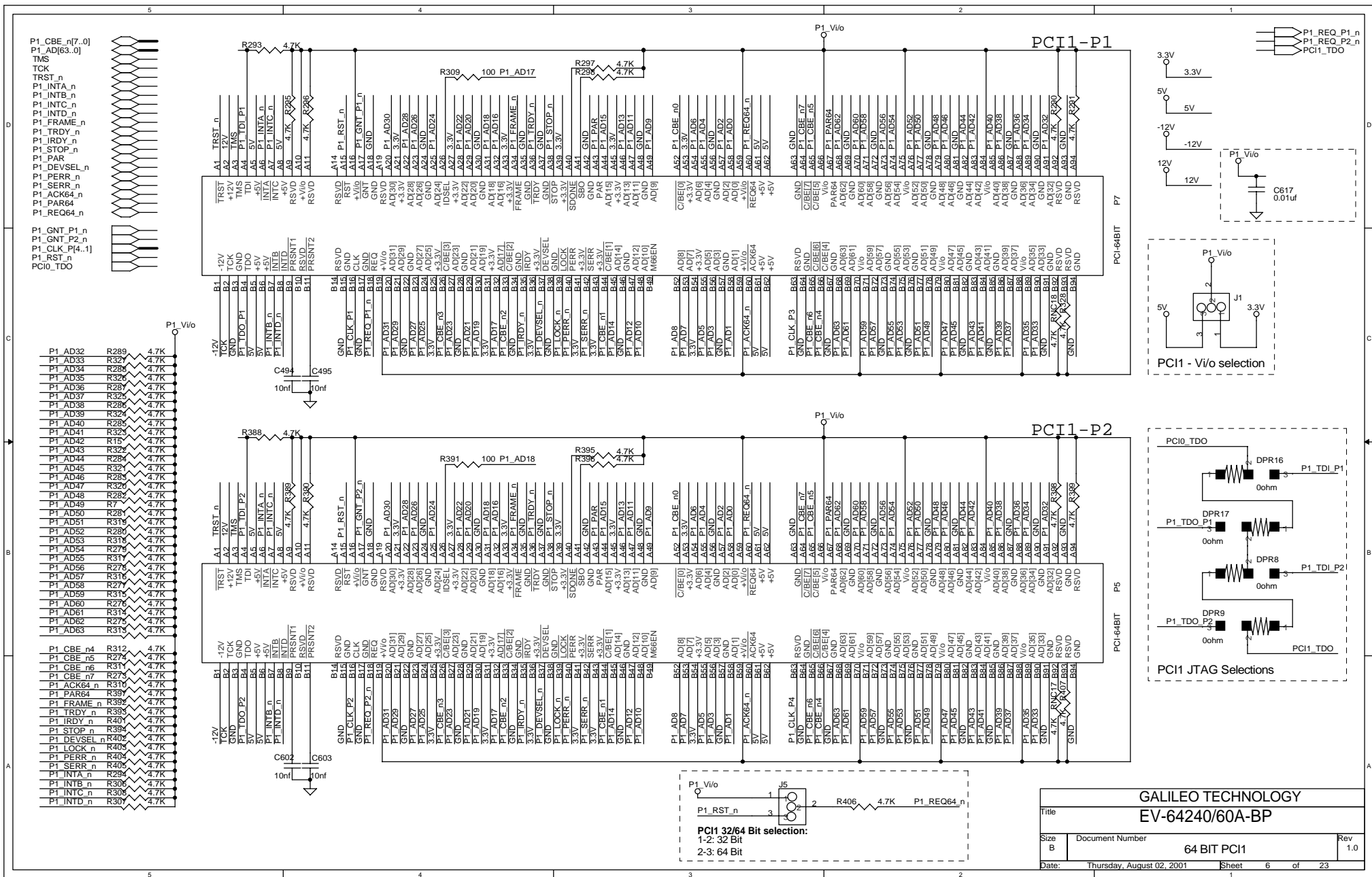
GALILEO TECHNOLOGY			
Title		EV-64240/60A-BP	
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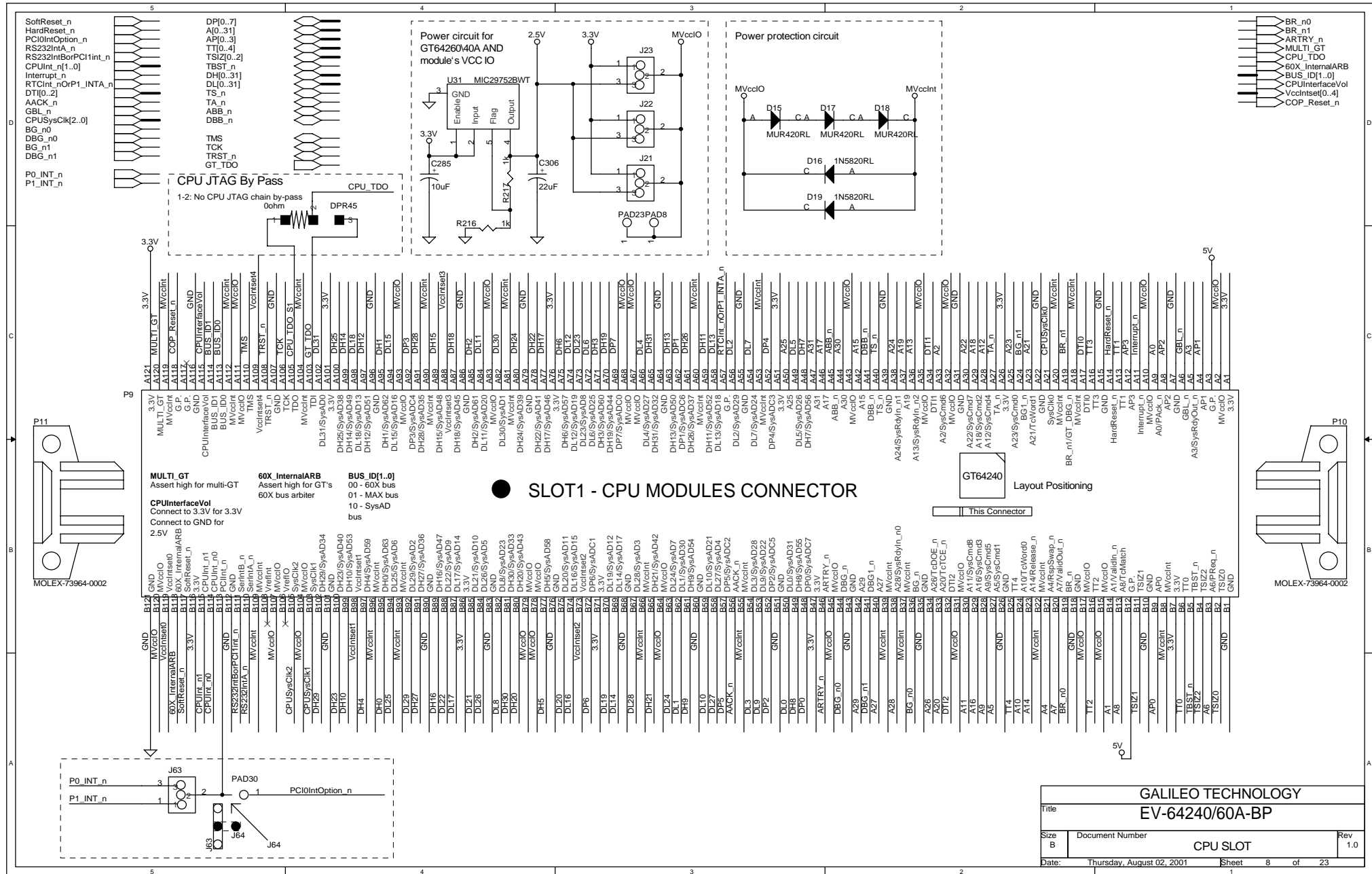


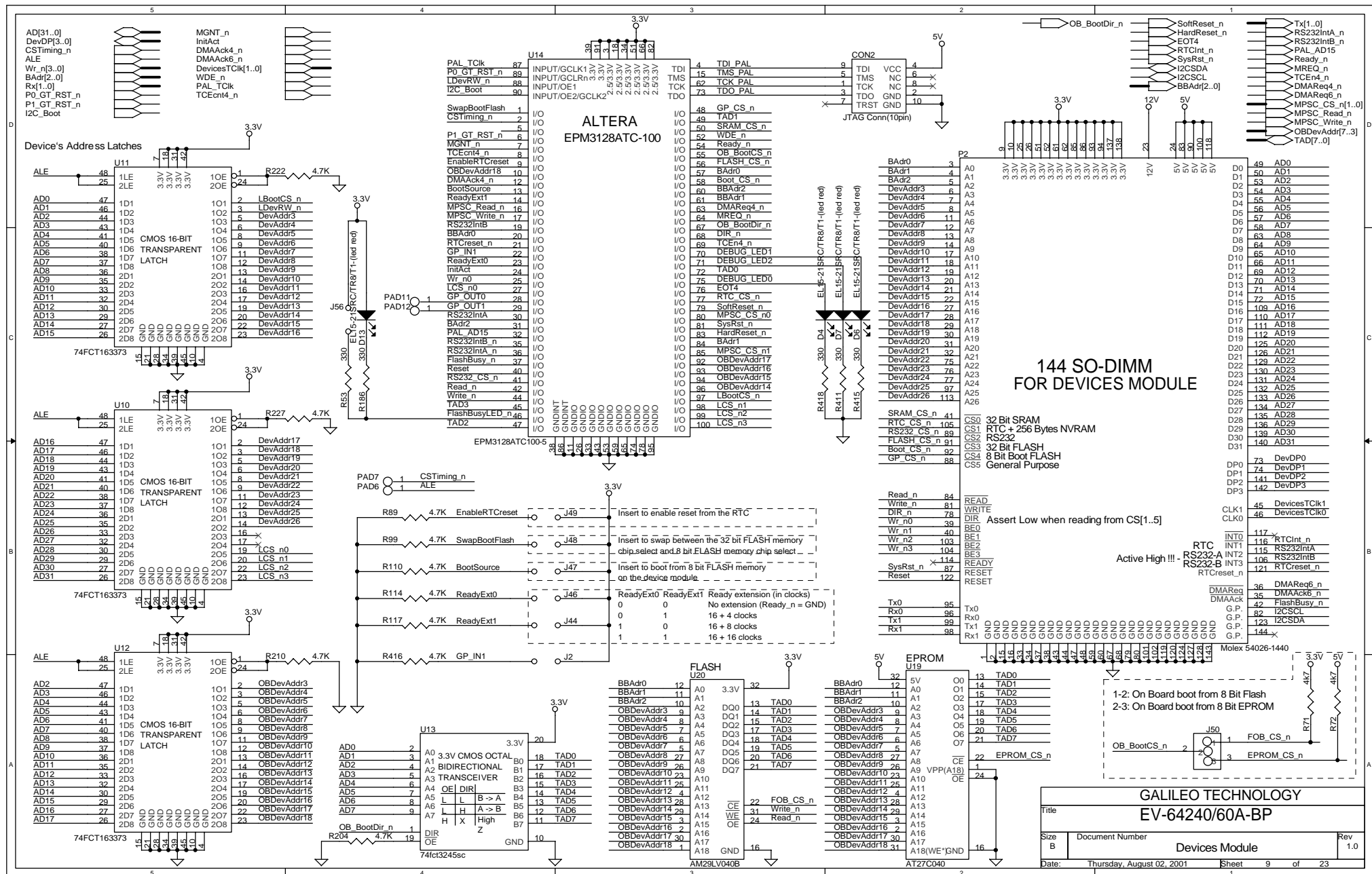


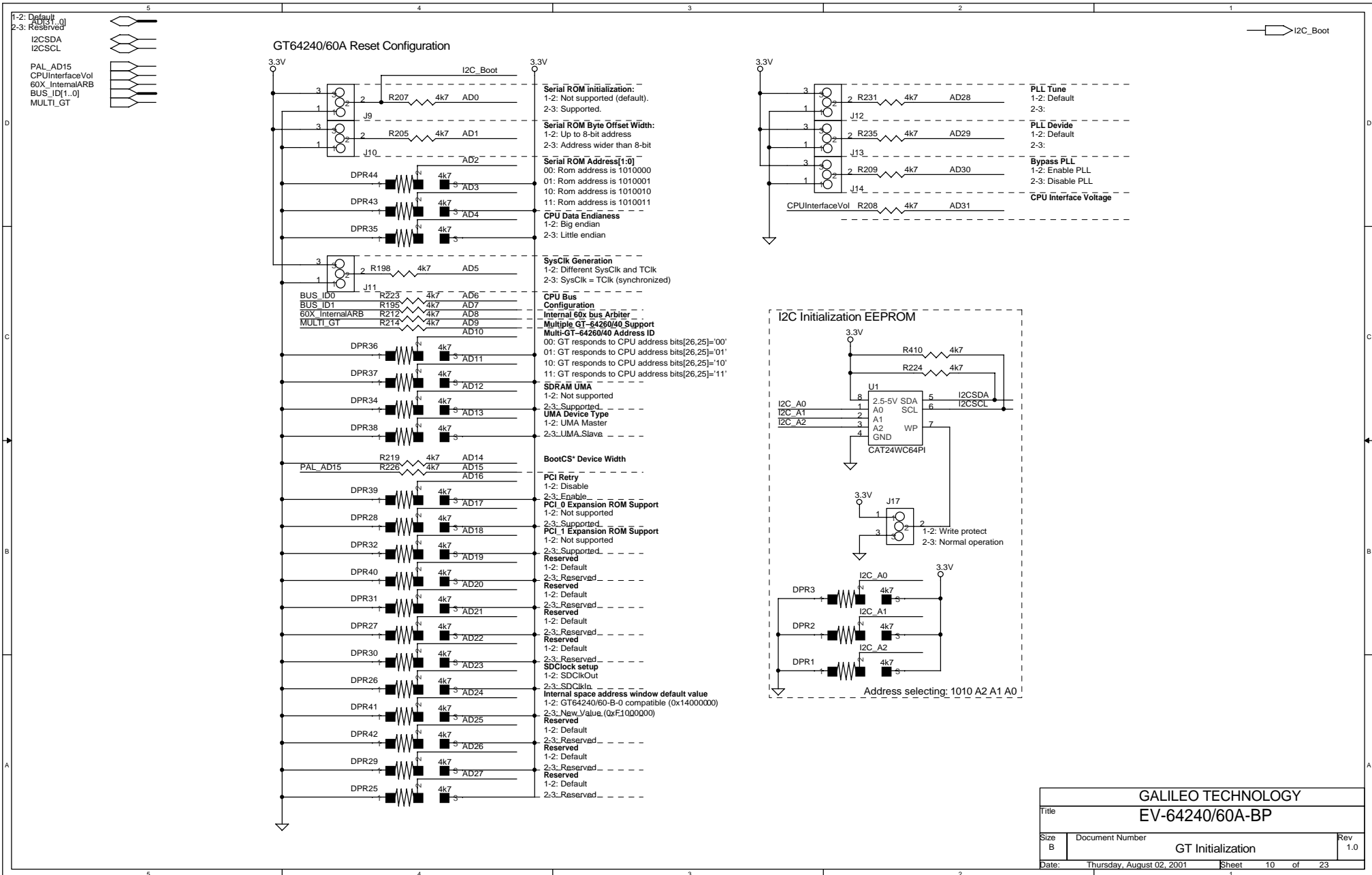


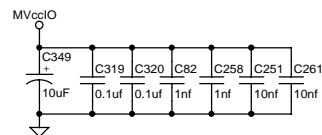
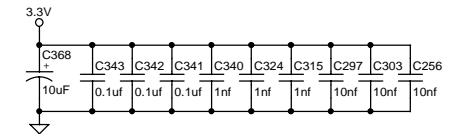
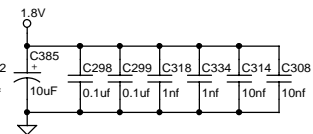
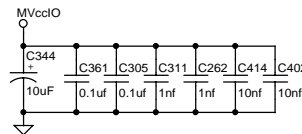
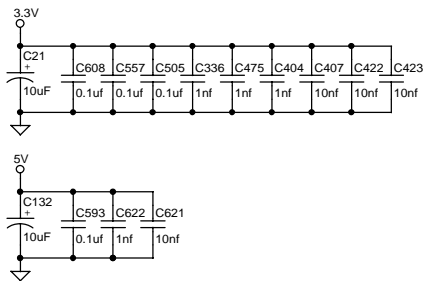
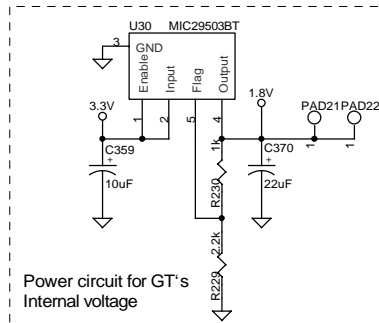






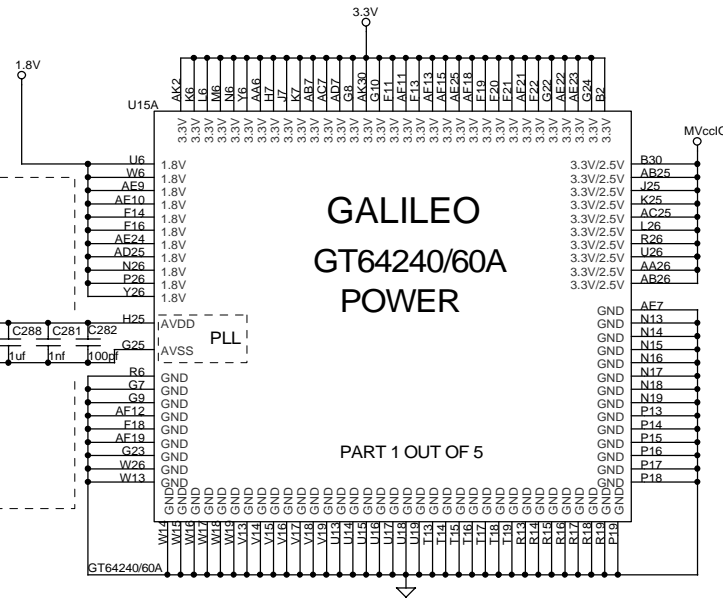
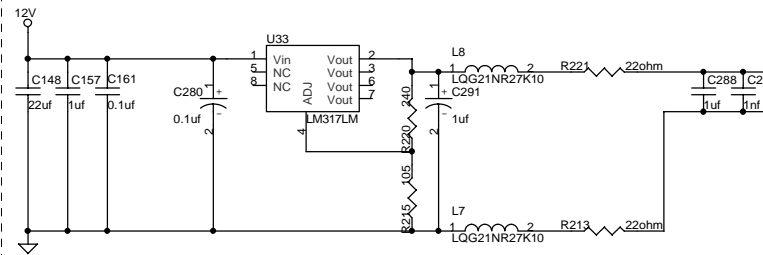






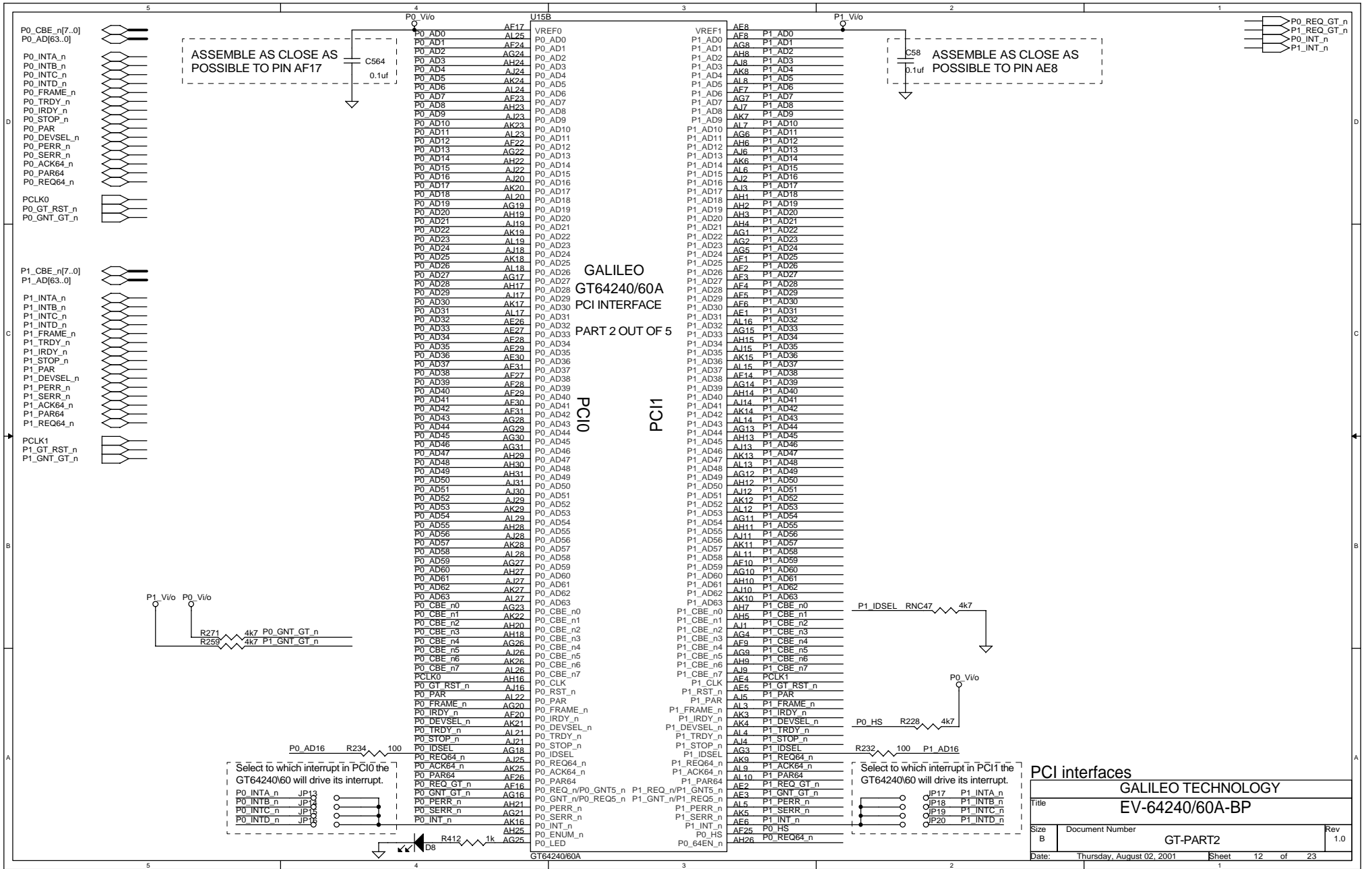
PLL FILTERING CIRCUIT

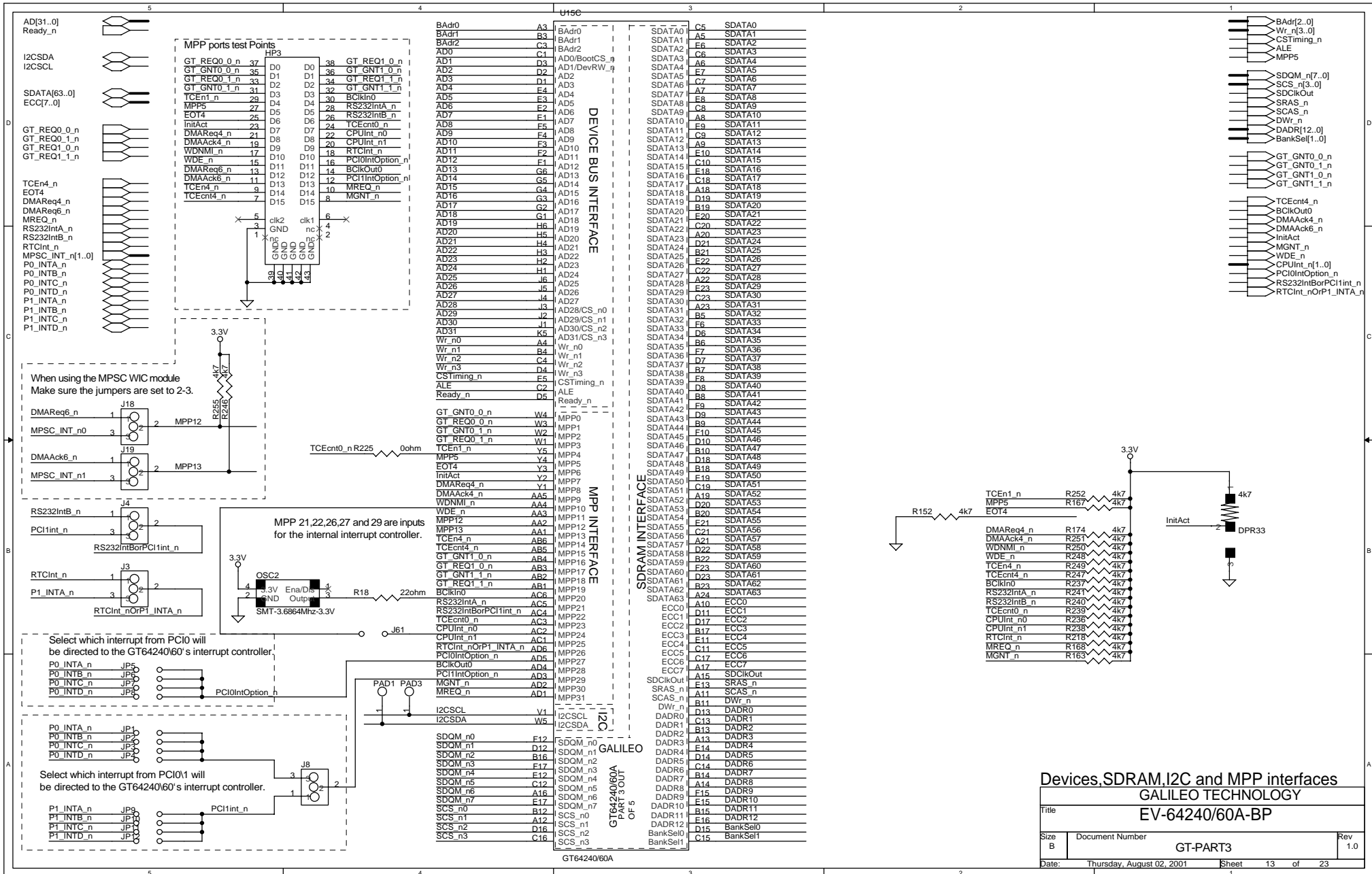
Please read carefully the layout application note for the PLL circuit in sheet number 16.



Power

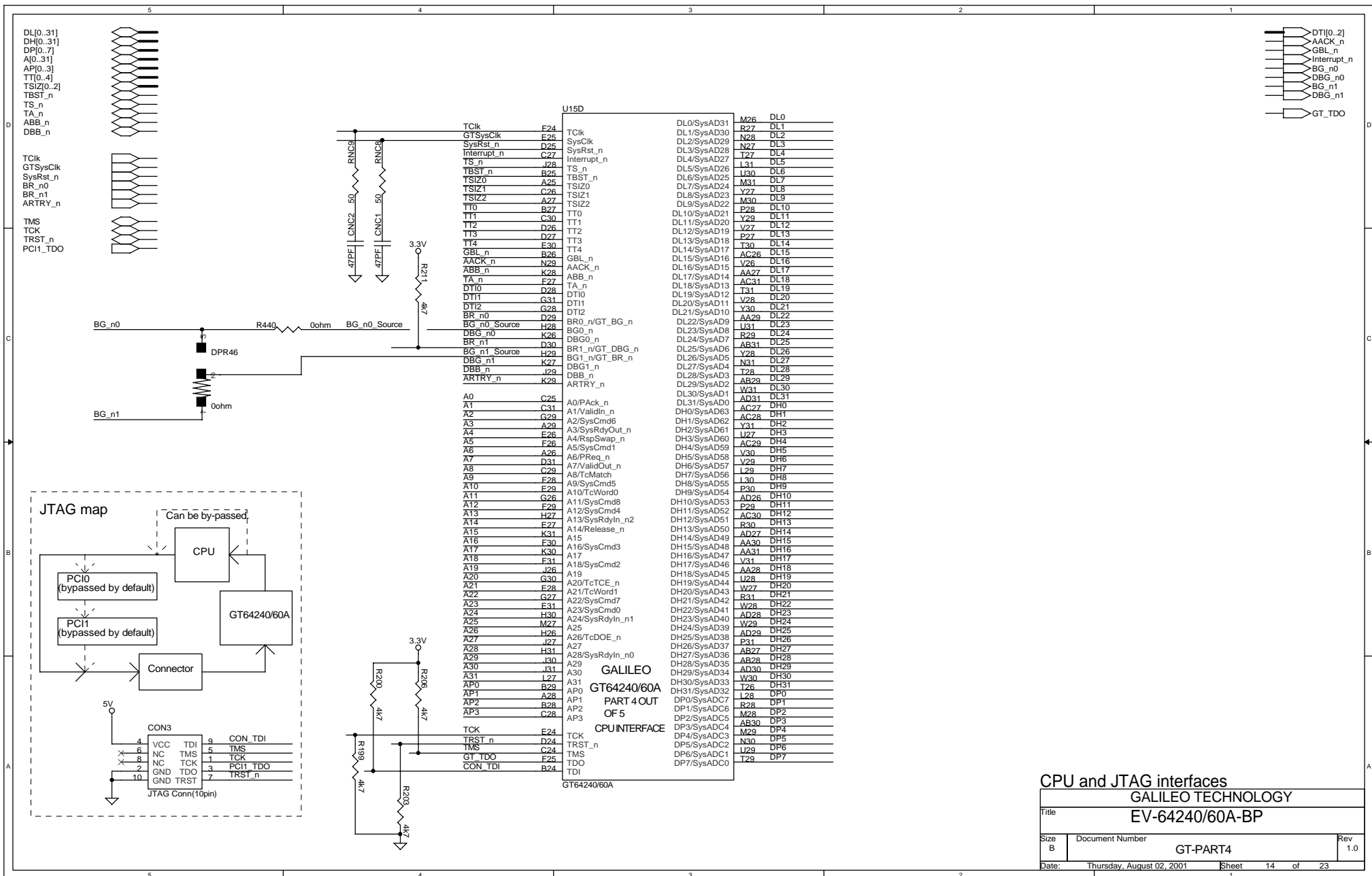
GALILEO TECHNOLOGY			
Title			
EV-64240/60A-BP			
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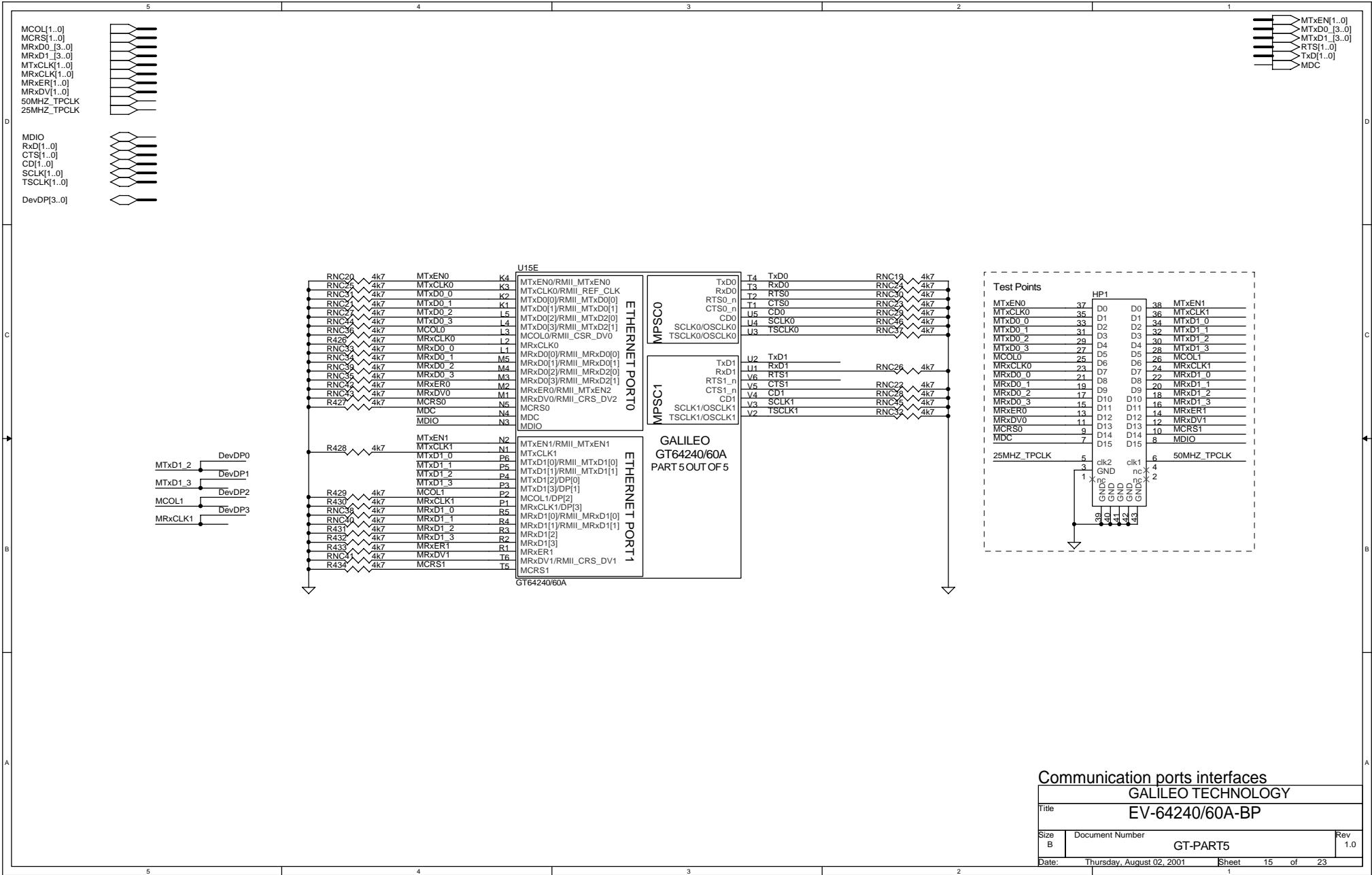




Devices,SDRAM,I2C and MPP interfaces	
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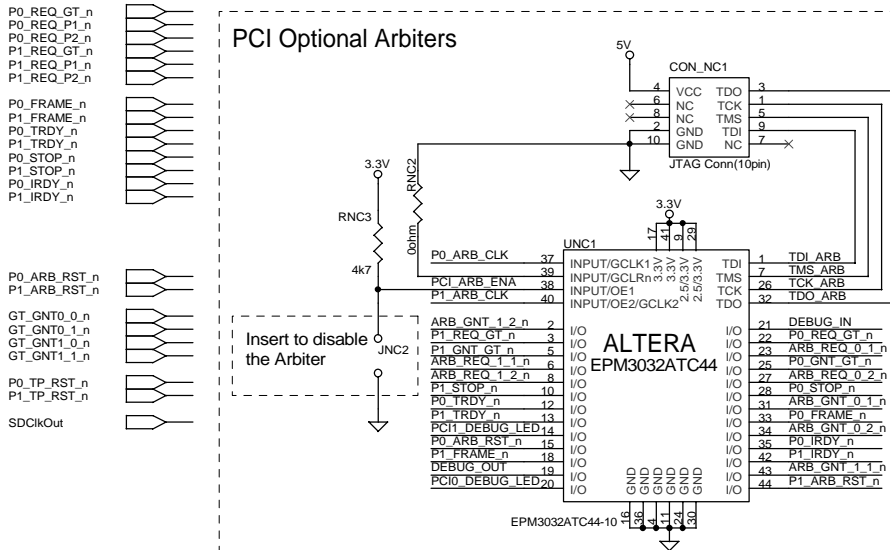
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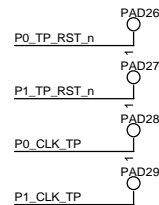
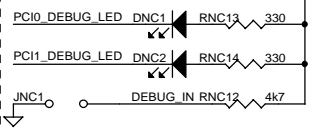


PCI Optional Arbiters

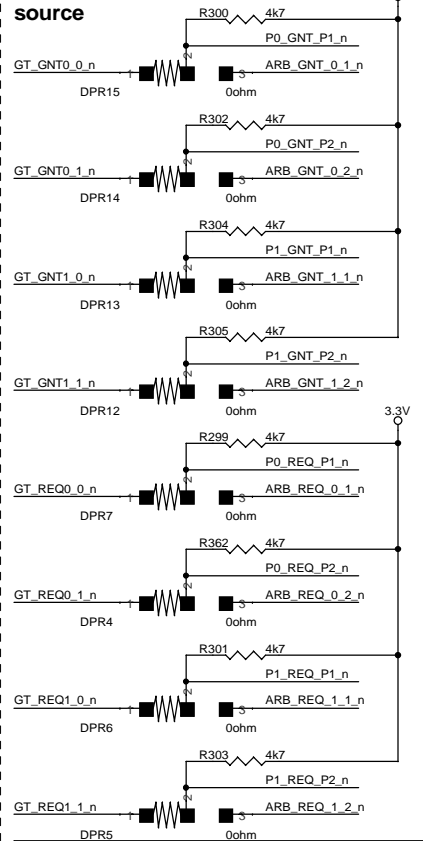
Insert to disable the Arbiter



PCI Debug

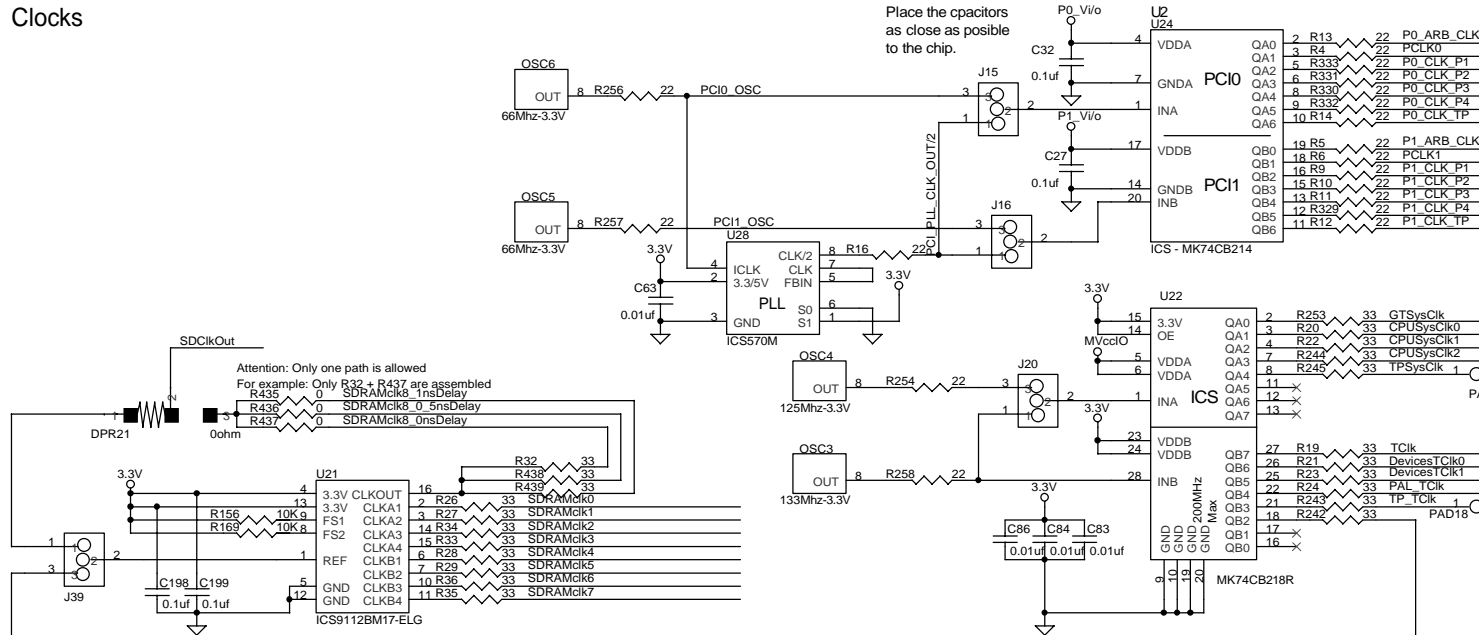


PCI Arbitration source



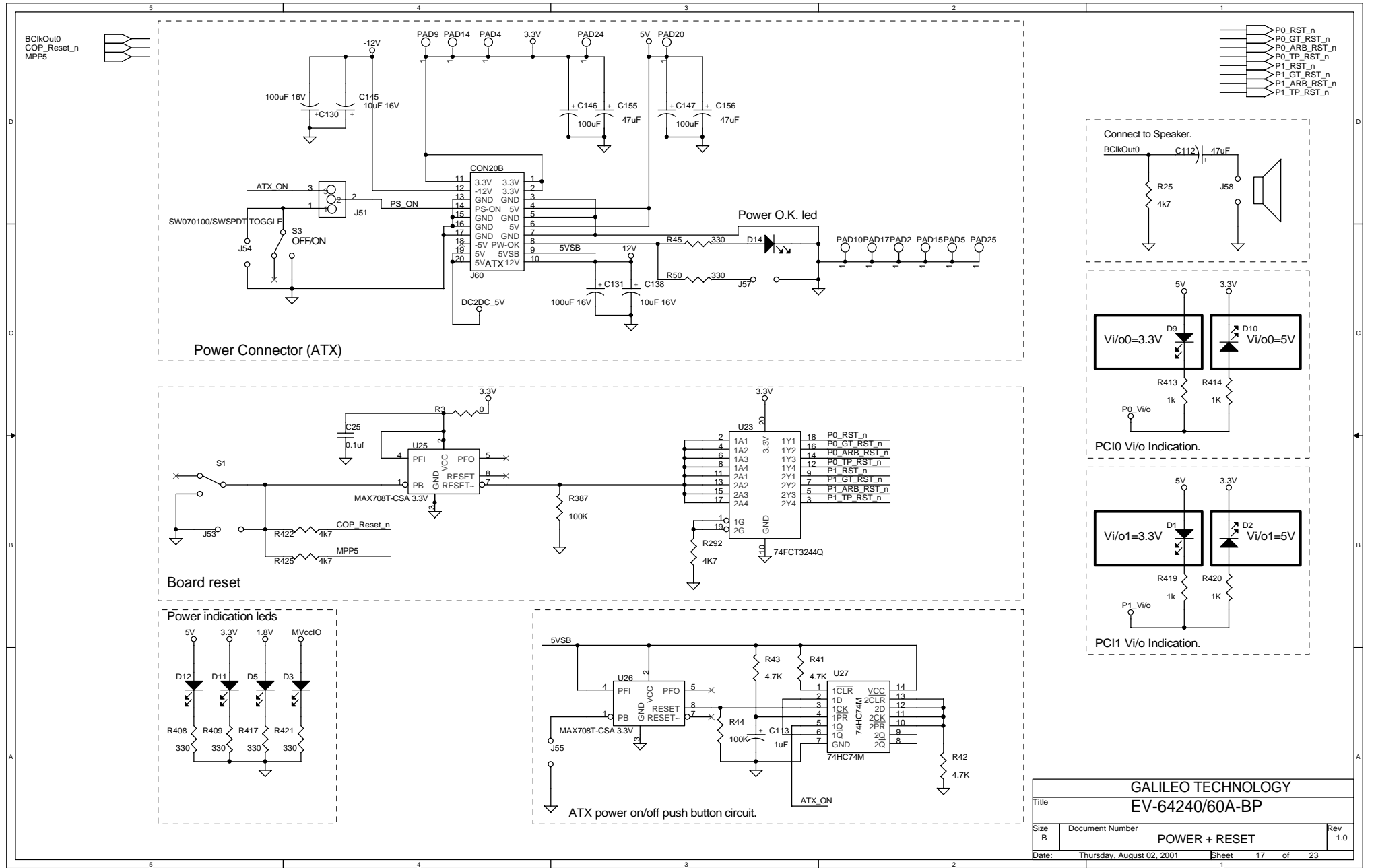
DPRs at : 1-2 => GT's Internal Arbiter
DPRs at : 2-3 => External Arbiter
Make sure to assemble the optional arbiter.

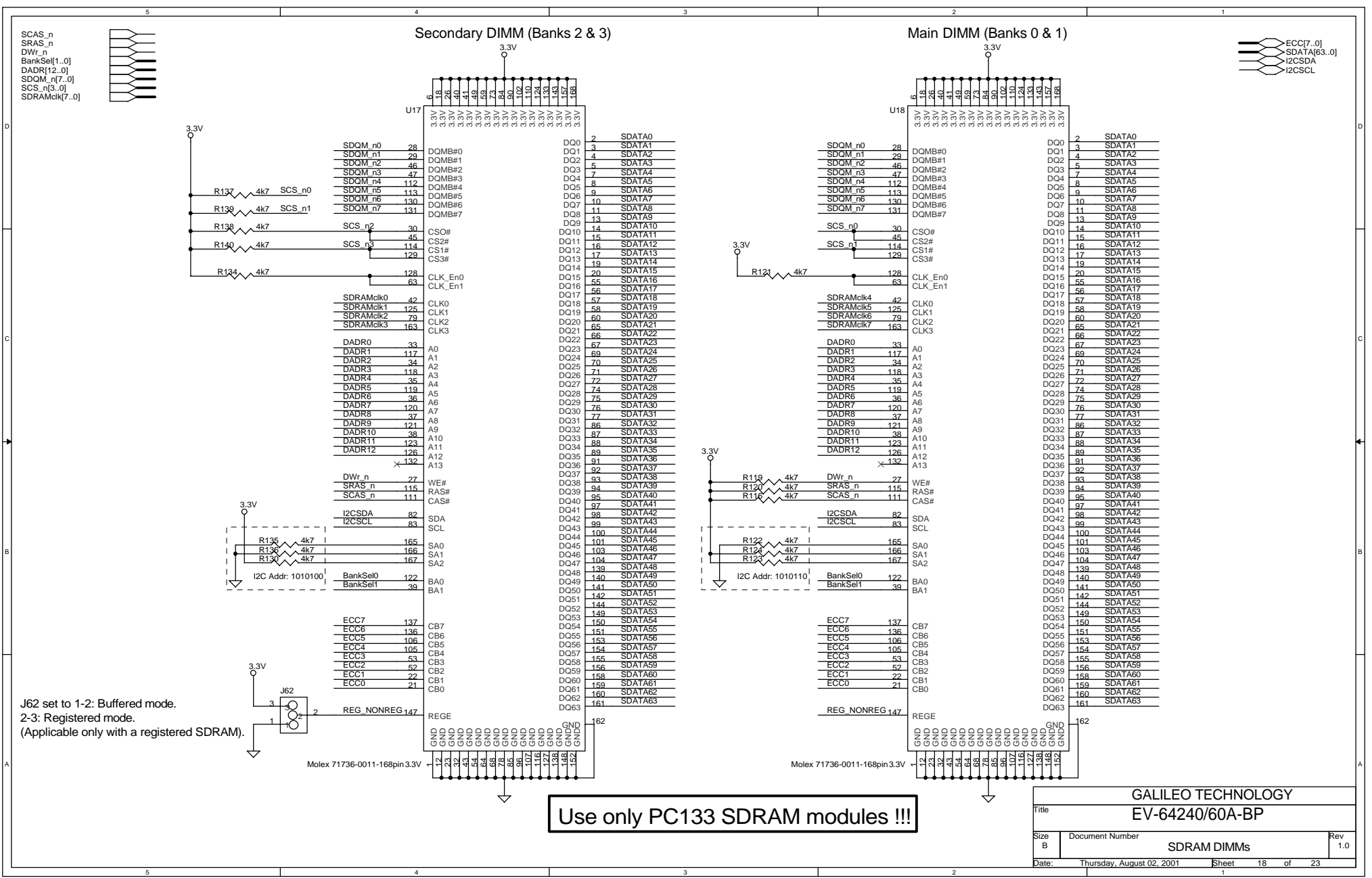
Clocks

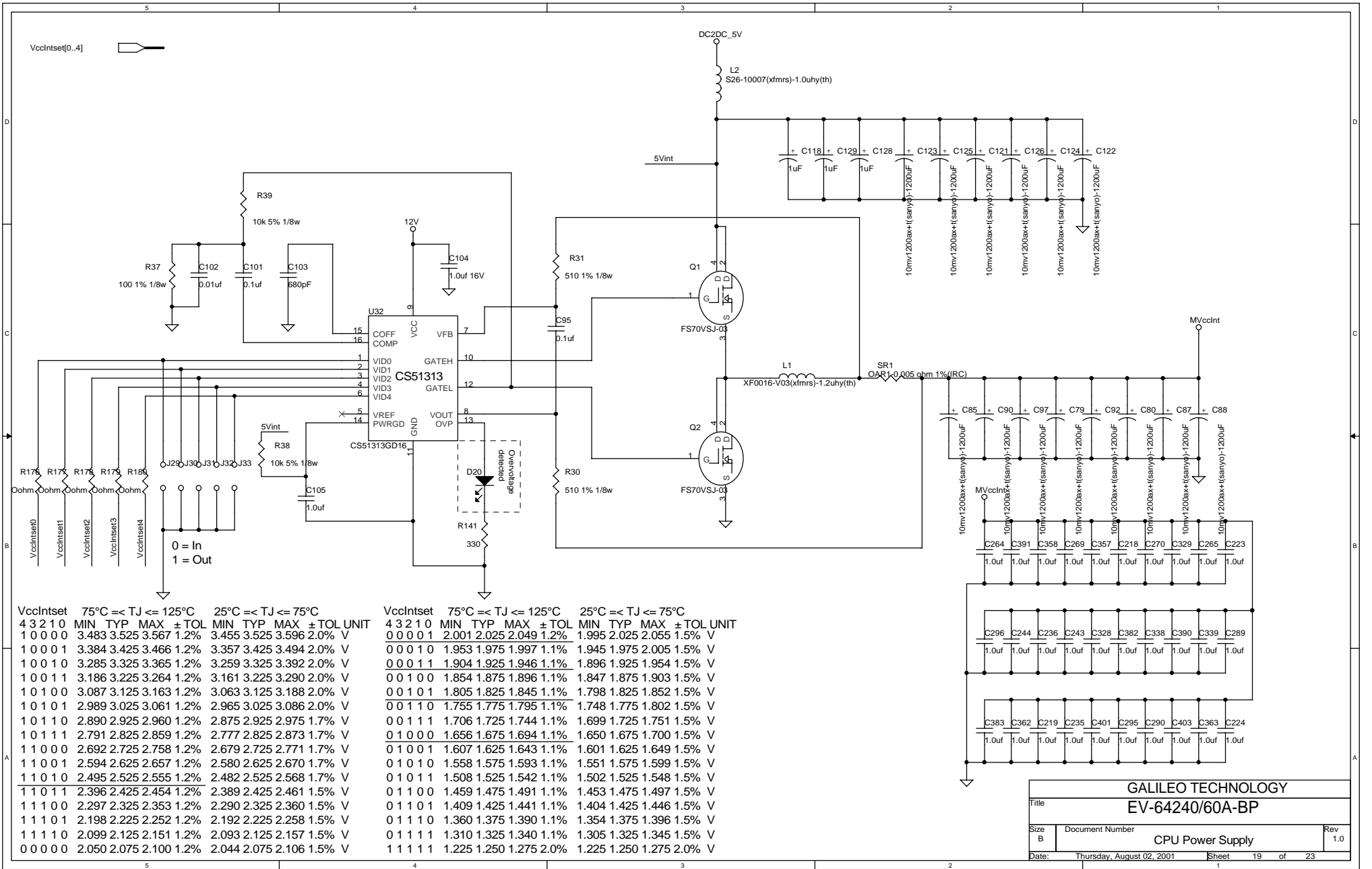


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EV-64240/60A-BP

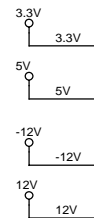
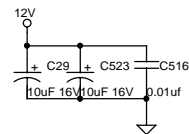
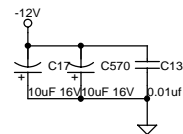
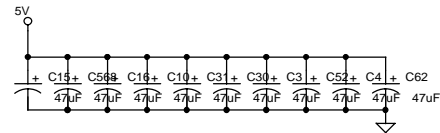
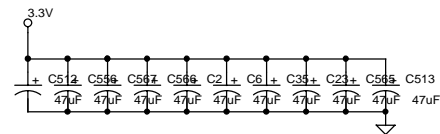
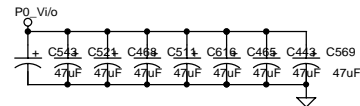
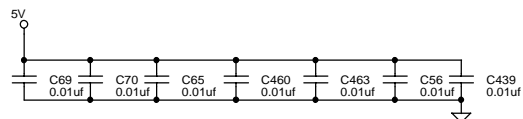
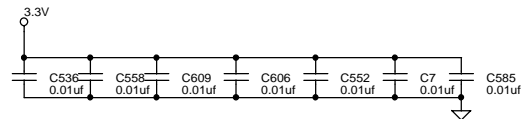
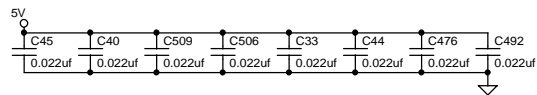
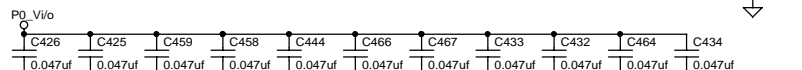
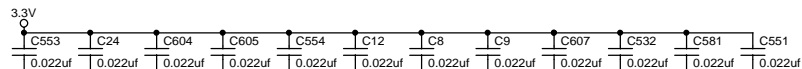
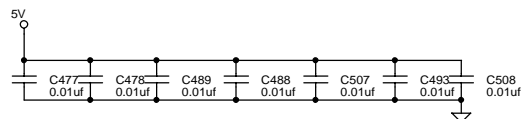
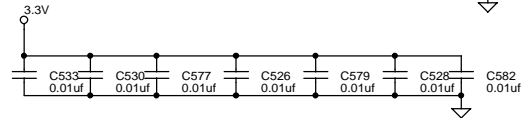
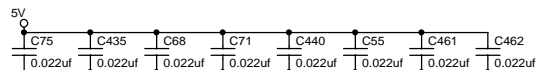
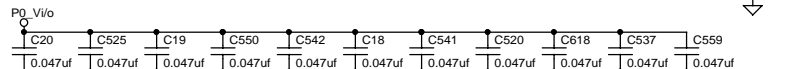
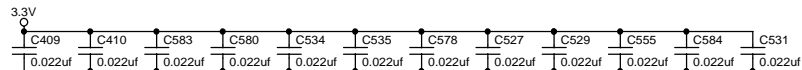
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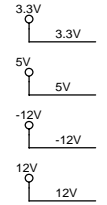
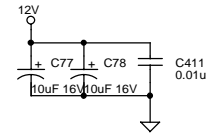
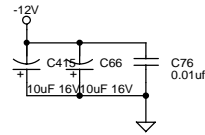
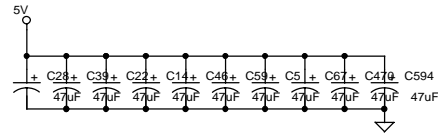
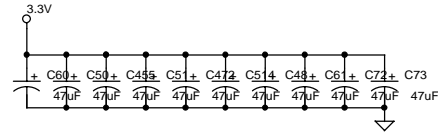
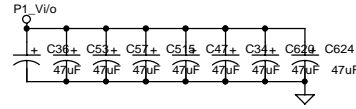
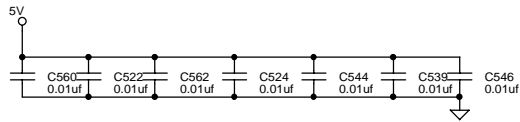
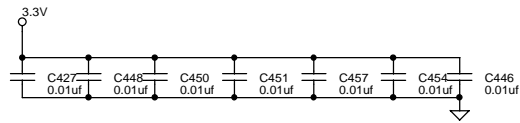
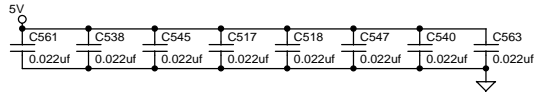
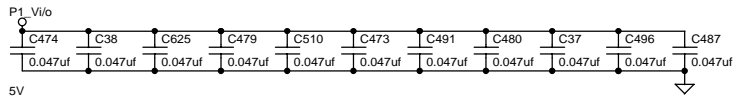
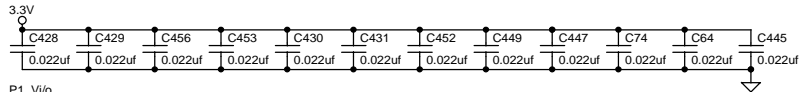
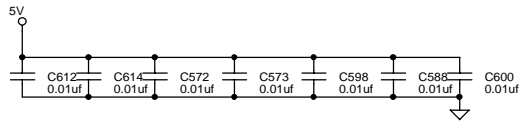
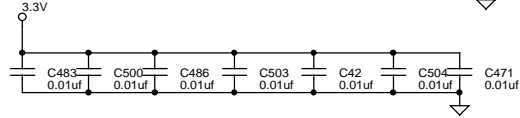
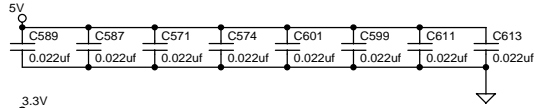
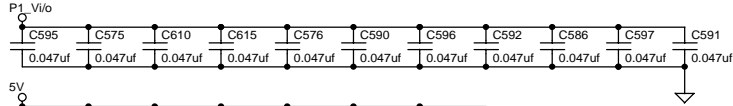
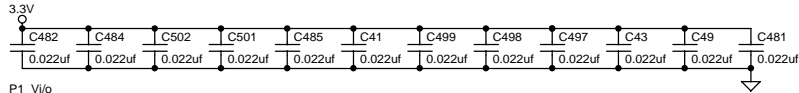


CAPACITORS TO BE CONNECTED TO THE 5V V/I/O AND 3.3V PINS
(AS CLOSE AS POSSIBLE AND NO MORE THEN 0.25")



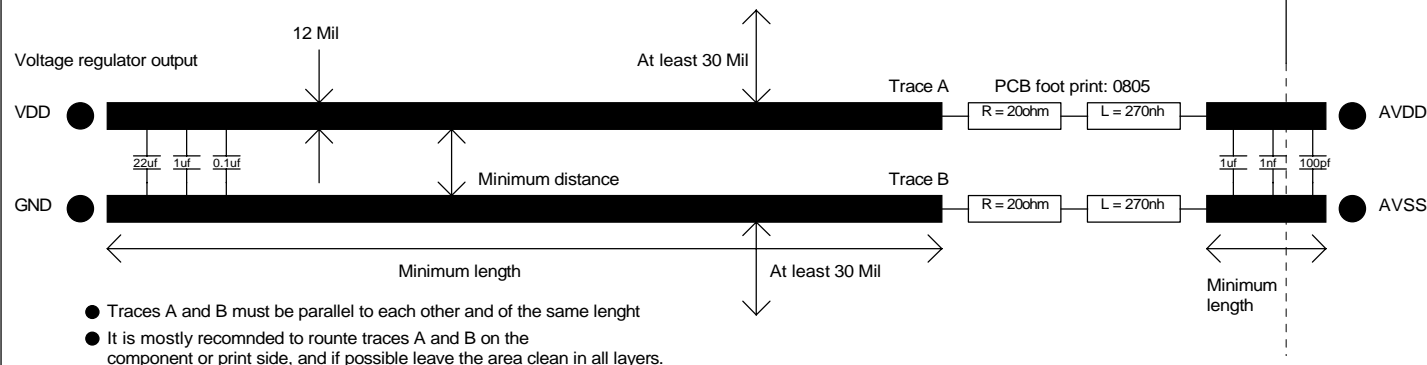
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CAPACITORS TO BE CONNECTED TO THE 5V V/I/O AND 3.3V PINS
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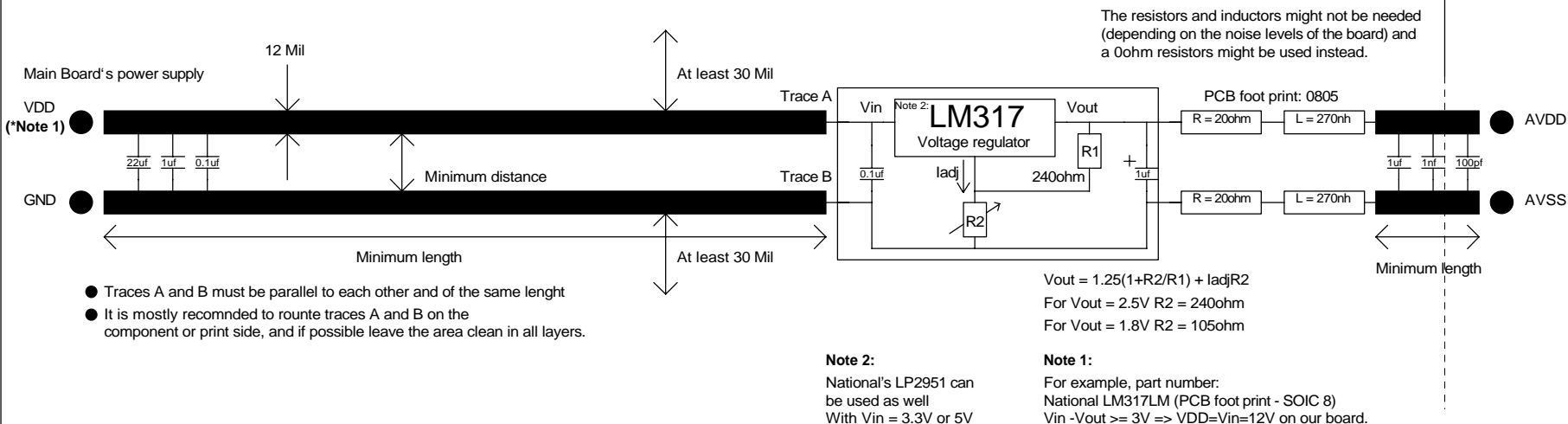


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Application note for a PCI add on card.



Application note for a back-plane layout



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