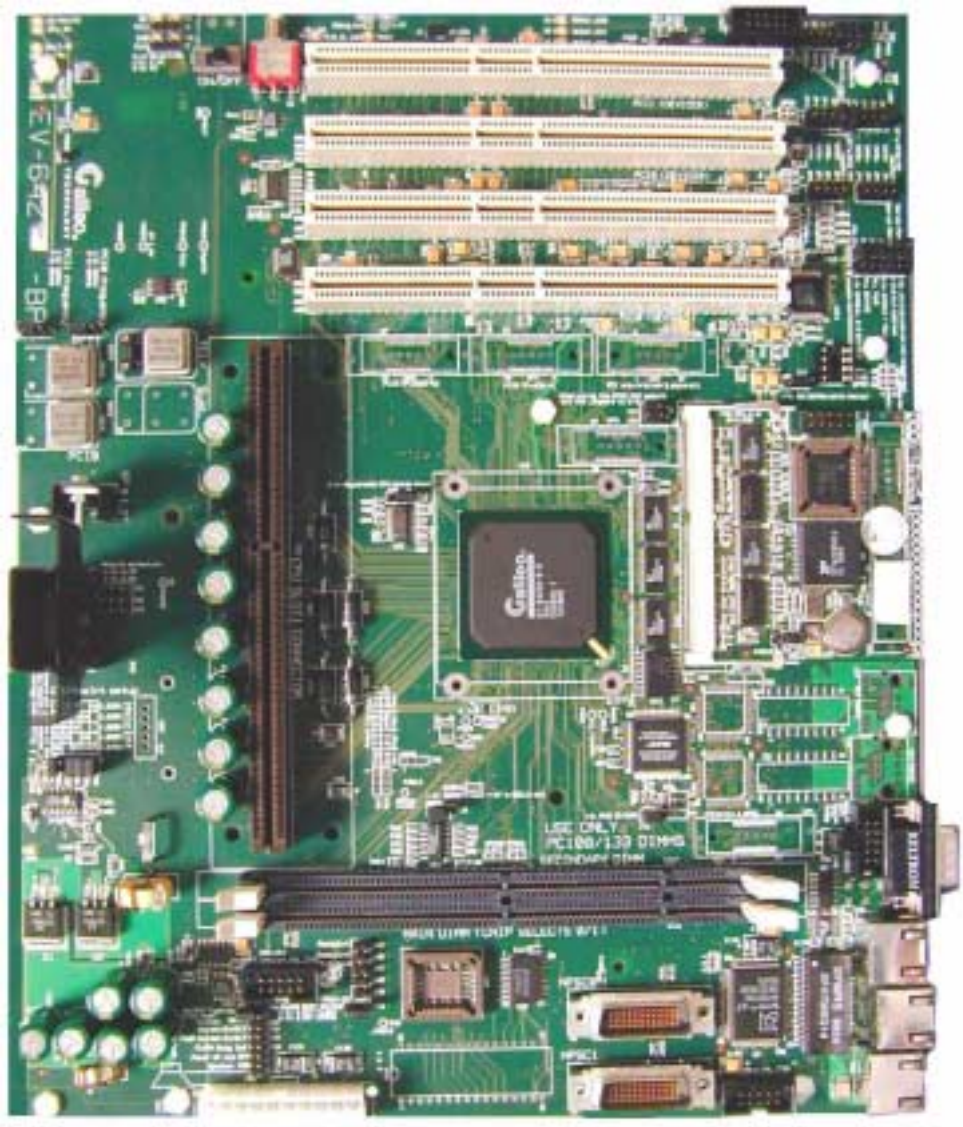
EV-64260A-BP
Development Platform for the GT-64260A

MV-L100016-10
September 23, 2001



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Marvell Semiconductor, Inc.
645 Almanor Avenue, Sunnyvale, CA 94085
Phone: (866) 674-7253, Fax: (408) 328-0122

Galileo Technology, Inc.
2350 Zanker Road, San Jose, CA 95131
Phone: (408) 367-1400, Fax: (408) 367-1401

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

The EV-64260A-BP Development Board was designed to evaluate Marvell's high-end GT-64260A CPU system controller. The EV-64260A-BP Development Board provides you with a reference design platform to begin system development prior to hardware availability.

1.1 EV-64260A-BP Components and Features

The features and components of the EV-64260A-BP Development Board are as follows:

- PPC processor support (Via SLOT1 connector):
  - Motorola MPC7410
  - Motorola MPC750
  - Motorola MPC7450
  - IBM 750L
  - IBM 750CXE
- Marvell's GT-64260A (133 MHz) system controller
  - Features Marvell's PPC system controller (133 MHz, with dual 64-bit, 66 MHz PCI buses)
- SDRAM (PC133) Memory support:
  - Dual Inline Memory Module (DIMM) sockets to support PC133-compliant (16, 64, 128, 256 or 512 MB device) modules. Up to 2 GB of memory, registered and non-registered modules
- Three 10/100 Ethernet ports:
  - 3 RMII Ethernet ports with LEDs for link and activity
- Four 64-bit PCI Expansion Slots:
  - Two slots are connected to PCI_0 of the GT-64260A and the other two are connected to PCI_1
- Two Multi Protocol Serial Channels (MPSC) connectors:
  - The GT-64260A incorporates two MPSC channels at 55 Mbps. Marvell has many modules designed for this connector to demonstrate the capabilities of the MPSC port. For more details about these modules, consult your distributor or FAE.
- Two COM ports connectors:
  - Can be driven by the device module's Dual UART or the GT-64260A's MPSCs
- I^2C EEPROM and interface:
  - The GT-64260A can be initialized from an I^2C EEPROM. It also has full I^2C master and slave capabilities. The I^2C bus is connected to two SDRAM DIMMs and to a connector which allows the attachment of devices external to the EV-64260A-BP.
- Onboard boot device:
  - You can boot from the device module boot device or from the onboard boot device. The onboard boot device can be either an 8-bit flash or an EEPROM which allows the use of a PromICE. For an example of a PromICE, see http://www.gei.com.
- Debug LEDs:
  - Three debug LEDs controlled by software or PCI accesses.
- External control:
  - The EV-64260A-BP can be installed in an ATX compatible PC case, which incorporates connectors for power (on/off), reset, power OK LED, and a speaker.

1.2 Shipping Contents

The EV-64260A-BP package is shipped with the following components.

- One EV-64260A-BP Development Board
- One CPU module
- One device module (EV-DEVICES-D144)
- Two SDRAM DIMMs

Note

Both DIMMs must be installed for proper operation.

Contact your distributor or local Marvell FAE if any of the above items are missing or damaged.

1.3 Related Documentation

See the Galileo Technology SLOT1 CPU Modules User Manual for additional information.

1.4 Additional Collateral

See our website, http://www.marvell for the following collateral:

- PLD equations
- Assembly map drawings
- EV-64260A-BP User Guide Errata
- Monitor Manuals
- Monitor Source Code
- Software Drivers
- BOM
- Block Diagram
- Galileo Technology SLOT1 CPU Modules User Guide
- Galileo Technology SLOT1 CPU Modules User Guide Errata
- A list of modules that work with this board

1.5 EV-64260A-BP Description

Figure 1 illustrates the main components on the board.

Figure 1: EV-64260A-BP Components

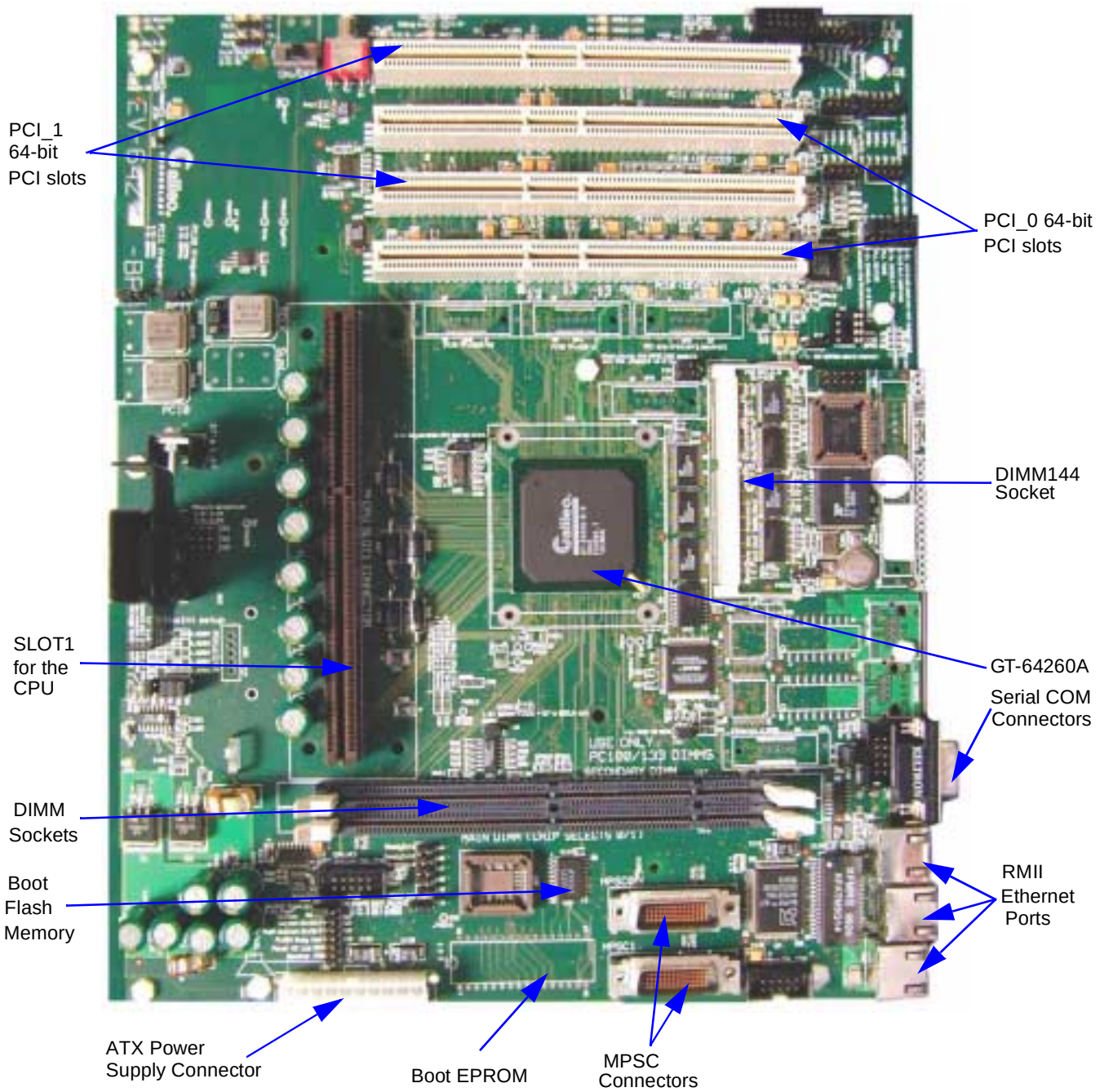
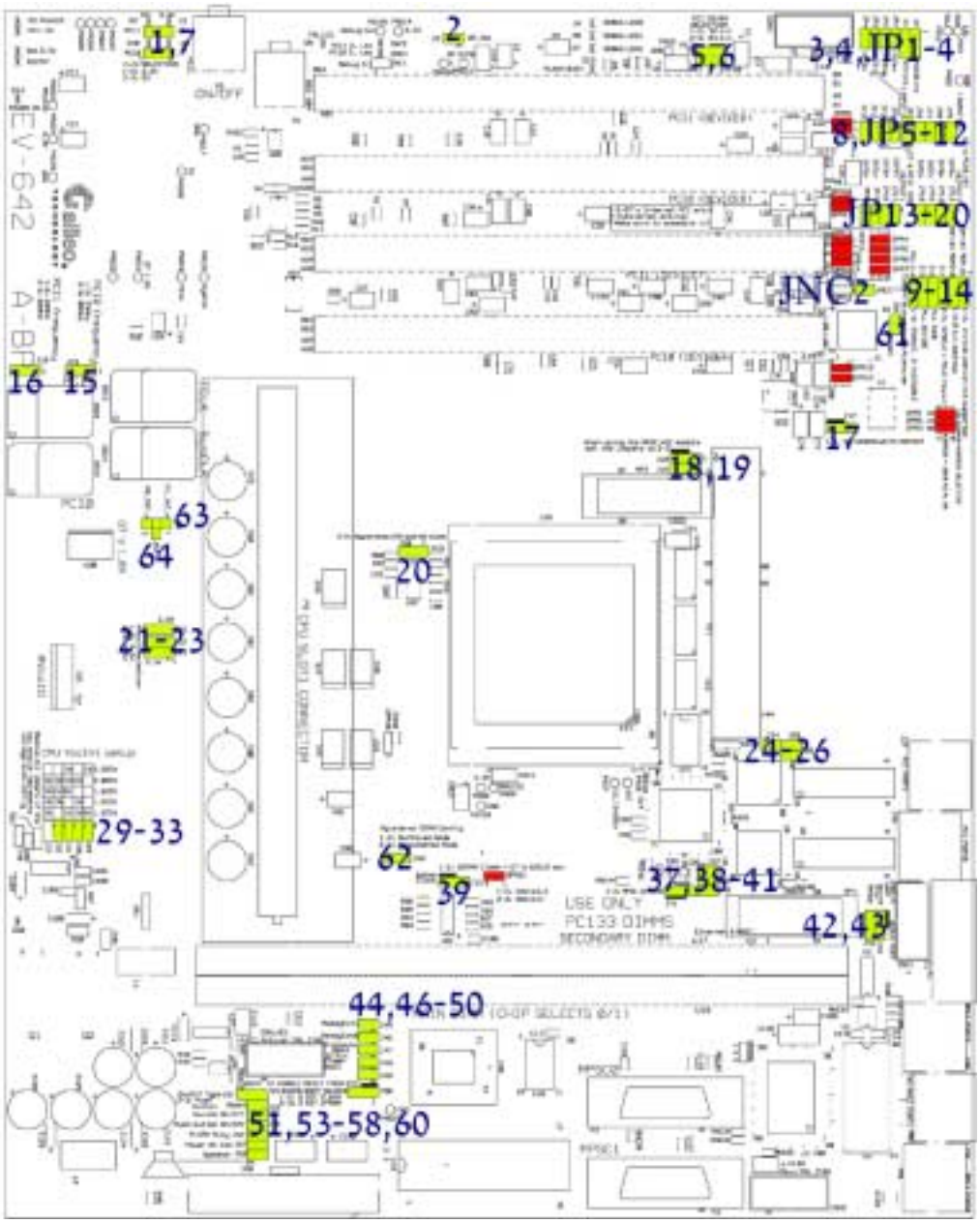


Figure 2 details the jumper locations.

Figure 2: EV-64260A-BP Jumper Location



2. Getting Started

The EV-64260A-BP is preconfigured and ready to run.

Note

Marvell recommends testing the board with this standard configuration before changing jumpers or other configuration options.

2.1 Additional Required Items

To use the EV-64260A-BP Development Board, you will need the following items which are not included in the board package:

- Null-modem cable, 9-pin (COM cable)
- ATX PC power supply
- Terminal emulation software, such as Windows 9x, or Windows NT HyperTerminal

3. Hardware Setup

The EV-64260A-BP expansion cards contain very delicate Integrated Circuits (ICs). To protect them against damage from static electricity, take the following precautions.

Caution

- Unplug the EV-64260A-BP power supply.
- Use a grounded wrist strap before handling EV-64260A-BP components. If you do not have one, touch your hands briefly to a safely grounded object or to a metal object, such as the power supply case, and then continue.
- Hold the components by the edges and try not to touch the ICs, connectors, or other components.
- Place components on a grounded anti-static pad or on the bag that came with the EV-64260A-BP.
- Ensure that the ATX power supply is switched off before you plug in or remove the ATX power connector on the EV-64260A-BP.

Take the following steps before applying power to the EV-64260A-BP:

1. Check the EV-64260A-BP settings. (See Section 3.1)
2. Install the memory modules. (See Section 3.3)
3. Install the CPU. (See Section 3.4.1)
4. Install the device module. (See Section 3.5)
5. Connect the RS-232 Null modem cable. (See Section 3.5)
6. Apply power to the EV-64260A-BP. (See Section 3.6)

3.1 EV-64260A-BP Feature Settings

The EV-64260A-BP features are adjusted via the jumpers or the DPRs. The DPRs are used for various functions. They are usually left at their default states.

DPRs are the same as 3-pad jumpers. The resistor can be placed on pads 1-2 or pads 2-3.

Table 1: COM Port Jumper/DPR Location

J/DPR	Default	Functionality	Remarks
J42 J43	1-2	1-2: The serial port source is the device module's UART. 2-3: The serial port source is the EV-64260A-BP's MPSC0 port (UART over MPSC).	J42 J43

Table 2: Internal Use DPR

J/DPR	Default	State	Remarks
DPR20	1-2	Internal use	N/A

Table 3: PCI_0 Jumpers and DPR

J/DPR	Default	Functionality	Remarks
J7	1-2 (3.3 V) on 3.3 V PCI boards. 2-3 (5V) on 5V PCI boards.	PCI0 Vi/o selection: 1-2: 3.3 V 2-3: 5 V	N/A
J6			N/A
DPR18 DPR19	1-2	PCI0 -P8 (device7) JTAG chain bypass: 1-2: Bypass 2-3: No bypass	N/A
DPR10 DPR11	1-2	PCI0 -P6 (device8) JTAG chain bypass: 1-2: Bypass 2-3: No bypass	N/A

Note

Refer to the schematics at http://www.marvell.com for the JTAG chain.

Table 4: PCI Arbitration Source Jumpers and DPRs

J/DPR	Default	Functionality	Remarks
DPR15 DPR14 DPR13 DPR12 DPR7 DPR4 DPR6 DPR5	1-2	PCI arbitration source: 1-2: GT-64260A's internal arbiter. 2-3: External arbiter.	To use the external arbiter, assemble the following: UNC1, CON_NC1, DNC1, DNC2, JNC1, JNC2, RNC2, RNC3, RNC12,13,14 and PAD16
JNC2	OUT	Insert to disable the external arbiter.	
JNC1	OUT	Debug-in for the external arbiter's Altera.	

Table 5: PCI Interrupt Jumpers

J/DPR	Default	Functionality
JP1	In	In: GT-64260A drives its PCI0 interrupt to PCI0 INTA_n

Table 5: PCI Interrupt Jumpers (Continued)

J/DPR	Default	Functionality
JP3	Out	In: GT-64260A drives its PCI0 interrupt to PCI0 INTB_n
JP5	In	In: GT-64260A drives its PCI0 interrupt to PCI0 INTC_n
JP7	Out	In: GT-64260A drives its PCI0 interrupt to PCI0 INTD_n
JP9	In	In: PCI0 INTA_n is forwarded to the GT.
JP10	Out	In: PCI0 INTB_n is forwarded to the GT.
JP11	Out	In: PCI0 INTC_n is forwarded to the GT.
JP12	Out	In: PCI0 INTD_n is forwarded to the GT

Table 6: I^2C Jumpers/DPRs

J/DPR	Default	Functionality
J17	2-3	I^2C Initialization EEPROM write policy 1-2: Write protect 2-3: Write enable
DPR3 DPR2 DPR1	1-2	I^2C Initialization EEPROM address selecting Address (7-bit wide) selecting: 1010 A2 A1 A0 (A2 = DPR1, A1=DPR2 and A0=DPR3) 1-2: 0 2-3: 1

Table 7: CPU JTAG Chain Bypass DPR

J/DPR	Default	Functionality
DPR45	1-2	1-2: Bypass 2-3: No bypass

Table 8: I^2C Serial ROM Initialization

J/DPR	Default	Functionality
J9	1-2	Serial ROM initialization: (The ROM address is 1010000) 1-2: Not supported (default) 2-3: Supported
J10	2-3	Serial ROM Byte Offset Width: 1-2: Up to 8-bit address 2-3: The address is wider than 8-bits

Table 8: I^2C Serial ROM Initialization (Continued)

J/DPR	Default	Functionality
DPR44 DPR43	1-2	Serial ROM Address[1:0]: 00: ROM address is 1010000 01: ROM address is 1010001 10: ROM address is 1010010 11: ROM address is 1010011

Note

See the schematics at http://www.marvell.com for more information

Table 9: GT-64260A Jumpers/DPRs

J/DPR	Default	Functionality
J11	Determined by CPU type.	SysClk Generation 1-2: Different SysClk and TClk 2-3: SysClk = TClk (synchronized)
DPR36 DPR37	1-2	Multi-GT-64260A Address ID 00: GT responds to CPU address bits[26,25]='00' 01: GT responds to CPU address bits[26,25]='01' 10: GT responds to CPU address bits[26,25]='10' 11: GT responds to CPU address bits[26,25]='11'
DPR34	1-2	SDRAM UMA 1-2: Not supported 2-3: Supported
DPR38	1-2	UMA Device Type 1-2: UMA Master 2-3: UMA Slave
DPR39	1-2	PCI Retry 1-2: Disable 2-3: Enable
DPR28	1-2	PCI_0 Expansion ROM Support 1-2: Not supported 2-3: Supported
DPR41	1-2	Internal Space Address Window Default Value 1-2: GT-64240/60 - B0 Compatible (0x1400:0000) 2-3: New Value 0xF100:0000
DPR26	1-2	SDClock Setup 1-2: SDClkOut 2-3: SDClkIn
J12	1-2 (Pull down)	PLL Tune

Table 9: GT-64260A Jumpers/DPRs (Continued)

J/DPR	Default	Functionality
J13	1-2 (Pull down)	PLL Divide
J14	1-2	Bypass PLL 1-2: Enable PLL 2-3: Disable PLL

Note

See the schematics at http://www.marvell for more information.

Table 10: Devices and Boot Option Jumpers

J/DPR	Default	Functionality	Remarks
J49	Out	Insert to enable reset from the RTC.	N/A
J48	Out	Insert to swap between the 32-bit FLASH memory chip select and the 8-bit FLASH memory chip select.	N/A
J47	Out	Insert to boot from 8-bit FLASH memory on the device module.	N/A
J50	1-2	On board boot source: 1-2: Onboard boot from 8-bit Flash (U20) 2-3: Onboard boot from 8-bit EPROM (U19)	Applicable only if J47 is OUT.
J46 J44	Out	ReadyExt0 ReadyExt1 Ready extension (in clocks) 0 0 No extension (Ready_n = GND) 1 0 16 + 4 clocks 0 1 16 + 8 clocks 1 1 16 + 16 clocks	For test purposes only. Do not use.
J2	Out	Used for debugging.	N/A

Table 11: SDRAM Table

J/DPR	Default	Functionality
J62	2-3	Registered DIMM configuration 1-2: Buffered Mode 2-3: Register Mode

Table 12: Connectors for a PC ATX-Case

J/DPR	Default	Functionality
J51	1-2	Power on/off type 1-2: On/Off switch (J54 is active) 2-3: Push button (J55 is active)
J53		External Reset
J54		External Power on/off switch
J55		External Power on/off (push button type)
J57		Power OK LED
J56		Flash busy LED (connect to the HD LED on the PC case)
J58		External speaker

Table 13: Watchdog Non-Maskable Interrupt (NMI)

J/DPR	Default	Functionality	Remarks
J61	Out	IN: GT-64260A's Watchdog NMI is directed to MPP 24 and the CPU module's CPUInt_n0. NOTE: For more information, refer to the schematics.	MPP24 must be configured as input.

Table 14: CPU I/O Interface Voltage Setting

J/DPR	Default	Functionality	Remarks
J21/J22/ J23	Deter-mined by CPU type.	1-2: 3.3V 2-3: 2.5V	N/A

3.2 Board Frequency and Clock Settings

Table 15: CPU Interface Clock Synchronization

J/DPR	Default	Functionality
J20	Deter-mined by CPU type.	1-2: Synchronized clocks for the CPU interface and GT-64260A. 2-3: Non-Synchronized clocks for the CPU interface and GT-64260A.

Table 16: SDclkOut/In Options

J/DPR	Default	Functionality	Remarks
DPR21	1-2	SDclkOut/SDclkIn options 1-2: SDclkIn 2-3: SDclkOut	The GT must be con-figured accordingly.
J39	2-3	SDRAM Clock Source 1-2: GT's SDClockOut (DPR 21 must be set to 2-3) 2-3: Oscillator	

Table 17: PCI_0 Frequency Setting

J/DPR	Default	Functionality	Remarks
J15	2-3	1-2: 33 MHz 2-3: 66 MHz	N/A

Table 18: PCI_1 Frequency Setting

J/DPR	Default	Functionality	Remarks
J16	2-3	1-2: 33 MHz 2-3: 66 MHz	N/A

3.3 System Memory (DIMM)

The EV-64260A-BP only uses Dual Inline Memory Modules (DIMMs). (Two sockets are available for 3.3 V (power level) unbuffered or registered Synchronous Dynamic Random Access Memory (SDRAM) of 8, 16, 32, 64, 128, 256, 512, or 1024 MB to form a memory size between 8 MB to 2 GB. The GT-64260A memory interface supports 16, 64, 128, 256, or 512 Mb devices.

Notes

- Only use SDRAMs that are compatible with the current PC133 SDRAM specification.
- Do not mix registered SDRAMs with unbuffered ones.
- When using registered SDRAM, configure the GT-64260A prior to the CPU access to the SDRAM.
- Always insert two DIMMs to acheive 133 MHz operation.
- When using only one memory module, install it in the main socket (U18). (For low frequencies only.)

- When using two memory modules, install the bigger one in the main module.

3.4 CPU Module

The EV-64260A-BP provides a SLOT1 connector for a CPU module.

3.4.1 CPU Module Installation Procedure

Take the following steps to install the CPU module:

1. Before installing a CPU module, read the respective module manual. Pay particular attention to the CPU multiplication ratio and permitted frequencies. Failure to do so may cause permanent damage to the CPU.
2. Insert the CPU module by holding it on both sides. Make sure you install the module firmly in place. There are two parallel rows of pins in the SLOT1 connector. Make sure there is no space between the card and SLOT1.

Warning

- Do not try to insert a CPU module that is not designed for the EV-64260A-BP.
- Make sure there is sufficient air circulation across the processor's heat sink.
- You must set the jumpers on the backplane according to the module used.

Note

Refer to the Galileo Technology SLOT1 CPU Modules User Manual for more information.

3.5 Device Modules

The EV-64260A-BP Development Board has an S0-DIMM144 connector for device modules. You can design your own module for development purposes or use Marvell's device module. (See Appendix A.)

Warning

- Do not try to insert modules not designed for the EV-64260A-BP.
- Avoid touching the battery, as this might cause time and data loss in the RTC's NVRAM.

3.5.1 Installing Device Modules

Take the following steps to install the Devices modules:

1. Hold the device module on both sides and insert it into the connector at a 45 degree angle. Push it towards the EV-64260A-BP and make sure the two racks on the sides of the connector lock it in place.
2. Use a plastic screw to tighten the module to the EV-64260A-BP.

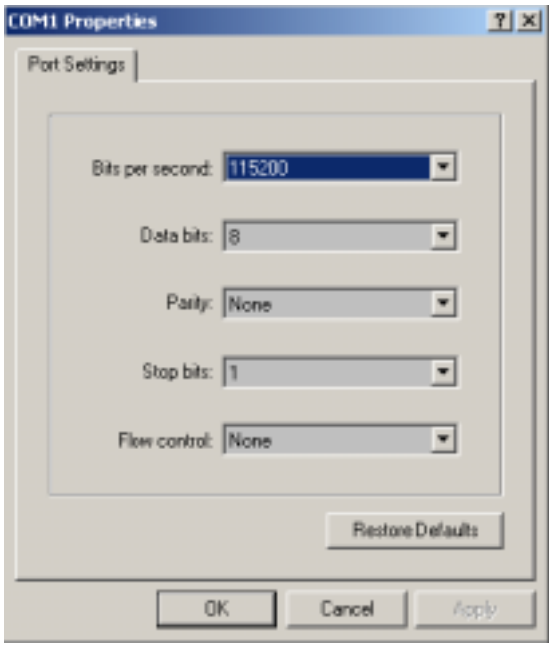
3.6 Applying Power to the EV-64260A-BP

The EV-64260A-BP uses a hyperterminal for communication with the system. You will need an RS232 cable and a PC which runs a hyperterminal application.Take the following steps to apply power to the board:

1. Be sure that all power switches are off.
2. Connect the power supply cord connector to the ATX header on the board.
3. Connect the RS232 cable to the COM1 port on the EV-64260A-BP and to the PC's COM port.
4. Open the hyperterminal window. You will see a File Menu on your PC screen.

5. From the File menu, select File|Properties.
6. In the Properties dialog box, click Configure, and confirm that the displayed parameters match the parameters in Figure 3.
7. Click OK.
8. From the File Menu, Choose File. Follow the instructions below.

Figure 3: COM1 Properties Dialog Box



9. Turn on the power. The operating system's logo appears in the Main window. The power LEDs on the EV-64260A-BP turn on. If for some reason, one of LEDs does not turn on immediately, turn the power off. Check that the CPU module is fully assembled in the SLOT1 socket, and that the power supply cord is firmly inserted in the ATX connector.

4. Software

The EV-64260A-BP is shipped with DINK32 Operating System. You can download software to the EV-64260A-BP via the hyper-terminal or by using one of the Ethernet ports in conjunction with various application provided by Marvell.

Note

The list of commands will be listed in the PMON manual in the near future.

4.1 GT-64260A Drivers

To ease the process of software development, Marvell has developed low-level drivers for the EV-64260A-BP. You can download these drivers from our website at http://www.marvell.com.

4.1.1 Other Operating Systems

Marvell currently supplies VxWorks for the EV-64260A-BP. A Linux version is in the development stage.

Appendix A. EV-DEVICES-D144

The EV-DEVICES-D144 module demonstrates how Marvell chips connect seamlessly with different devices, such as the EV-64260A-BP Development Board.

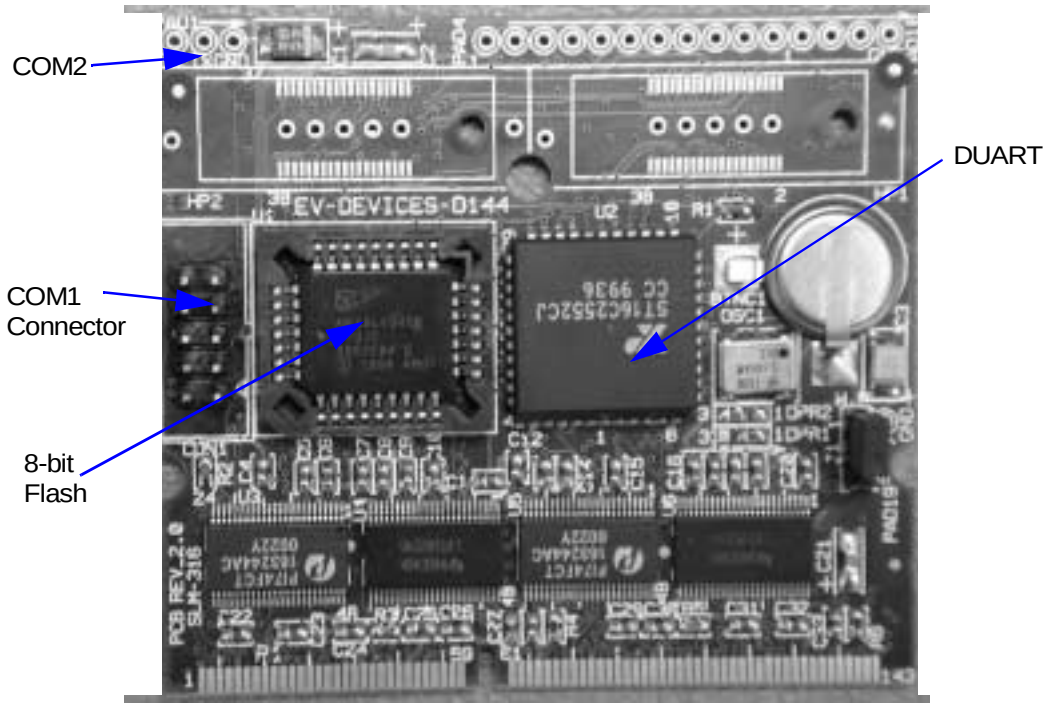
The EV-DEVICES-D144 module has the following features:

- SRAM
  - up to 2 MB, 32-bit wide device (ships with 1 MB)
  - up to 133 MHz
- Flash
  - Intel's Strata Flash-16 MB, 32-bit wide device (up to 64 MB)
- Boot flash
  - 0.5 MB (8-bit wide device)
- R.T.C (Real Time Clock)
  - This chip includes Non-volatile ROM memory (256 Byte NVRAM) (DS-DALLAS DS1501WE)
- 16552 DUART RS232
  - Two RS-232 serial channels

A.1 Description

Figure 4 details the main components of the module.

Figure 4: The EV-DEVICES-D144 Module Components



A.2 Jumpers and DPRs

The EV-DEVICES-D144 module has two DPRs which are illustrated in Table 19.

Jumper J1 for FLASH write protect has the following properties:

- 1-2 Default
- 2-3 Write protect. If the jumper is in this position, you cannot write to, or erase the chip.

Do not touch the battery or pin 4 of U8 (R.T.C) to avoid corrupting the data.

Table 19: DPR Settings for Various Memory Configurations

DPR1	DPR2	DESCRIPTION
1-2	1-2	2 MB - Micron 512 x 18 T-version
1-2	2-3	2 MB - Micron 512 x 18 S-version
1-2	2-3	2 MB - IDT 512 x 18
1-2	2-3	1 MB - Micron 256 x 18 (default configuration)
1-2	2-3	1 MB - IDT 256 x 18
2-3	x	For internal use only. (Test the 16-bit device, 256 x 18-microns.)

Appendix B. Revision History

Table 20: Revision History

Document Type	Rev. #	Date	Comments
First Release	Rev. A	September 23, 2001	Document was given Marvell Document number MV-L100016-10.