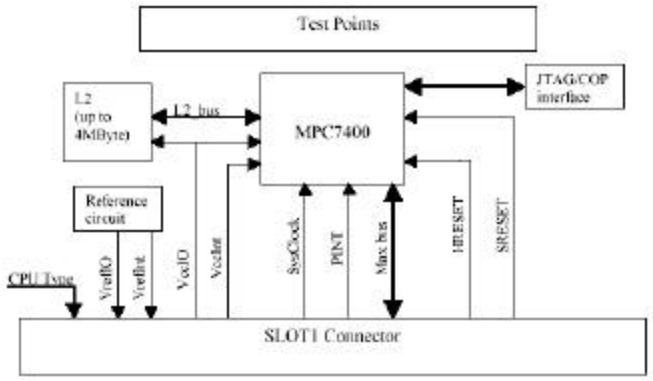
Main

EV-MPC7400-S1 Block Diagram



Notes:

1. The G4 support only up to 2Mbyte L2 backside cache but it has a reserved pin to support 4MByte L2 cache.
2. HRESET and SRESET are generated at the PLD on the EV-64240/60.
3. The test point will not include the L2 backside cache signals.
4. Two different regulators on the EV-64240/60 will generate the VccIO and VccInt.
5. VccInt = 1.8 volts determined by VrefInt.
6. VccIO = 3.3 or 2.5 volts depend on CPU type DC spec. determined by VrefIO.

Layout and routing instructions:

1. Use split power plane to connect VccInt from power supply to CPU.
2. Avoid routing traces across CPUPLL bus.
3. Keep PLL power supply filters near the MPC7400, use heavy and short traces from filter to pins.
4. Use short and equal-length traces from MPC7400 to SRAM address and data pins.
5. Rout SYNCIN → SYNCOUT path to equal longest cache address, data or control lines. This should be the CLOCKA and CLOCKB length too.
6. Surround MPC7400 with bypass capacitors to provide additional ground returns paths.
7. Insure COP pin numbering matches the schematics.
8. Place cache SRAMs within 3.5 cm of MPC7400 (center to center). Surround each component with bypass capacitors.
9. Use thick traces for power supply to L2 cache SRAMs.

Sheet Number:	Content:
1	Info page
2	Module - Top hierarchy.
3	MPC7400 - Top hierarchy.
4	MPC7400 - CPU interface.
5	MPC7400 - L2 cache interface.
6	Module configurations
7	Decoupeling capacitors.
8	SLOT1 connector
9	L2 cache data SRAM
Rev Number 0.9	Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.91	HP1 was added to support the Agilent (HP) Emulation and Analysis in conjunction with the test points on the EV-64260BP. Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.92	schematics for production (after rename). Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 1.0	Production release. Please make sure you have latest revision when referencing this schematic.
Rev Number 2.0	1. All YC199-J103JR were replaced with YCN15-103JR 2. COP_HRESET signal was connected to SLOT1 3. Fixed signal integrity on JTAG interface. 4. BVSEL can be connected to HRESET. 5. no-DRTRY support with DTI1 6. CPU_TRST signal is tied to (HRESET & TRST) 7. Support 5-pin power supply configuration. Production release. Please make sure you have latest revision when referencing this schematic.

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Title: EV-MPC7400/750-S1		
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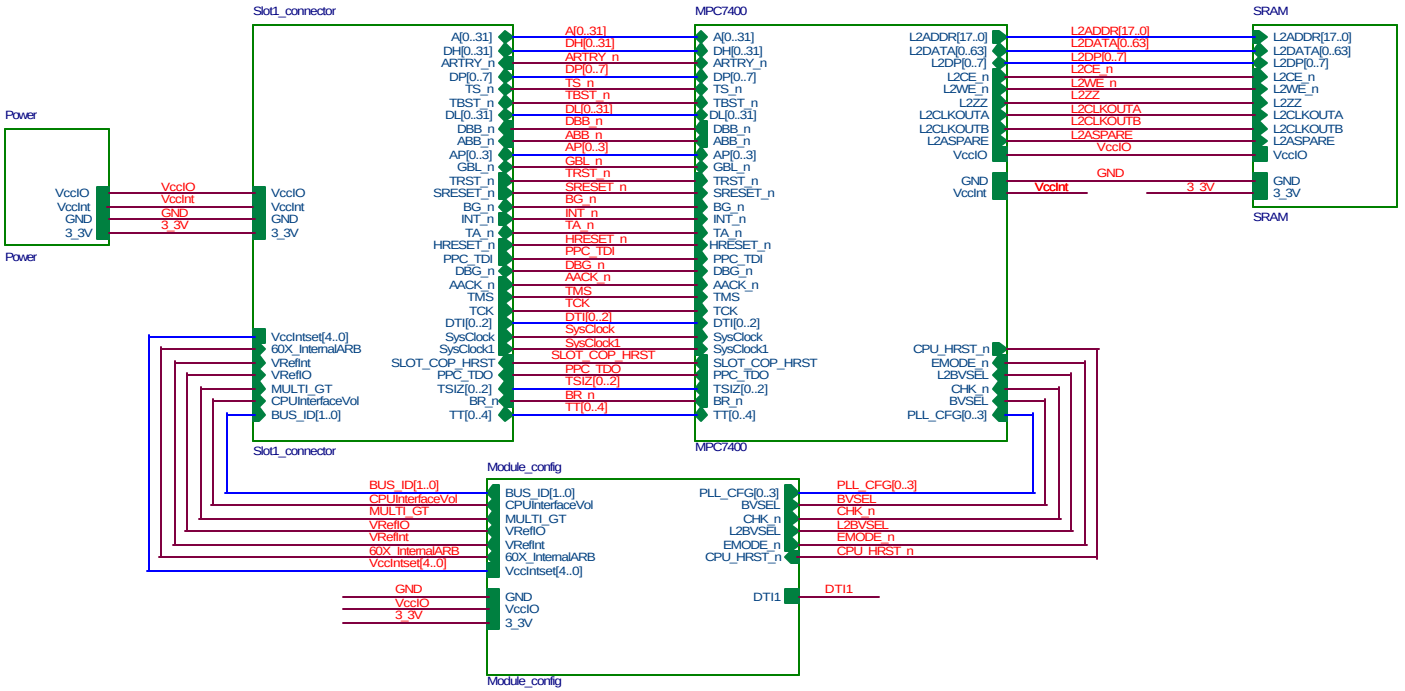

Galileo Technology		
Title: EV-MPC7400/750-S1		
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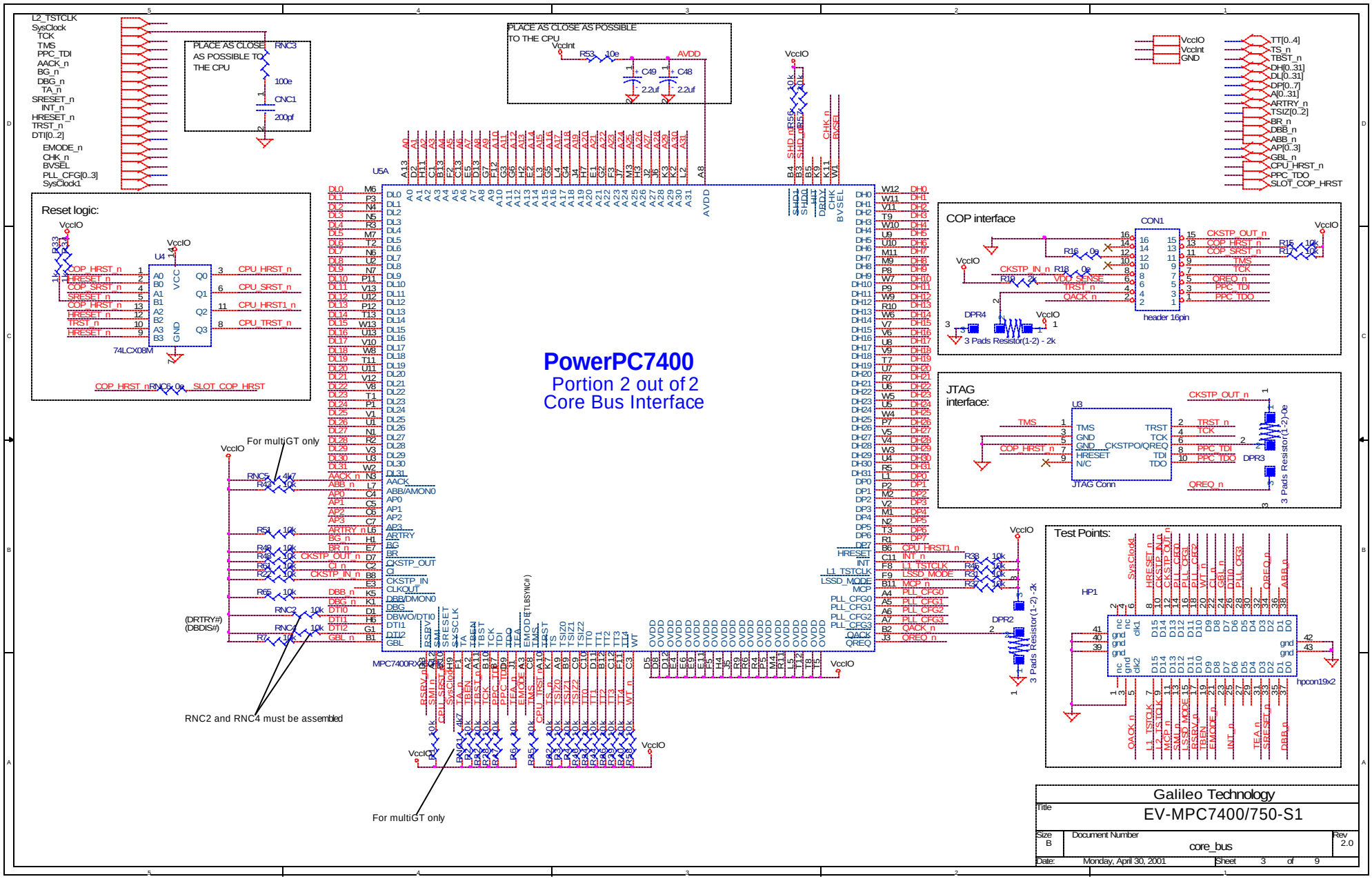
PowerPC7400
Portion 2 out of 2
Core Bus Interface
U5A
MPC7400RX
Reset logic:
U4
74LCX08M
COP interface
CON1
header 16pin
JTAG interface:
U3
JTAG Conn
Test Points:
HP1
hpcon19x2
PLACE AS CLOSE AS POSSIBLE TO THE CPU
RNC2 and RNC4 must be assembled
For multiGT only
3 Pads Resistor(1-2) - 2k
3 Pads Resistor(1-2)-0e
Galileo Technology
EV-MPC7400/750-S1
core_bus
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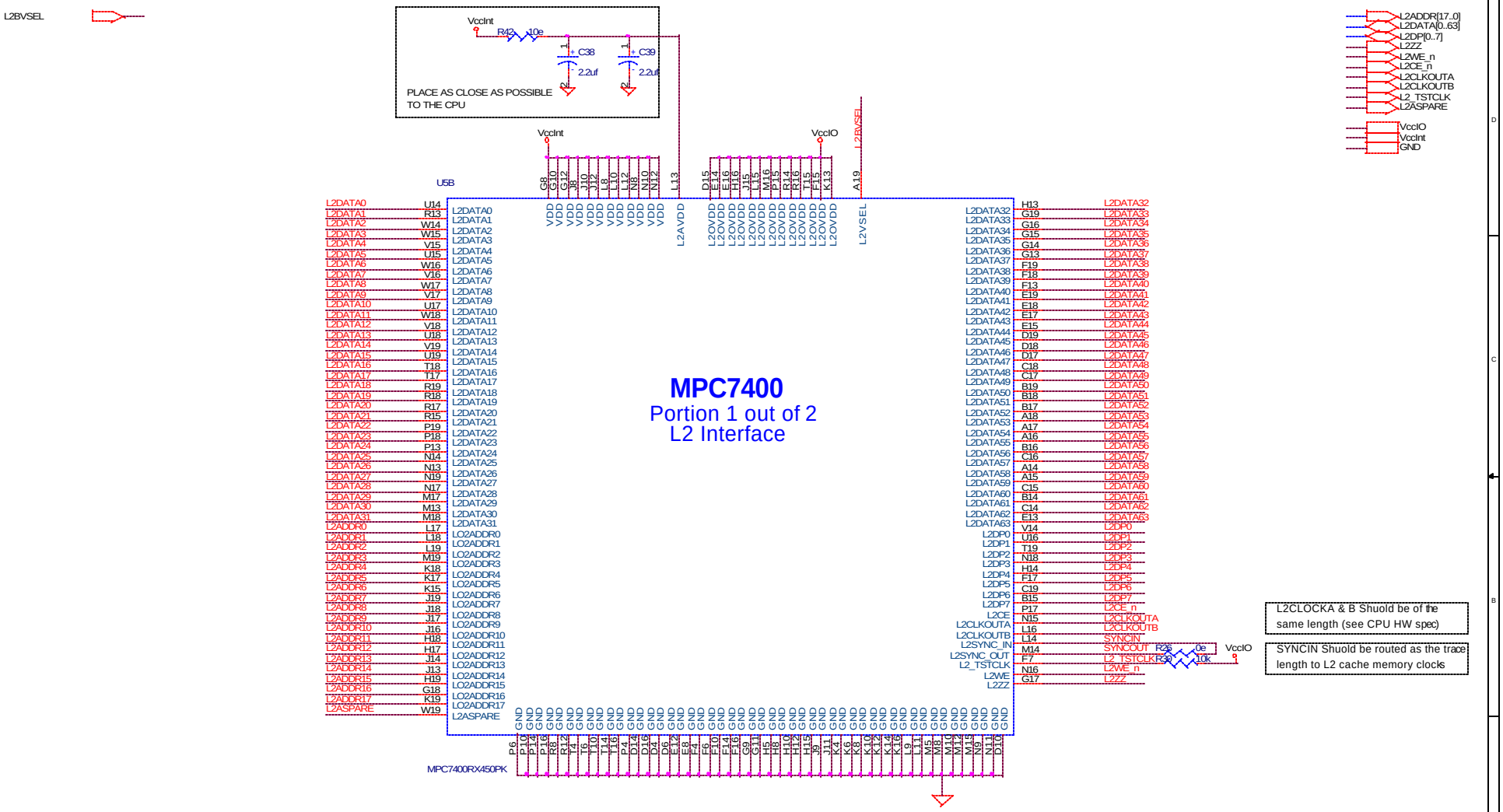
L2BVSEL
VccInt
R42 10e
C38 2.2uf
C39 2.2uf
PLACE AS CLOSE AS POSSIBLE TO THE CPU
L2ADDR[17..0]
L2DATA[0..63]
L2DP[0..7]
L2ZZ
L2WE_n
L2CE_n
L2CLKOUTA
L2CLKOUTB
L2_TSTCLK
L2ASPARE
VccIO
VccInt
GND
U5B
MPC7400
Portion 1 out of 2
L2 Interface
MPC7400RX450PK
L2CLOCKA & B Shuold be of the same length (see CPU HW spec)
SYNCIN Shuold be routed as the trace length to L2 cache memory clocks
R26 0e
10k
Galileo Technology
EV-MPC7400/750-S1
L2_bus
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CPU_HRST_n

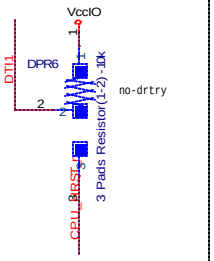
VccIO
GND
3_3V
VccIntset[4..0]

EMODE_n
DTI1
PLL_CFG[0..3]

BUS_ID[1..0]
CPUInterfaceVol
VRefIO
VRefInt
60X_InternalARB

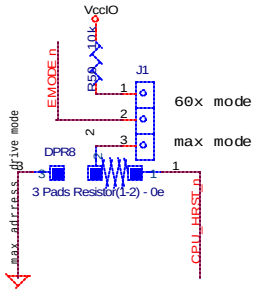
PLL_CFG[0..3]
BVSEL
CHK_n
L2BVSEL
MULTI_GT

MPC750 no-DRTRY mode selection:



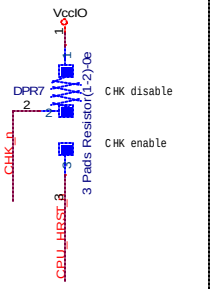
When the MPC750 is in no-DRTRY mode, data can not be cancled the cycle after it is aknowledged by the assertion of TA.

CPU bus mode selection:



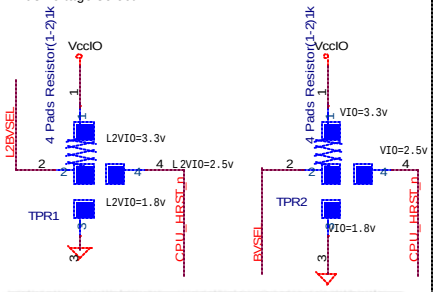
Address bus drive mode cause the G4 to drive the address bus whenever BG is asserted independet of whether G4 has a bus transaction to run or not.

CPU post power on reset internal test selection:



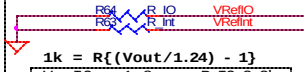
A post power on reset internal memory test and initiolization can beselected by tying CHK to HRESET, for normal operation tie CHK high.

Bus voltage select:



BVSEL	L2VSEL	CPU interface voltage	L2 interface voltage
0	0	1.8V	1.8V
0	1	1.8V	3.3V
0	HRESET	1.8V	2.5V
1	0	3.3V	1.8V
1	1	3.3V	3.3V
1	HRESET	3.3V	2.5V

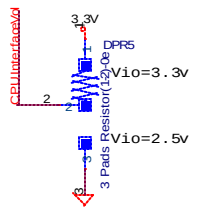
Power supply voltage selection:



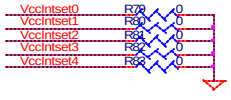

```
1k = R{(Vout/1.24) - 1}
VccIO = 1.8v => R_IO=2.2k
VccIO = 2.5v => R_IO=1k
VccIO = 3.3v => R_IO=0.6k

VccInt = 1.8v => R_Int=2.2k
VccInt = 2.5v => R_Int=1k
VccInt = 3.3v => R_Int=0.6k
```

GT64240's CPU interface voltage selection:

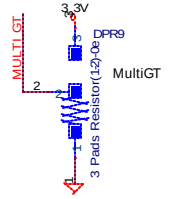


CPU power selction - configuration depends on CPU internal voltage



VccInt	R83	R82	R81	R80	R79
2.6v	Out	Out	In	In	In
2.05v	In	In	In	In	In
1.9v	In	In	In	Out	Out
1.8v	In	In	Out	In	Out
1.65v	In	Out	In	In	In

GT64240's multi GT selection:

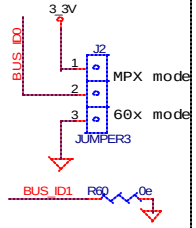


MULT_GT selection:
0 - multi GT disabled
1 - multi GT enabled

GT64240's internal arbiter selectin:

60x_InternalARB selection:
0 - internal arbiter disabled
1- internal arbiter enabled

GT64240's CPU interface bus mode:



BUS_ID[1..0] selection:
00 - 60x bus
01 - MAX bus
10 - SysADbus

JP1 - JP4

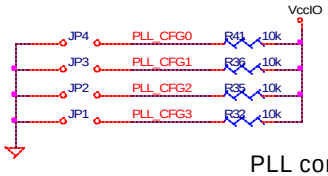
MPC7400 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 25 MHz	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 100 MHz	Bus 133 MHz	Bus 150 MHz
0100	2x	2x						200 (400)	266 (533)	300 (600)
0110	2.5x	2x					187 (375)	250 (500)	333 (666)	375 (750)
1000	3x	2x				200 (400)	225 (450)	300 (600)	400 (800)	450 (900)
1110	3.5x	2x			175 (350)	233 (466)	262 (525)	350 (700)		
1010	4x	2x			200 (400)	266 (533)	300 (600)	400 (800)		
0111	4.5x	2x			225 (450)	300 (600)	337 (675)	450 (900)		
1011	5x	2x			250 (500)	333 (666)	375 (750)			
1001	5.5x	2x		183 (366)	275 (550)	366 (733)	412 (825)			
1101	6x	2x		200 (400)	300 (600)	400 (800)	450 (900)			
0101	6.5x	2x		216 (433)	325 (650)	433 (866)				
0010	7x	2x	175 (350)	233 (466)	350 (700)					
0001	7.5x	2x	187 (375)	250 (500)	375 (750)					
1100	8x	2x	200 (400)	266 (533)	400 (800)					
0000	9x	2x	225 (450)	300 (600)	450 (900)					
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied							
1111	PLL off		PLL off, no core clocking occurs							

JP1 - JP4

XPC750P Microprocessor PLL Configuration

PLL_CFG [0-3]	Sample Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz
1000	9x	2x						250 (500)	300 (600)
1110	8.5x	2x					262 (525)	292 (584)	350 (700)
1010	4x	2x				266 (533)	300 (600)	333 (666)	400 (800)
0111	4.5x	2x				300 (600)	330 (660)	375 (750)	
1011	5x	2x			250 (500)	333 (666)	375 (750)		
1001	5.5x	2x			275 (550)	366 (733)			
1101	6x	2x			300 (600)	400 (800)			
0101	6.5x	2x		260 (520)	325 (650)				
0010	7x	2x		280 (560)	350 (700)				



PLL configuration:

Galileo Technology			
Title: EV-MPC7400/750-S1			
Size: B	Document Number: Module config		Rev: 2.0
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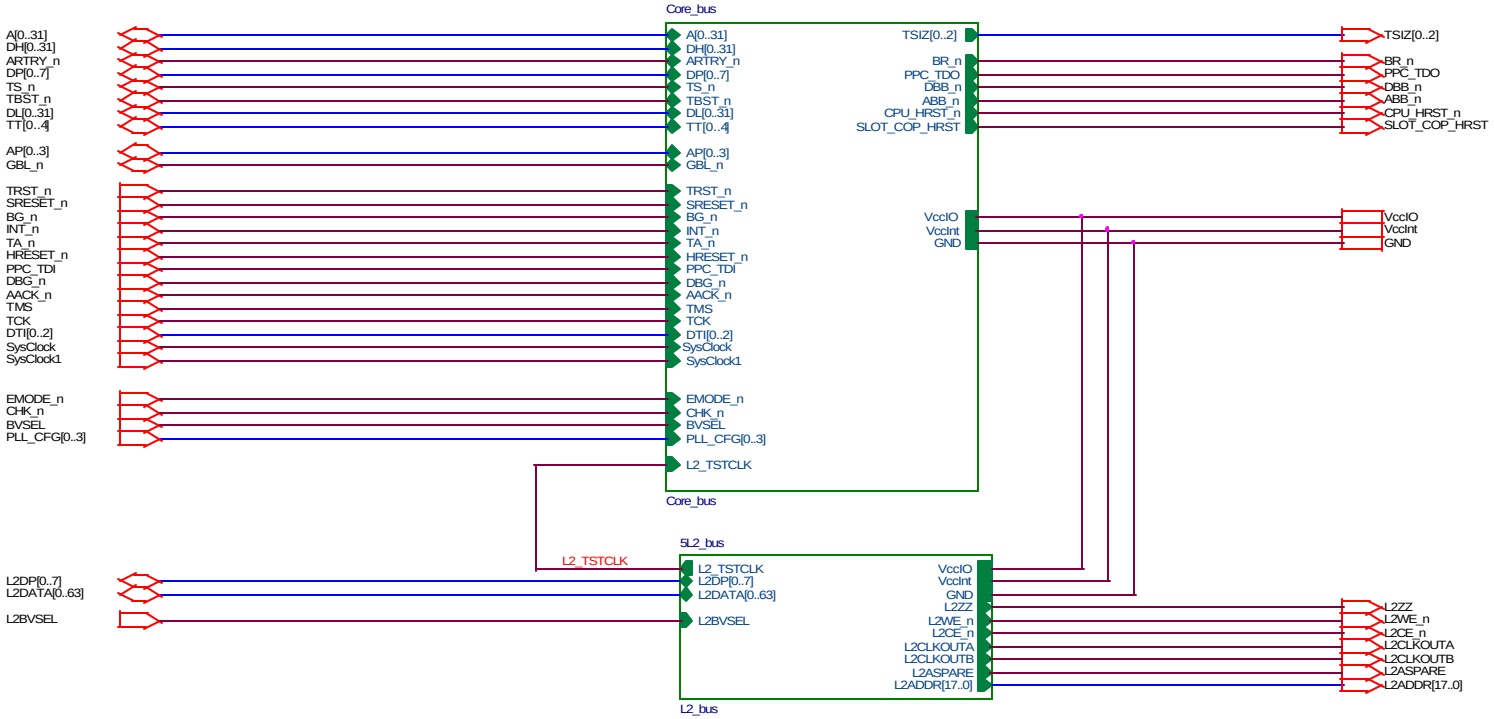

Galileo Technology		
Title: EV-MPC7400/750-S1		
Size: B	Document Number: MPC7400	Rev: 2.0
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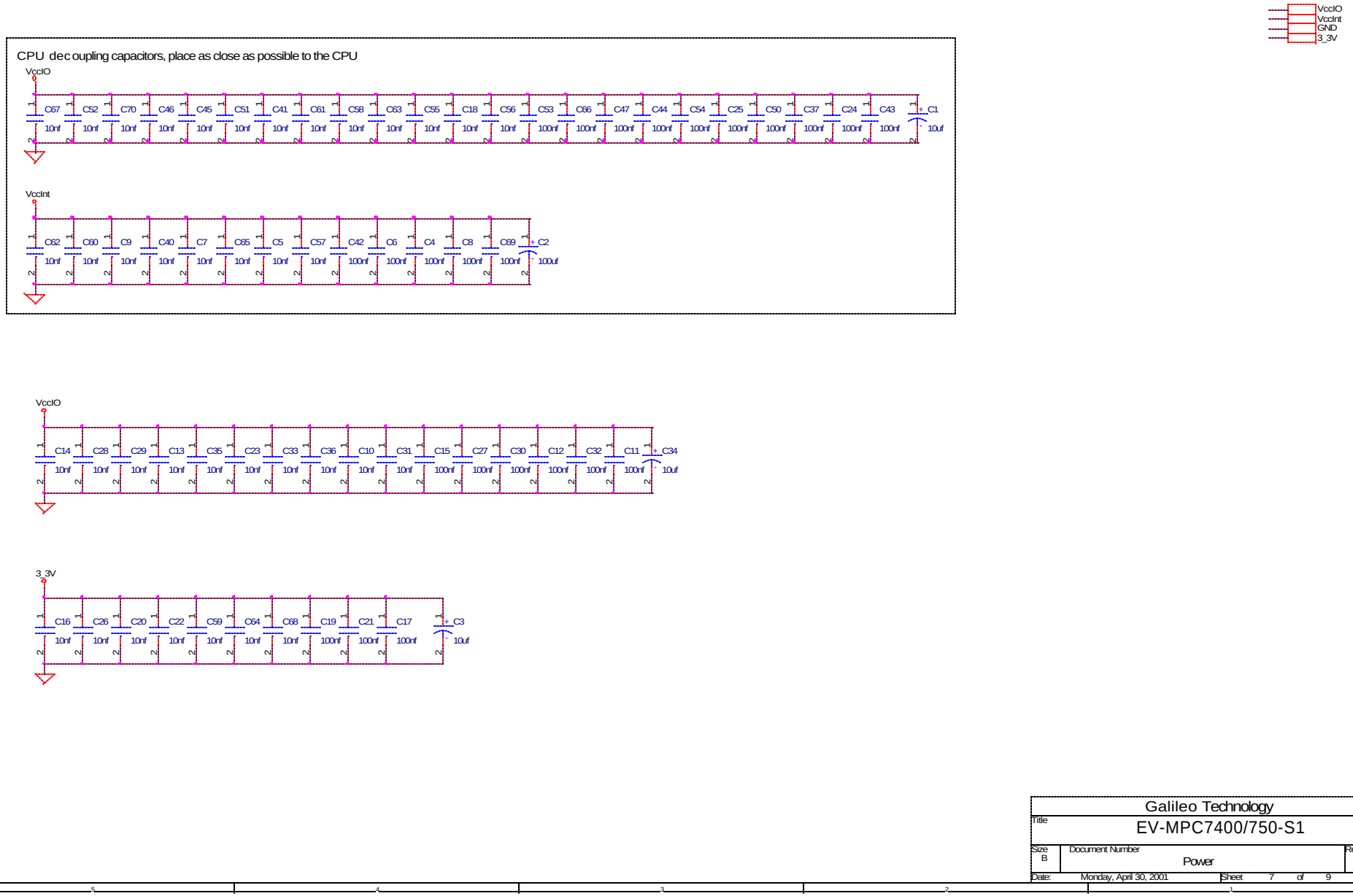

Galileo Technology		
Title: EV-MPC7400/750-S1		
Size: B	Document Number: Power	Rev: 2.0
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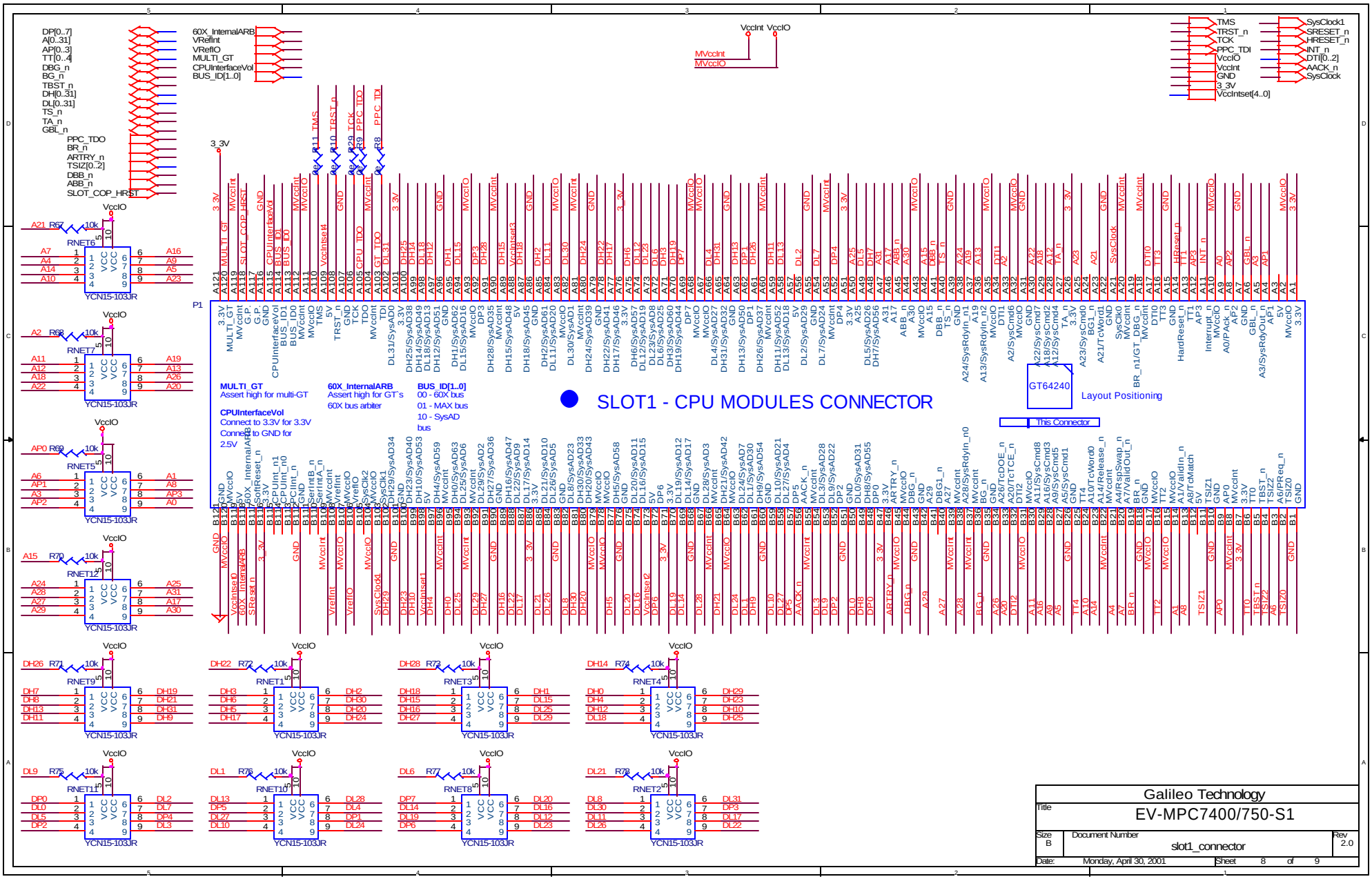
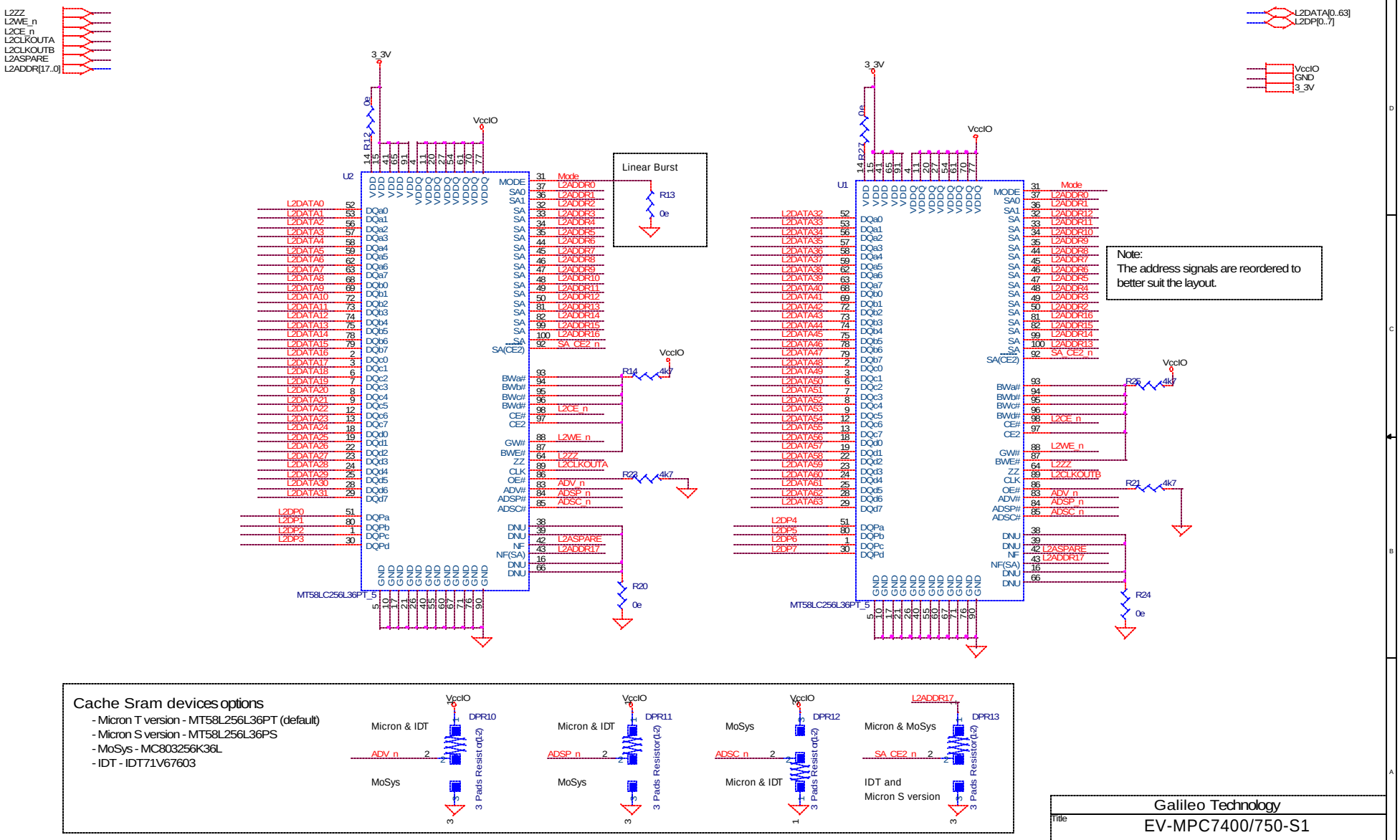

SLOT1 - CPU MODULES CONNECTOR
MULTI_GT
Assert high for multi-GT
CPUInterfaceVol
Connect to 3.3V for 3.3V
Connect to GND for 2.5V
60X_InternalARB
Assert high for GT`s
60X bus arbiter
BUS_ID[1..0]
00 - 60X bus
01 - MAX bus
10 - SysAD bus
GT64240
Layout Positioning
This Connector
Galileo Technology
EV-MPC7400/750-S1
slot1_connector
Monday, April 30, 2001
Rev 2.0


L2ZZ
L2WE_n
L2CE_n
L2CLKOUTA
L2CLKOUTB
L2ASPARE
L2ADDR[17..0]
L2DATA[0..63]
L2DP[0..7]
VccIO
GND
3_3V
U2
U1
MT58LC256L36PT_5
Linear Burst
R13
0e
R14
4k7
R22
R20
R12
R27
R25
R21
R24
Note:
The address signals are reordered to better suit the layout.
Cache Sram devices options
- Micron T version - MT58L256L36PT (default)
- Micron S version - MT58L256L36PS
- MoSys - MC803256K36L
- IDT - IDT71V67603
Micron & IDT
MoSys
Micron & MoSys
IDT and
Micron S version
DPR10
DPR11
DPR12
DPR13
3 Pads Resistor(1-2)
ADV_n
ADSP_n
ADSC_n
SA_CE2_n
Galileo Technology
Title
EV-MPC7400/750-S1
Size
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Document Number
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