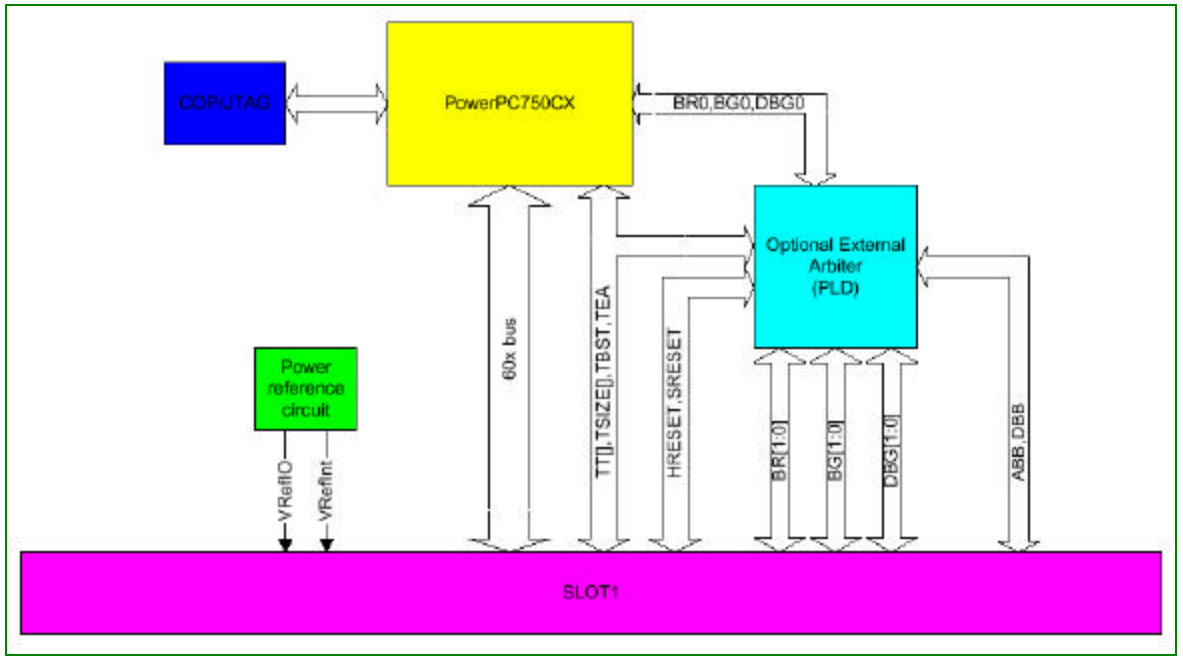
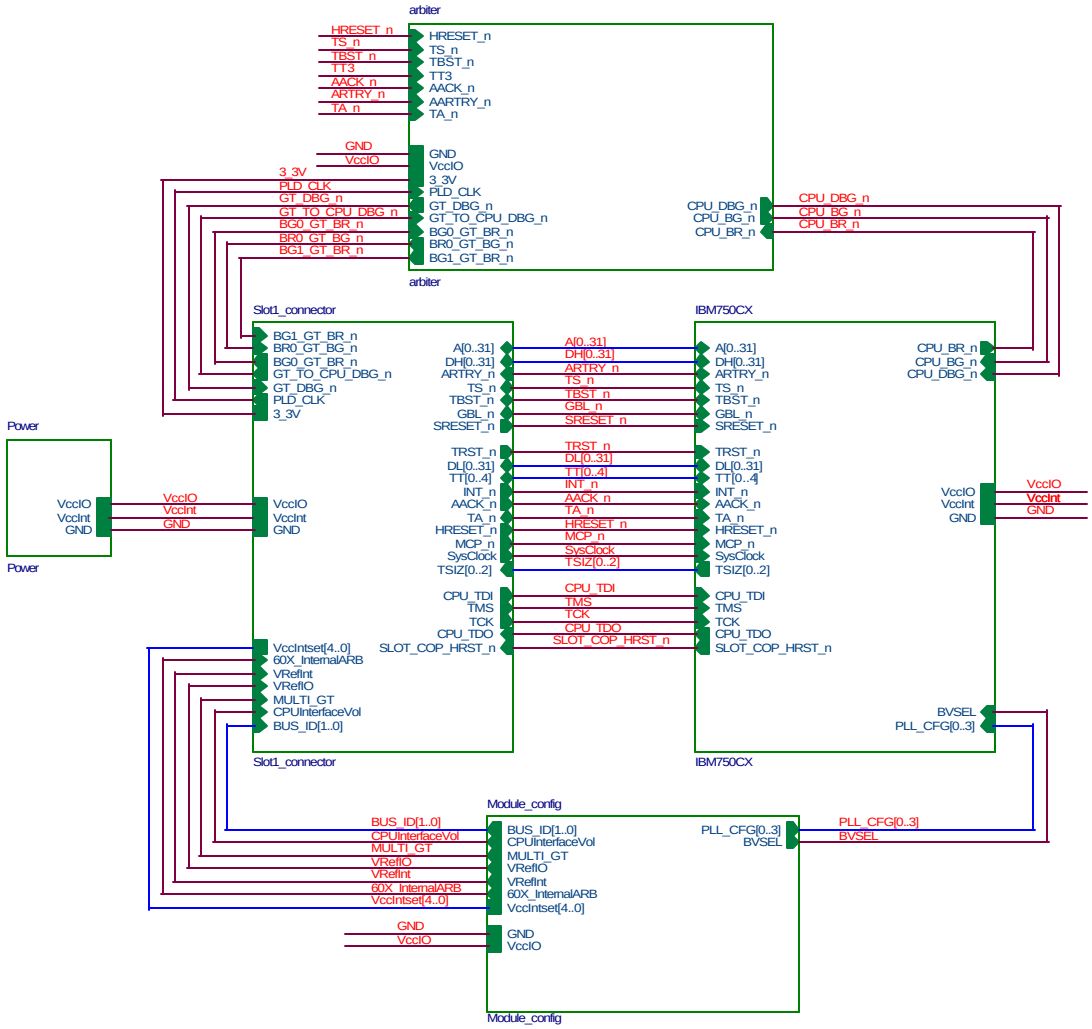
main

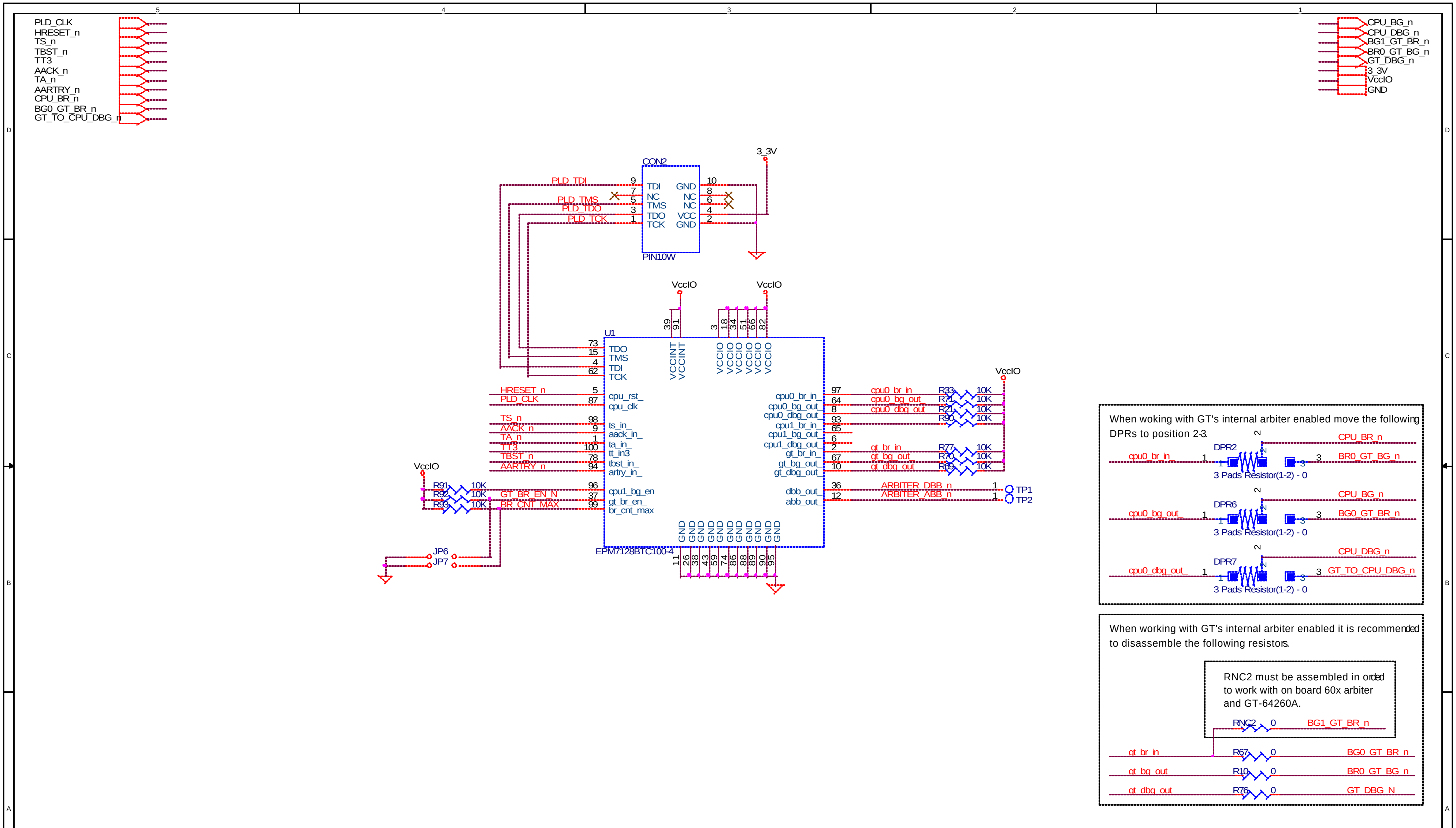


Sheet Number:	Content:
1	Info page
2	Module - Top hierarchy.
3	PLD - 60x bus optional external arbiter
4	IBM PPC750CX
5	Module configurations
6	Decoupeling capacitors.
7	SLOT1 connector
Rev Number 0.9	Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.91	After rename. Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 2.0	change list: 1. New PLD device. 2. mechanical space for heat sink. Preliminary release. Please make sure you have latest revision when referencing this schematic.

Galileo Technology		
Title: EV-IBM750CX-S1		
Size: B	Document Number: block_diagram	Rev: 2.0
Date: Monday, May 21, 2001	Sheet 1 of 7	



Galileo Technology		
Title: EV-IBM750CX-S1		
Size: B	Document Number: Main	Rev: 2.0
Date: Monday, May 21, 2001	Sheet 2 of 7	

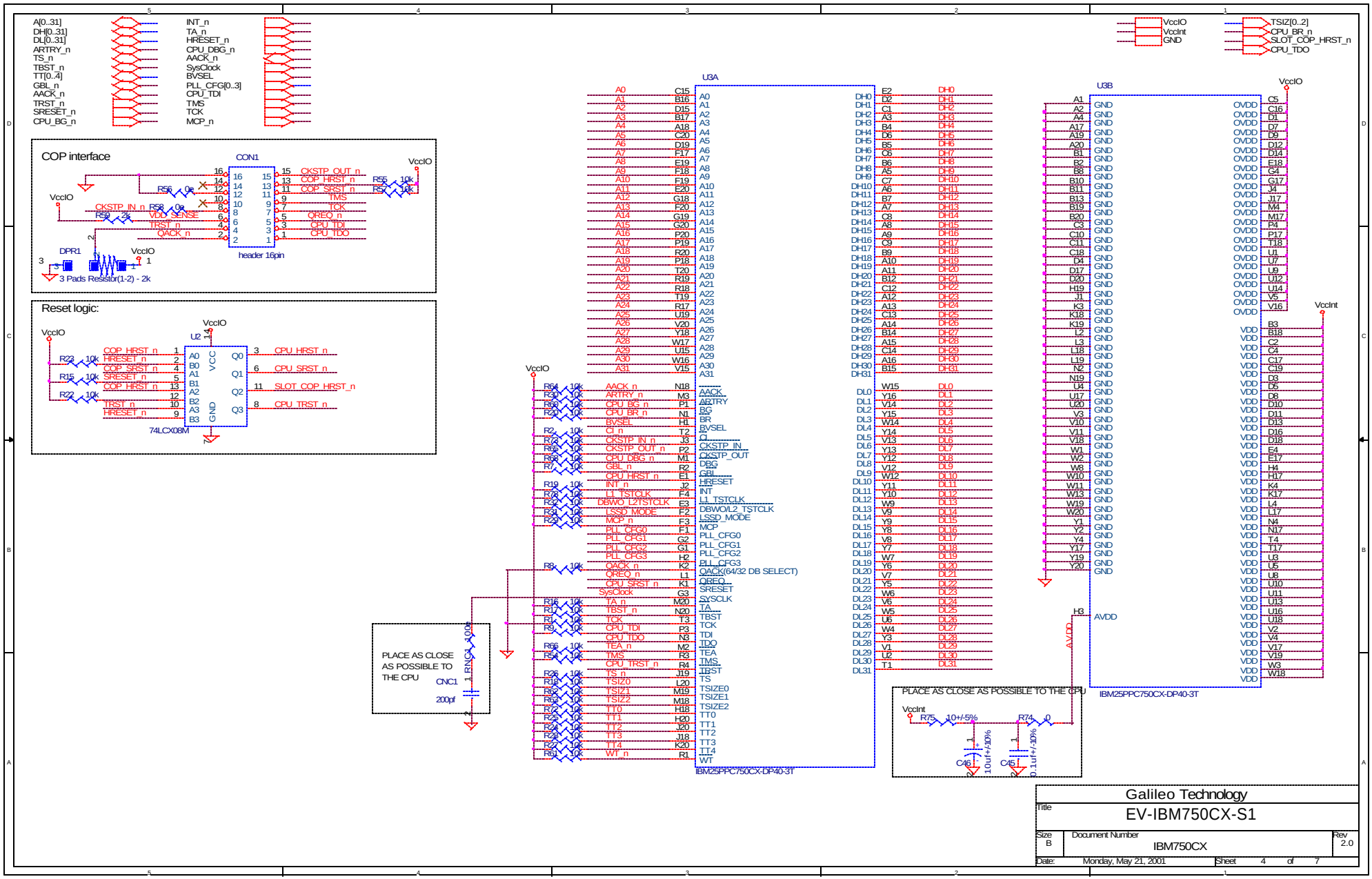


Galileo Technology

Title: EV-IBM750CX-S1

Size	Document Number	Rev
B	Arbiter	2.0

Date: Wednesday, May 23, 2001 Sheet 3 of 7

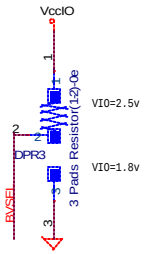

A[0..31]
DH[0..31]
DL[0..31]
ARTRY_n
TS_n
TBST_n
TT[0..4]
GBL_n
AACK_n
TRST_n
SRESET_n
CPU_BG_n
INT_n
TA_n
HRESET_n
CPU_DBG_n
AACK_n
SysClock
BVSEL
PLL_CFG[0..3]
CPU_TDI
TMS
TCK
MCP_n
VccIO
VccInt
GND
TSIZ[0..2]
CPU_BR_n
SLOT_COP_HRST_n
CPU_TDO
COP interface
CON1
header 16pin
CKSTP_OUT_n
COP_HRST_n
COP_SRST_n
TMS
TCK
QREQ_n
CPU_TDI
CPU_TDO
CKSTP_IN_n
VDD_SENSE
TRST_n
QACK_n
DPR1
3 Pads Resistor(1-2) - 2k
Reset logic:
74LCX08M
U3A
IBM25PPC750CX-DP40-3T
U3B
PLACE AS CLOSE AS POSSIBLE TO THE CPU
CNC1
200pf
RNC1 100R
PLACE AS CLOSE AS POSSIBLE TO THE CPU
10+/-5%
10uf+/-10%
0.1uf+/-10%
AVDD
Galileo Technology
EV-IBM750CX-S1
IBM750CX
Monday, May 21, 2001
Sheet 4 of 7

VccIO
GND
VccIntset[4..0]

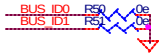
BUS_ID[1..0]
CPUInterfaceVol
VRefIO
VRefInt

PLL_CFG[0..3]
BVSEL
MULTI_GT
60X_InternalARB

Bus voltage select:

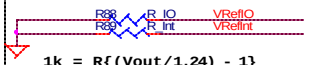


GT64240's CPU interface bus mode:



BUS_ID[1..0] selection:
00 - 60x bus
01 - MAX bus
10 - SysADbus

Power supply voltage selection:



1k = R{(Vout/1.24) - 1}

```
VccIO = 1.8v => R_IO=2.2k
VccIO = 2.5v => R_IO=1k
VccIO = 3.3v => R_IO=0.6k

VccInt = 1.8v => R_Int=2.2k
VccInt = 2.5v => R_Int=1k
VccInt = 3.3v => R_Int=0.6k
```

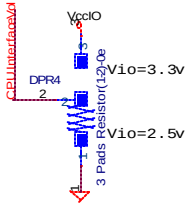
PowerPC 750CX Microprocessor PLL Configuration

PLL_CFG [0:3]		Processor to Bus Frequency Ratio (n)	Frequency Range Supported by VCO having an example range of VCO_{min} = 800 to VCO_{max} = 1200MHz[6]			
			SYSCLK		Core	
bin	dec		Min	Max	Min	Max
0000	0	2.5x	120	133[5]	300	333
0001	1	7.5x	40	80	300	600[6]
0010	2	7x	43	86		
0011	3	PLL Bypass[3]	n/a	n/a	n/a	n/a
0100	4	2x	Note 1	Note 1	Note 1	Note 1
0101	5	6.5x	46	93	300	600[6]
0110	6	10x	31[2]	60	310	600[6]
0111	7	4.5x	66	133	300	600[6]
1000	8	3x	100	133[5]		
1001	9	5.5x	55	109		
1010	10	4x	75	150		
1011	11	8x	40	120		
1100	12	8x	37	75		
1101	13	8x	50	100		
1110	14	3.5x	86	172		
1111	15	Off[4]	n/a	n/a	Off	Off

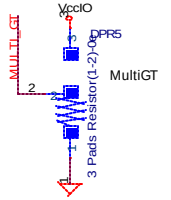
Note:

1. The 2X Processor to Bus Ratio is currently not supported..
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see section "Clock AC Specifications" on page 13 for valid SYSCLK and VCO frequencies
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In Clock - off mode, no clocking occurs inside the PowerPC 750CX regardless of the SYSCLK input.
5. The SYSCLK limit is 133 MHz, as specified in Table 6 on page 15. Applications requiring SYSCLK over 133 MHz will be investigated by application conditions.
6. VCO_{max} is specified in this table by the maximum core processor speed. The VCO maximum of 1200 MHz reflects a processor core speed of 600 MHz, which is not currently supported.

GT64240's CPU interface voltage selection:

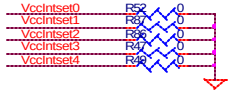


GT64240's multi GT selection:



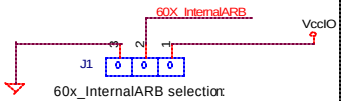
MULT_GT selection:
0 - multi GT disabled
1 - multi GT enabled

CPU power selction - configuration depends on CPU internal voltage

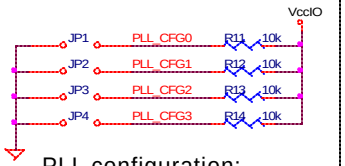


VccInt	R49	R47	R86	R87	R52
2.6v	Out	Out	In	In	In
2.05v	In	In	In	In	In
1.9v	In	In	In	Out	Out
1.8v	In	In	Out	In	Out
1.65v	In	Out	In	In	In

GT64240's internal arbiter selection:



60x_InternalARB selection:
0 - internal arbiter disabled
1- internal arbiter enabled



PLL configuration:

Galileo Technology			
Title: EV-IBM750CX-S1			
Size: B	Document Number: Module Configuration		Rev: 2.0
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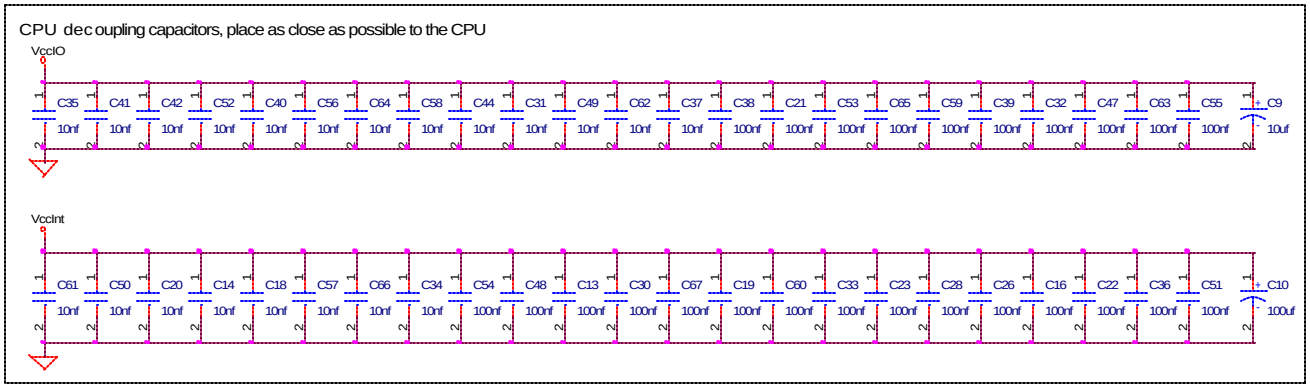
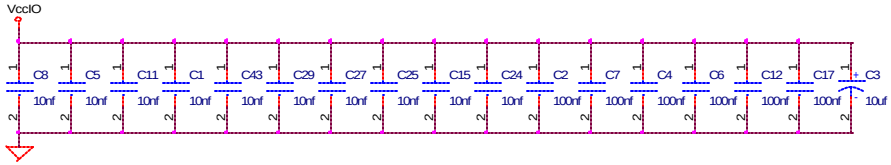
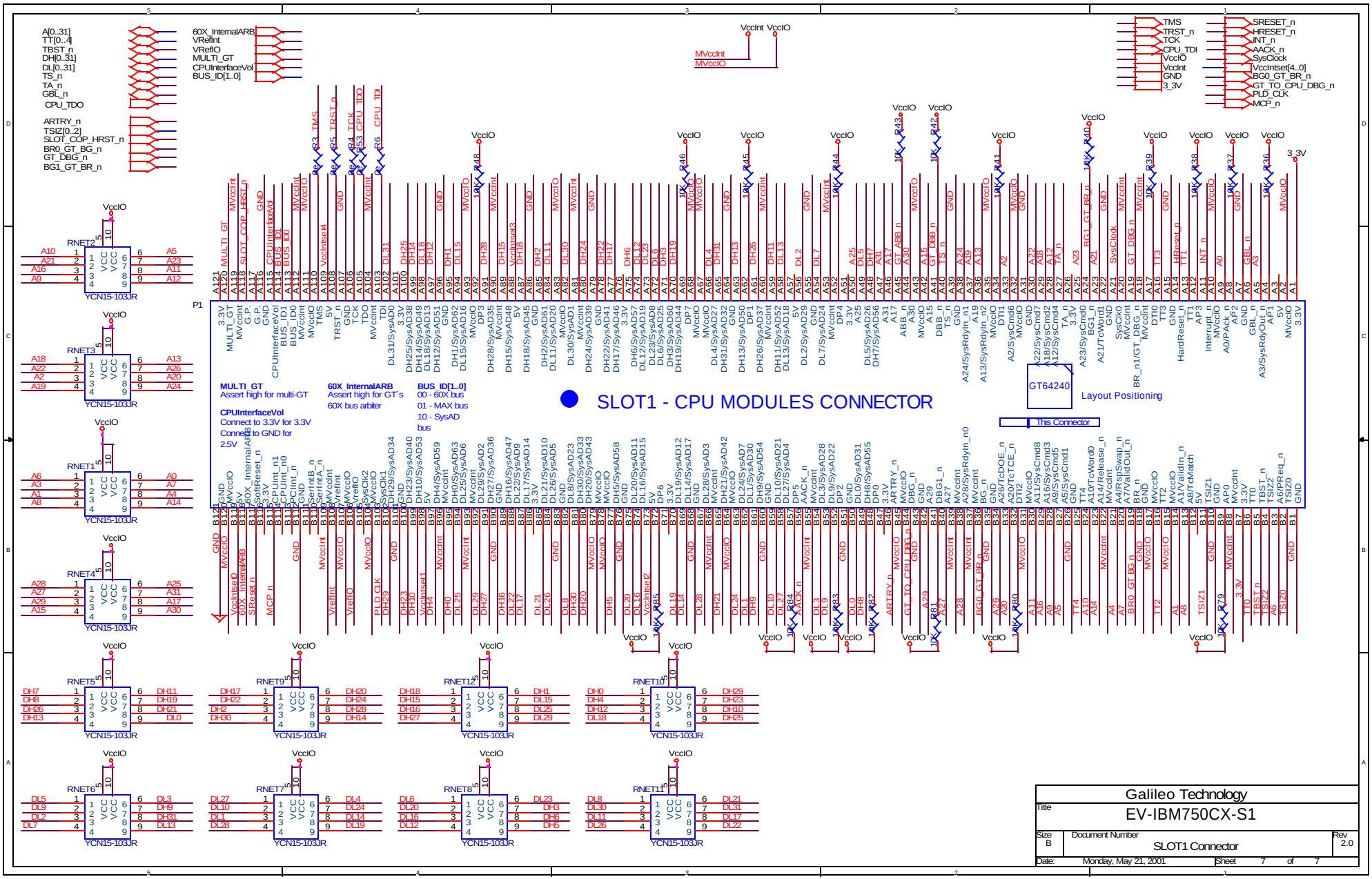




Galileo Technology		
Title: EV-IBM750CX-S1		
Size: B	Document Number: Power	Rev: 2.0
Date: Monday, May 21, 2001	Sheet 6 of 7	


SLOT1 - CPU MODULES CONNECTOR
P1
MULTI_GT
Assert high for multi-GT
CPUInterfaceVol
Connect to 3.3V for 3.3V
Connect to GND for 2.5V
60X_InternalARB
Assert high for GT`s
60X bus arbiter
BUS_ID[1..0]
00 - 60X bus
01 - MAX bus
10 - SysAD bus
GT64240
Layout Positioning
This Connector
Galileo Technology
EV-IBM750CX-S1
SLOT1 Connector
Monday, May 21, 2001
Sheet 7 of 7