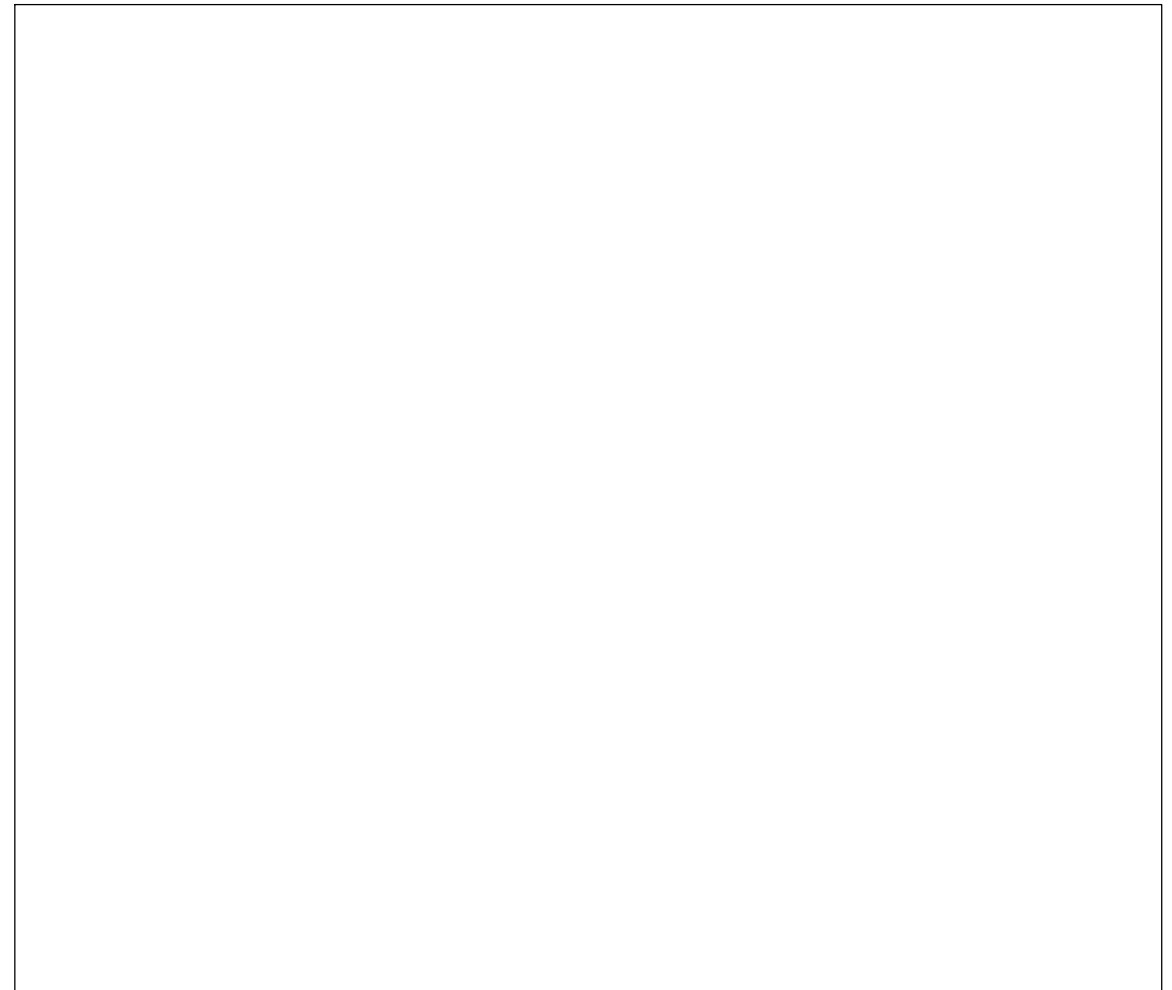
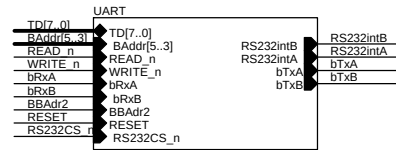


BLOCK DIAGRAM

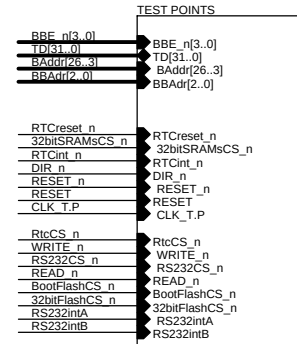
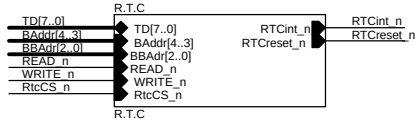
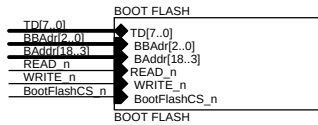
Sheet Number:	Content:
1	Info page
2	Top hierarchy.
3	144 SO DIMM male connector.
4	BOOT FLASH.
5	BUFFERS + TRANSCEIVERS.
6	FLASH MEMORY & J1 for flash write protect configuration.
7	R.T.C -Real Time Clock.
8	SRAM MEMORY.
9	SERIAL: ST16C2552 , voltage converter (ADM3202) ,serial connector.
10	TEST POINTS .
Rev Number 0.9	Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.91	The strata flash memory address bus should be connected differently in x8 and x16 modes, in rev 0.9 it was connected for x8 mode, it should be connected in x16 mode.
Rev Number 0.92	1) The board name changed from EV-SO DIMM144 to EV-DEVICES- D144. 2) Fix the table in page 8.
Rev Number 0.93	1) New setup configuration for the SRAM - Add three pad resistors to: adsp*, adsc* and adv* signals.
Rev Number 1.0	1) Production release. 2) The GT's write device parameters refer to Wr_n[3..0].Therefore, the write signals on the devices are connected to Wr_n [3..0]. We connected the Write_n signal, in the device module, which is DevRW_n. (This is better defined as an output enable signal). To correct it, we created a different equation in the PAL.The new equation for the Write_n signal is as follows: IF(!SRAM_CS_n) THEN Write_n=LDevRW_n # CStiming_n; ELSE Write_n=GP_IN[0] (Wr_n0); END IF; GP_IN[0] is abbreviated on the board as follows: Wr_n0 (BE_n0 on the EV-DEVICES-D144). 3) Fix name of U6,U4 to 74LVT162245 and U9,U10 to 28F640J3A.



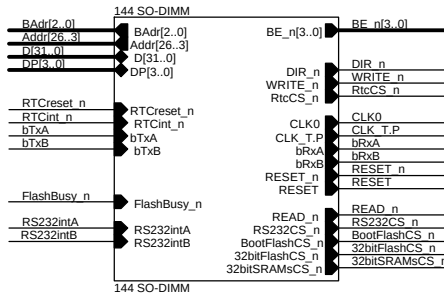
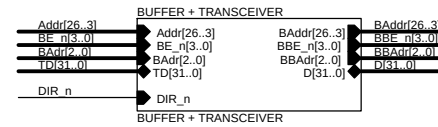
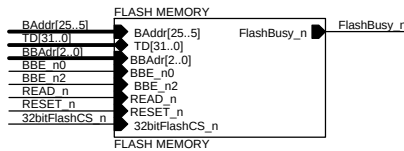
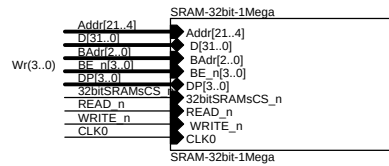
GALILEO TECHNOLOGY			
EV-DEVICES-D144			
Title			
Size B	Document Number	Info	Rev 1.0
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UART

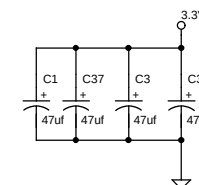
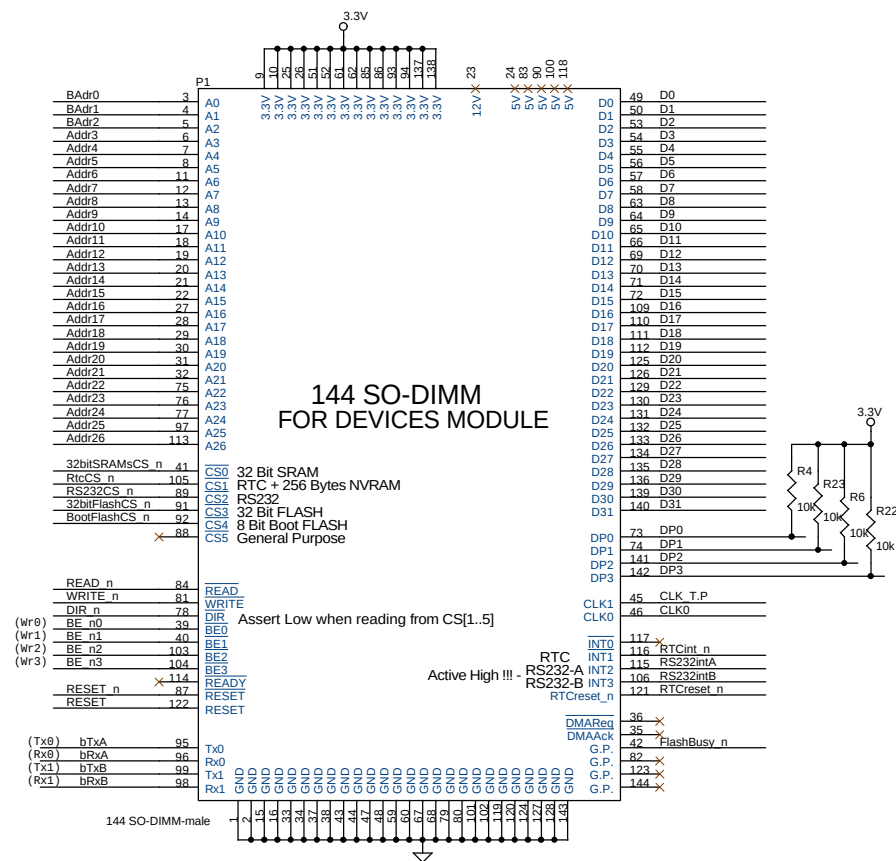


TEST POINTS



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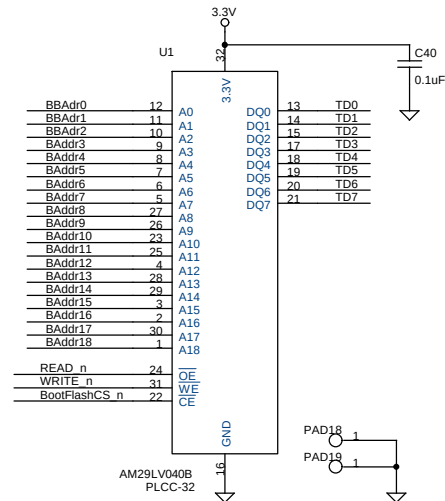
32bitSRAMsCS_n
RtcCS_n
RS232CS_n
32bitFlashCS_n
BootFlashCS_n
DIR_n
CLK_T_P
bRxA
bRxB
RESET_n
DIR_n
READ_n
WRITE_n



TD[7..0]

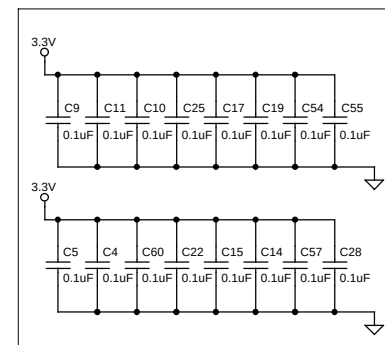
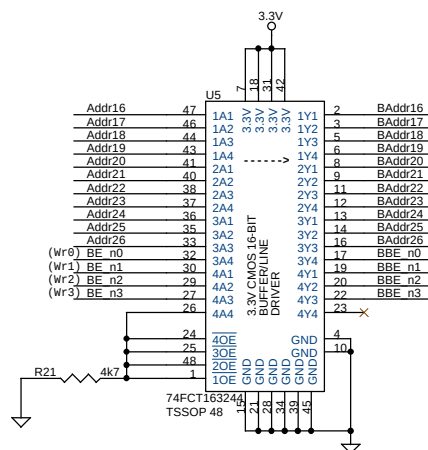
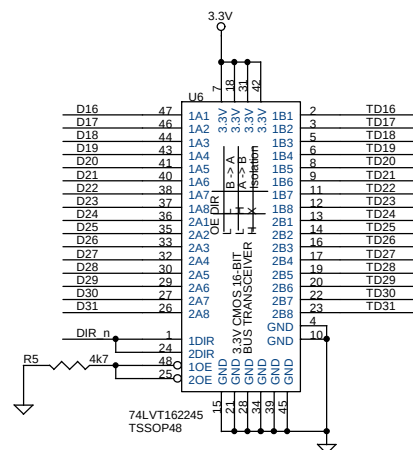
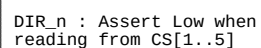


BBAAddr[2..0]
BBAAddr[18..3]
BootFlashCS_n
READ_n
WRITE_n



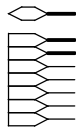
ST's M29W040 can also be used

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TD[31..0]

BAddr[25..5]
BBAddr[2..0]
32bitFlashCS_n
READ_n
RESET_n
BBE_n0
BBE_n2

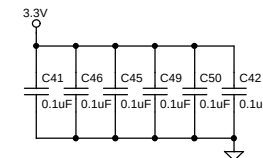
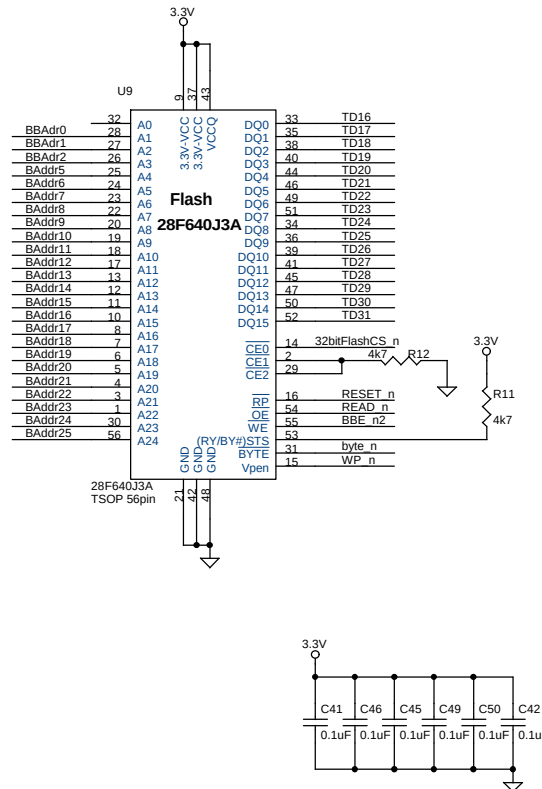
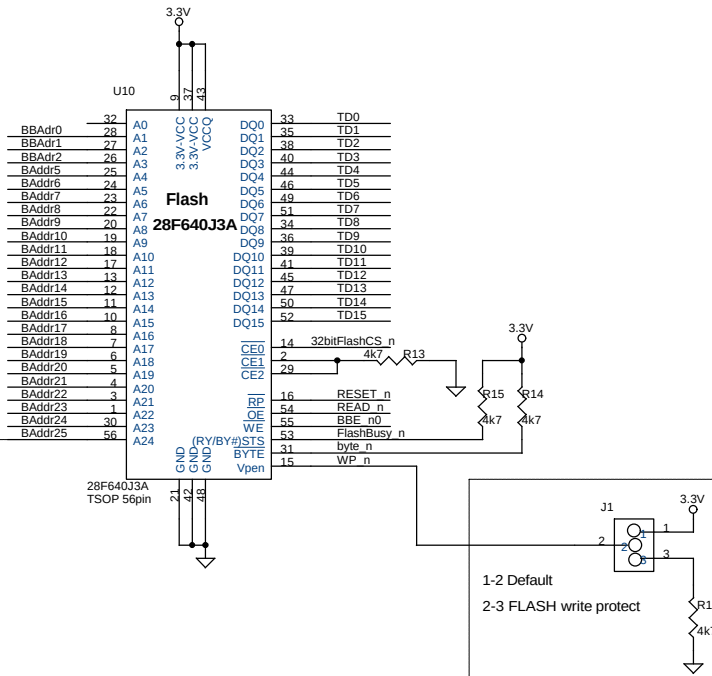


INTEL'S STRATA FLASH

FLASH SIZE OPTIONS:

28F320J3A 8Mbyte
28F640J3A 16Mbyte
28F128J3A 32Mbyte

For future 256-Mbit device



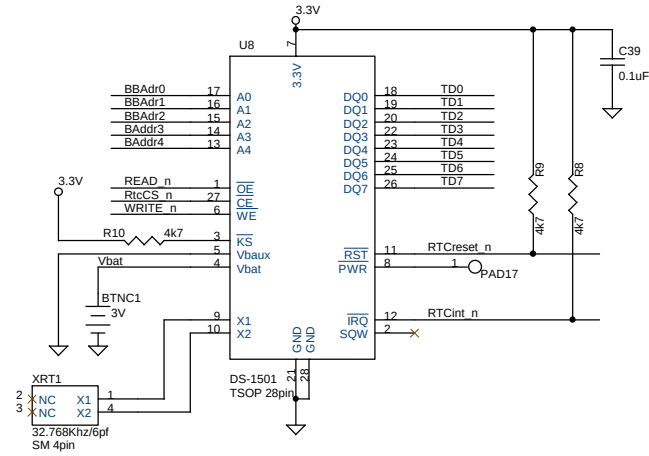
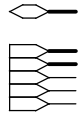
FlashBusy_n

GALILEO TECHNOLOGY EV-DEVICES-D144

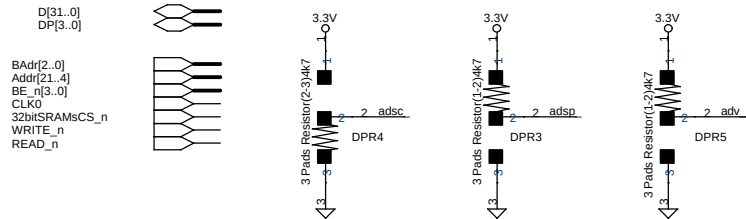
Title			
Document Number			
Size B	FLASH MEMORY		
Date:	Thursday, November 02, 2000	Sheet 6 of 10	Rev 1.0

TD[7..0]

BAddr[4..3]
BAddr[2..0]
RtcCS_n
READ_n
WRITE_n

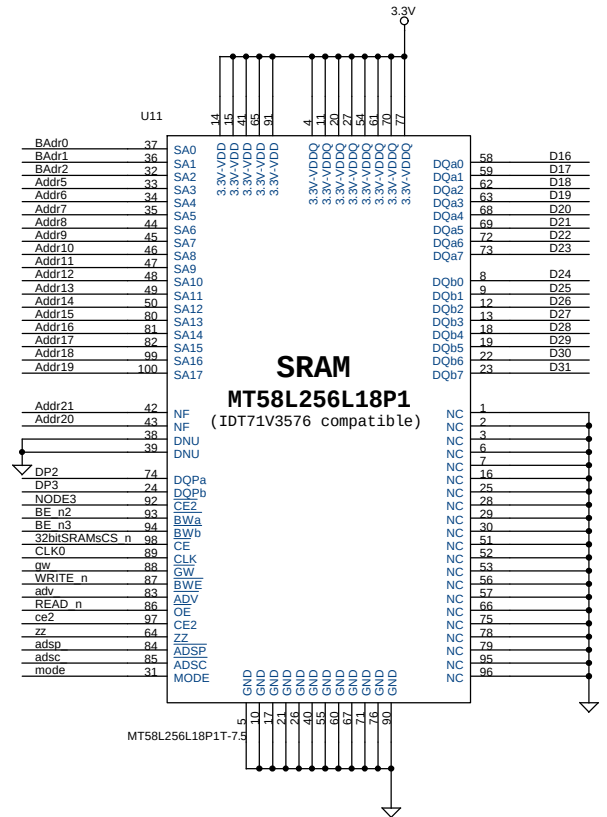
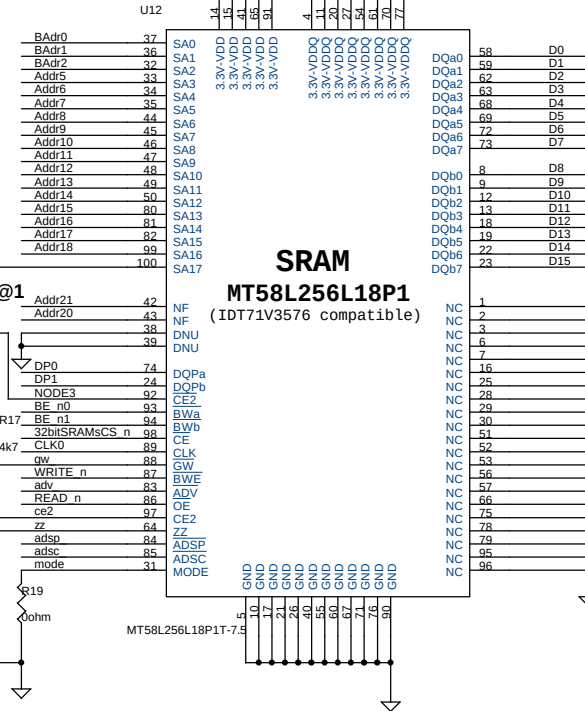
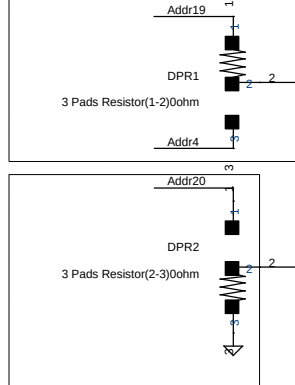


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EV-DEVICES-D144			
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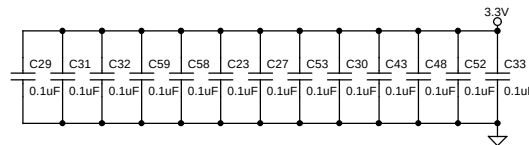
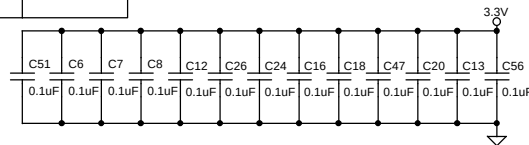
GALILEO INTERNAL USE ONLY!

(For 16bit Device testing USE ONLY
Micron's 256x18 device connect 2-3 0ohm.)



2 Mbyte			1 Mbyte	
Micron 512x18 S-version	Micron 512x18 T-version	Idt 512x18	Micron 256x18	Idt 256x18
DPR1:(1,2)0ohm DPR2:(2,3)0ohm	DPR2:(1,2)0ohm DPR1:(1,2)0ohm	DPR1:(1,2)0ohm DPR2:(2,3)0ohm	DPR1:(1,2)0ohm DPR2:(2,3)0ohm	DPR1:(1,2)0ohm DPR2:(2,3)0ohm

@1 On the s version, Pin 42 is reserved as an address upgrade pin for the 16Mb SyncBurst SRAM.

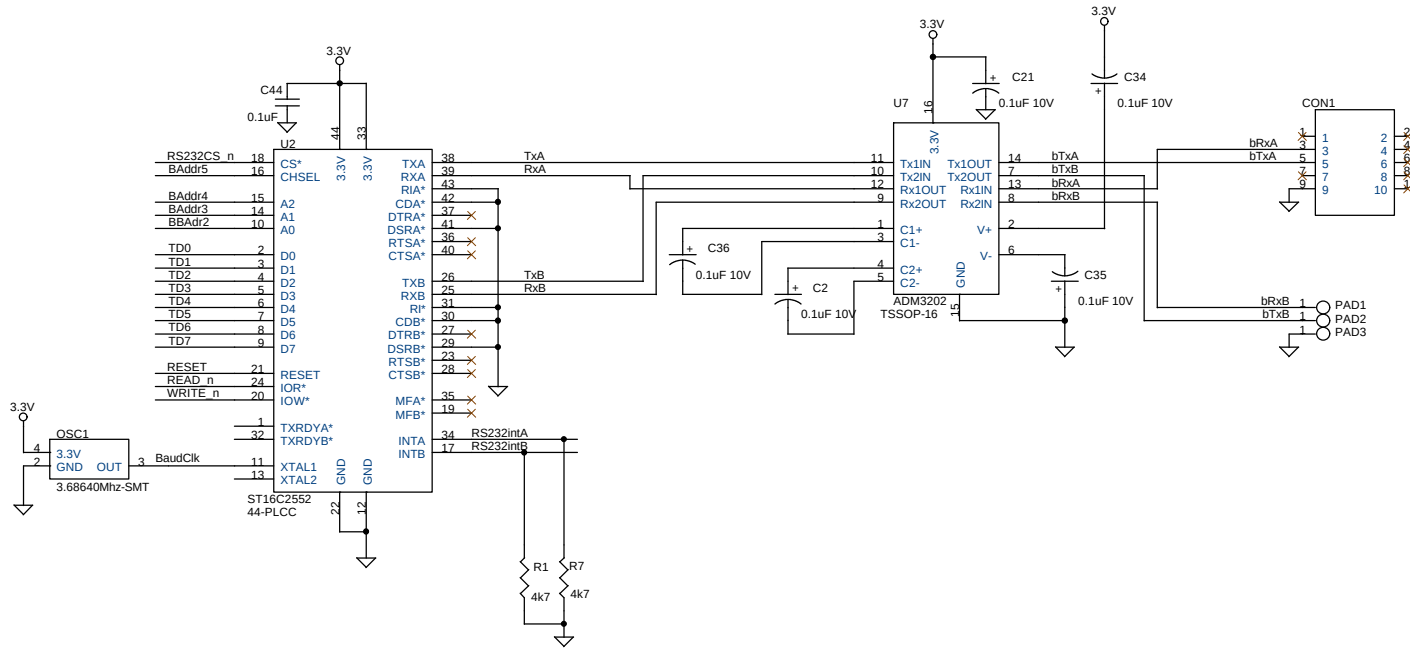


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Title	Document Number	SRAM - 32 bit - 1MEGA	
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TD[7..0]

BAddr[5..3]
BAddr2
RS232CS_n
READ_n
WRITE_n
bRxA
bRxB
RESET

bTxA
bTxB
RS232intA
RS232intB



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TD[31..0]
BBE_n[3..0]
BAddr[26..3]
BAddr[2..0]
32bitSRAMCS_n
RttCS_n
RS232CS_n
32bitFlashCS_n
BootFlashCS_n
READ_n
WRITE_n
RESET_n
RESET_n
DIR_n
RTClnt_n
RTCreset_n
RS232inA
RS232inB
CLK_T.P

