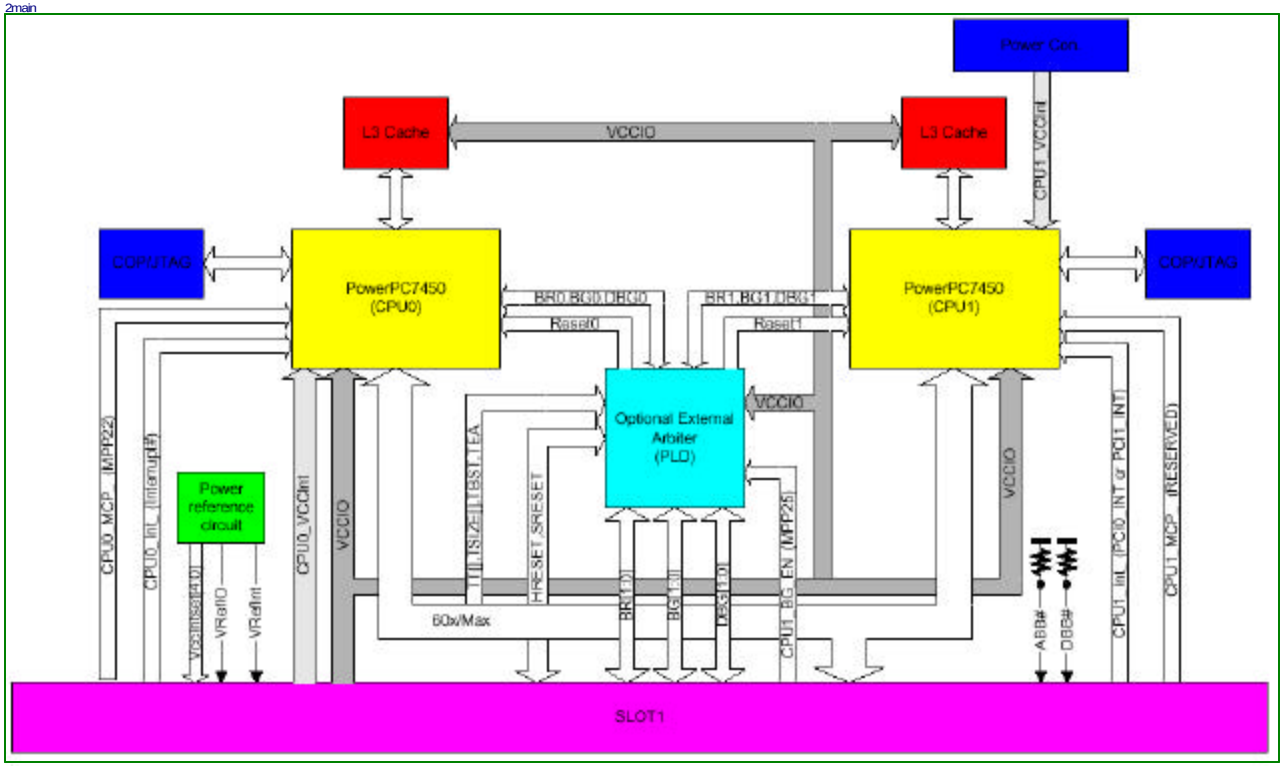
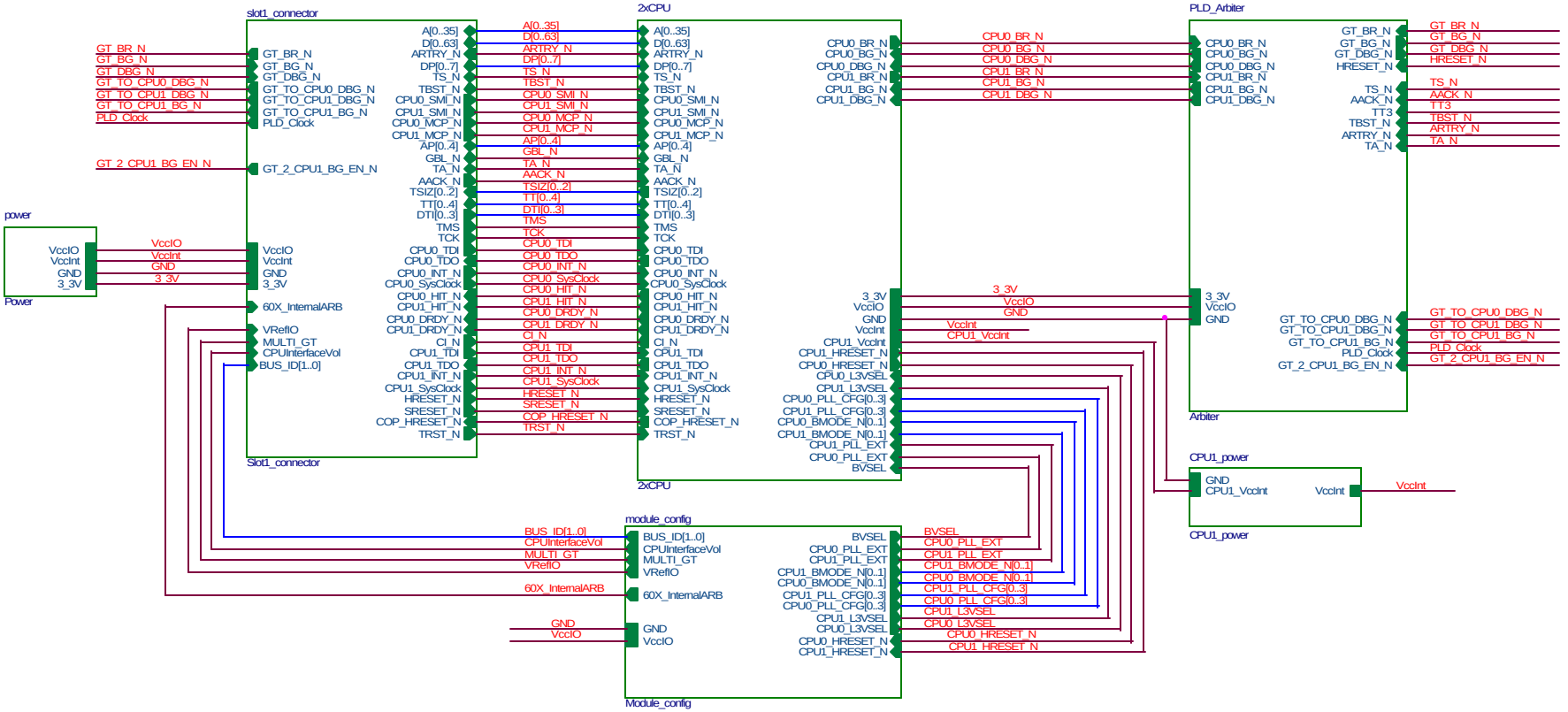
2main

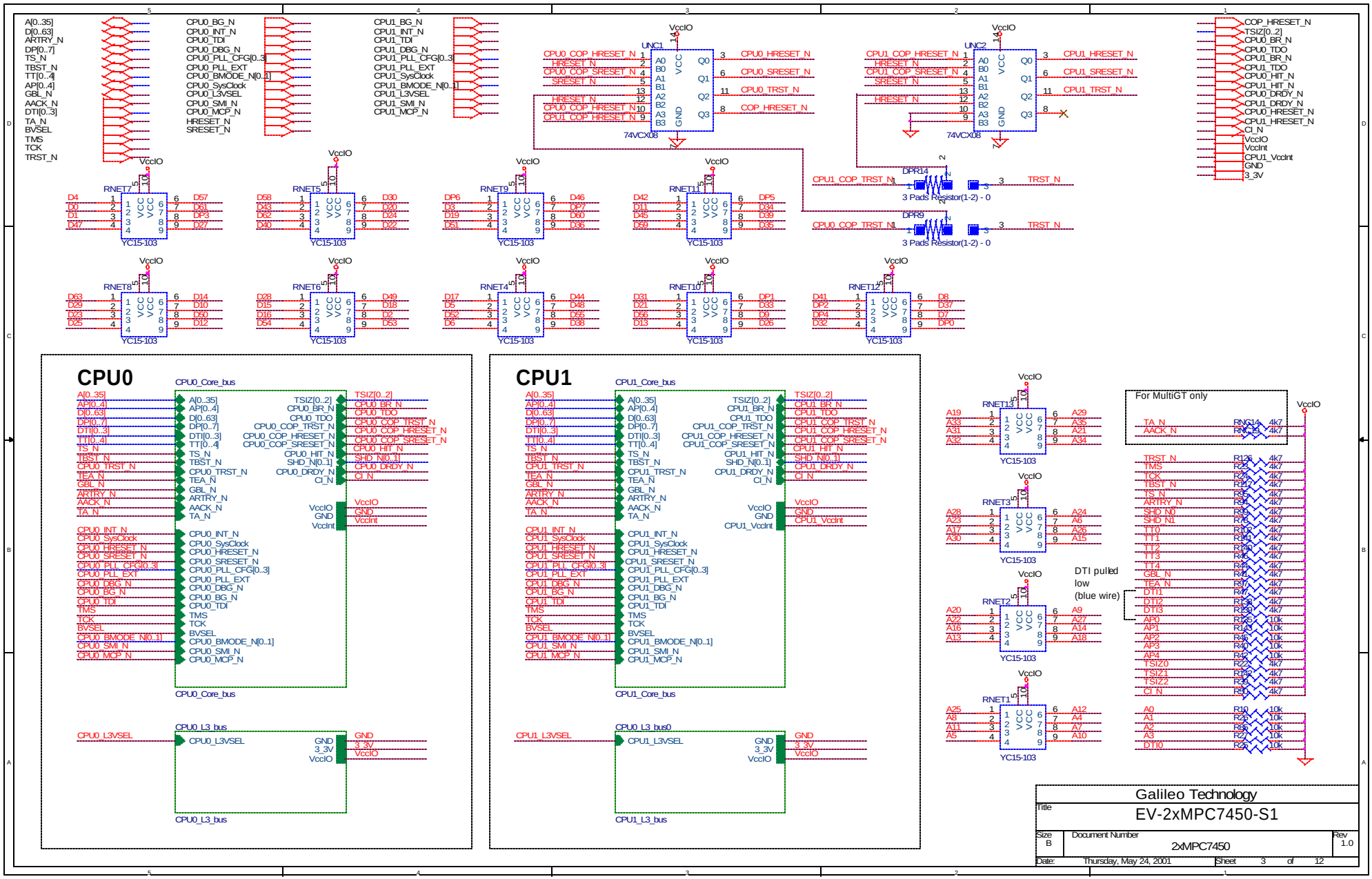


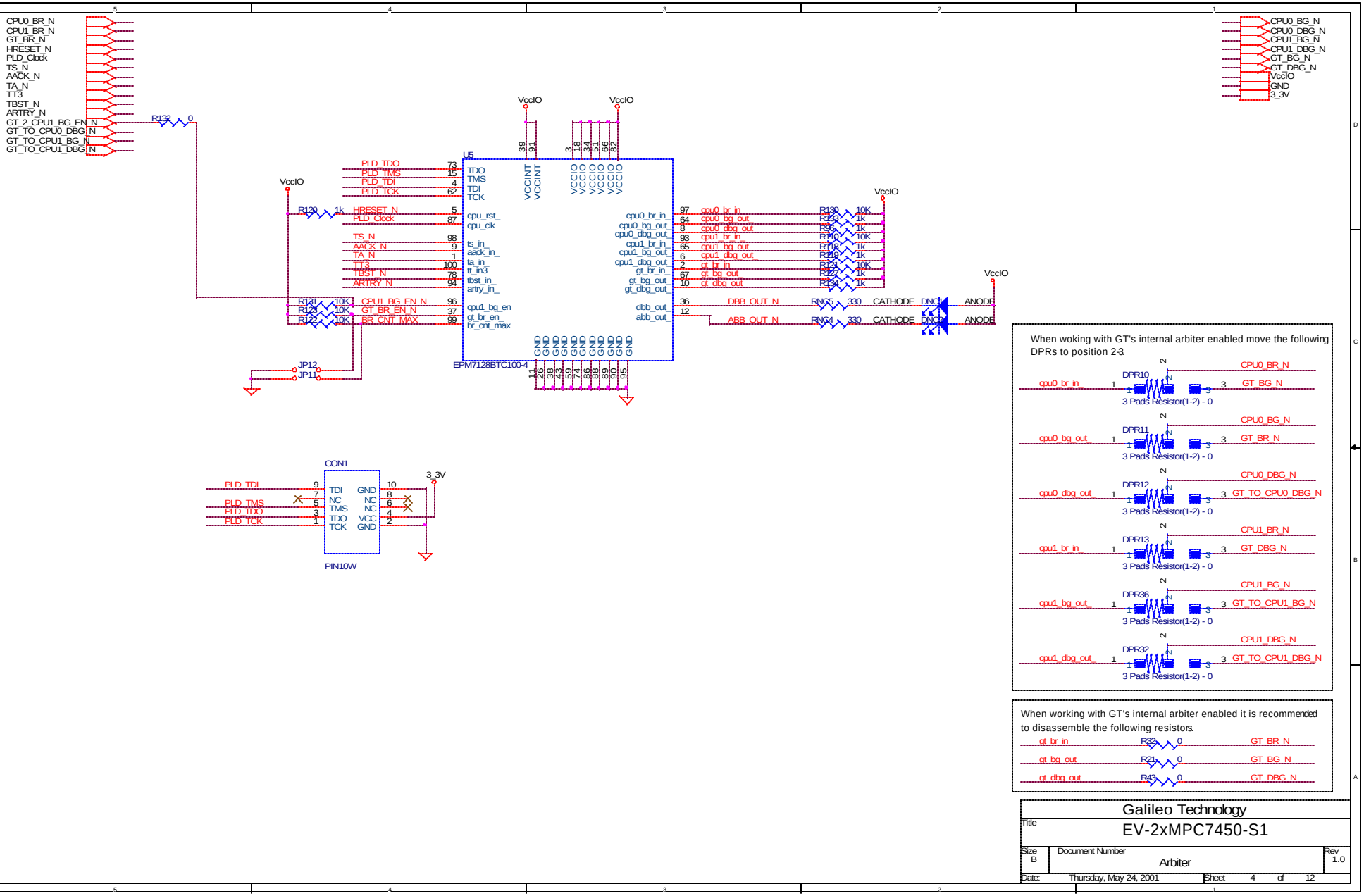
Sheet Number:	Content:
1	Info page
2	Module - Top hierarchy.
3	2xMPC7450 - Top hierarchy
4	FPGA - CPU bus arbiter
5	CPU0 - core bus
6	CPU0 - L3
7	CPU1 - core bus
8	CPU1 - L3
9	CPU1 - Power supply
10	Module configuration setting
11	Power
12	SLOT1 Connector
Rev Number 0.1	Preliminary version. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.2	Following changes from previous revision: 1. L3 cache was replaced to PBSRAM. 2. Additional decoupling capacitors. 3. No address support in the FPGA. Preliminary version. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.9	After rename. Preliminary version. Please make sure you have latest revision when referencing this schematic.
Rev Number 1.0	Follwing changes from prefious revision: 1. TDI[1..3] must be connected to pull down (blue wire). 2. CPUx_L1_TSTCLK must be pulled low (blue wire). 3. DPR27 must be connected in position 2-3. 4. DPR25 must be connected in position 2-3. Please make sure you have latest revision when referencing this schematic.

Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: block_diagram	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 1 of 12	



Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: Main	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 2 of 12	


A[0..35]
D[0..63]
ARTRY_N
DP[0..7]
TS_N
TBST_N
TT[0..4]
AP[0..4]
GBL_N
AACK_N
DTI[0..3]
TA_N
BVSEL
TMS
TCK
TRST_N
CPU0_BG_N
CPU0_INT_N
CPU0_TDI
CPU0_DBG_N
CPU0_PLL_CFG[0..3]
CPU0_PLL_EXT
CPU0_BMODE_N[0..1]
CPU0_SysClock
CPU0_L3VSEL
CPU0_SMI_N
CPU0_MCP_N
HRESET_N
SRESET_N
CPU1_BG_N
CPU1_INT_N
CPU1_TDI
CPU1_DBG_N
CPU1_PLL_CFG[0..3]
CPU1_PLL_EXT
CPU1_SysClock
CPU1_BMODE_N[0..1]
CPU1_L3VSEL
CPU1_SMI_N
CPU1_MCP_N
VccIO
UNC1
74VCX08
CPU0_COP_HRESET_N
HRESET_N
CPU0_COP_SRESET_N
SRESET_N
CPU0_COP_TRST_N
CPU0_HRESET_N
CPU0_SRESET_N
CPU0_TRST_N
UNC2
CPU1_COP_HRESET_N
CPU1_COP_SRESET_N
CPU1_COP_TRST_N
CPU1_HRESET_N
CPU1_SRESET_N
CPU1_TRST_N
COP_HRESET_N
TSIZ[0..2]
CPU0_BR_N
CPU0_TDO
CPU1_BR_N
CPU1_TDO
CPU0_HIT_N
CPU1_HIT_N
CPU0_DRDY_N
CPU1_DRDY_N
CPU0_HRESET_N
CPU1_HRESET_N
CI_N
VccInt
CPU1_VccInt
GND
3_3V
DPR14
DPR9
3 Pads Resistor(1-2) - 0
RNET7
RNET5
RNET9
RNET11
RNET8
RNET6
RNET4
RNET10
RNET12
YC15-103
CPU0
CPU0_Core_bus
CPU0_L3_bus
CPU1
CPU1_Core_bus
CPU1_L3_bus
CPU1_L3_bus0
RNET13
RNET3
RNET2
RNET1
For MultiGT only
RNG14
RNG15
DTI pulled low (blue wire)
R126
R125
R124
R123
R122
R121
R120
R119
R118
R117
R116
R115
R114
R113
R112
R111
R110
R109
R108
R107
R106
4k7
10k
Galileo Technology
EV-2xMPC7450-S1
2xMPC7450
Thursday, May 24, 2001
Sheet 3 of 12
Size B
Rev 1.0

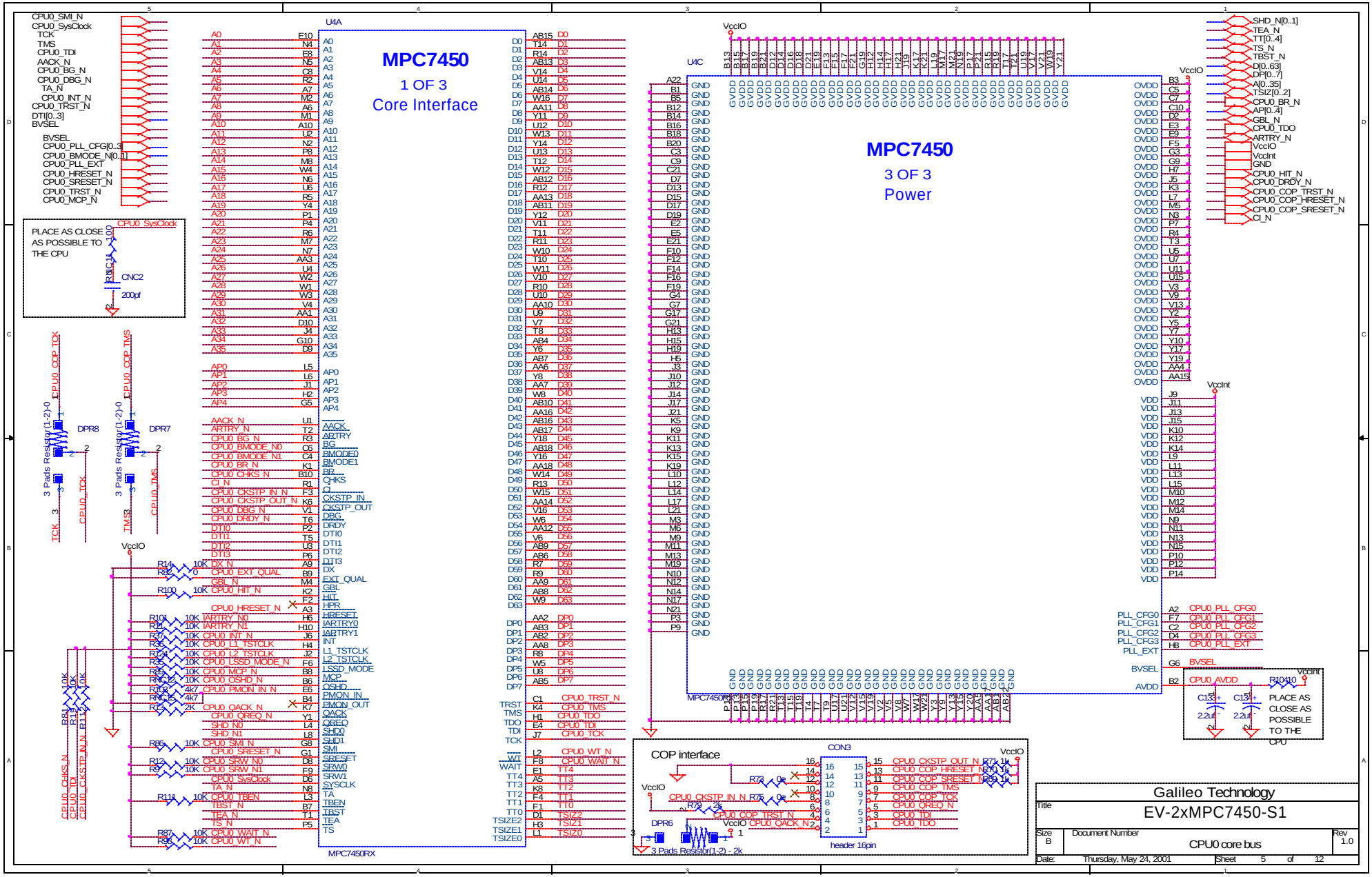


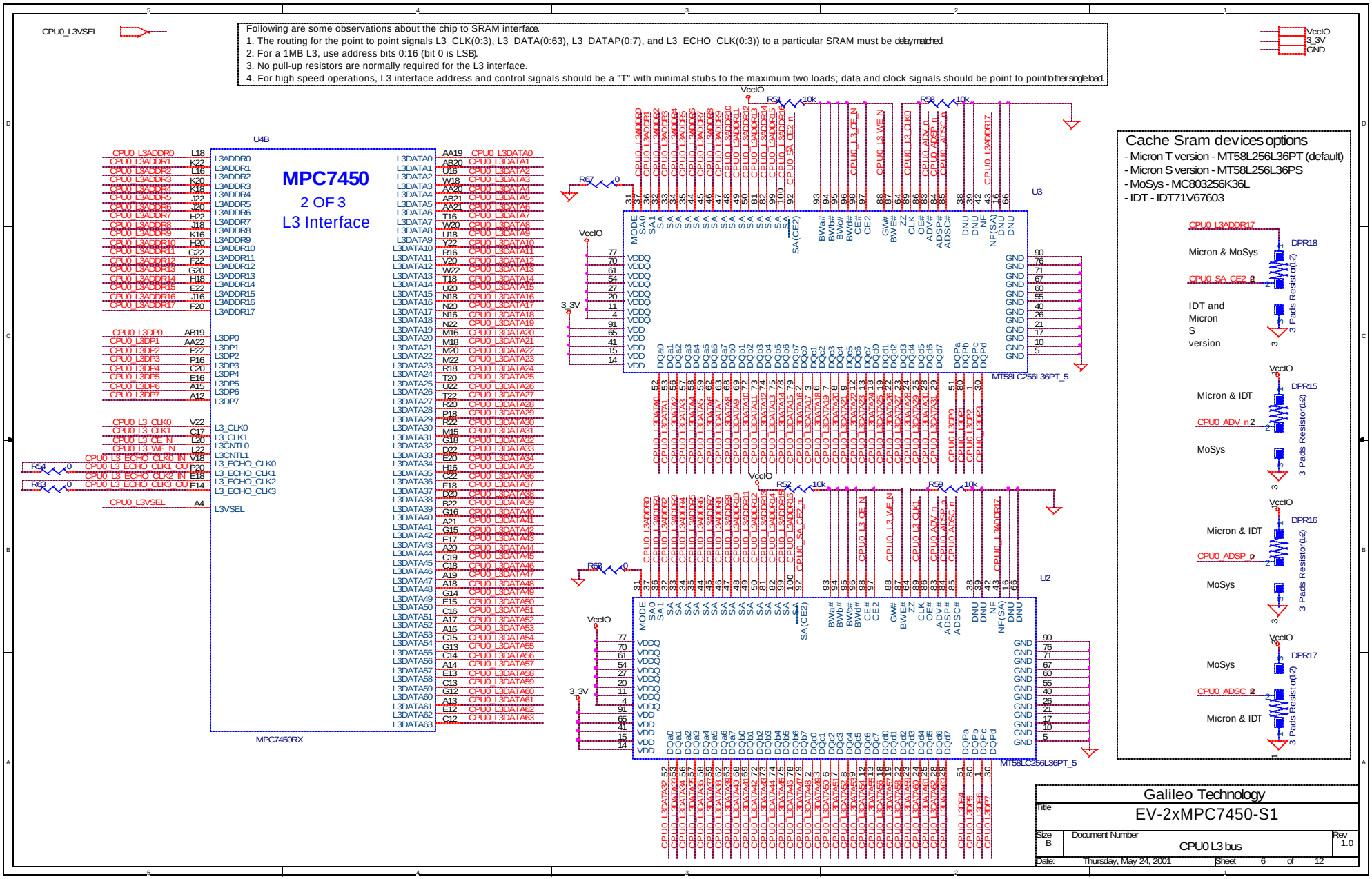
Galileo Technology

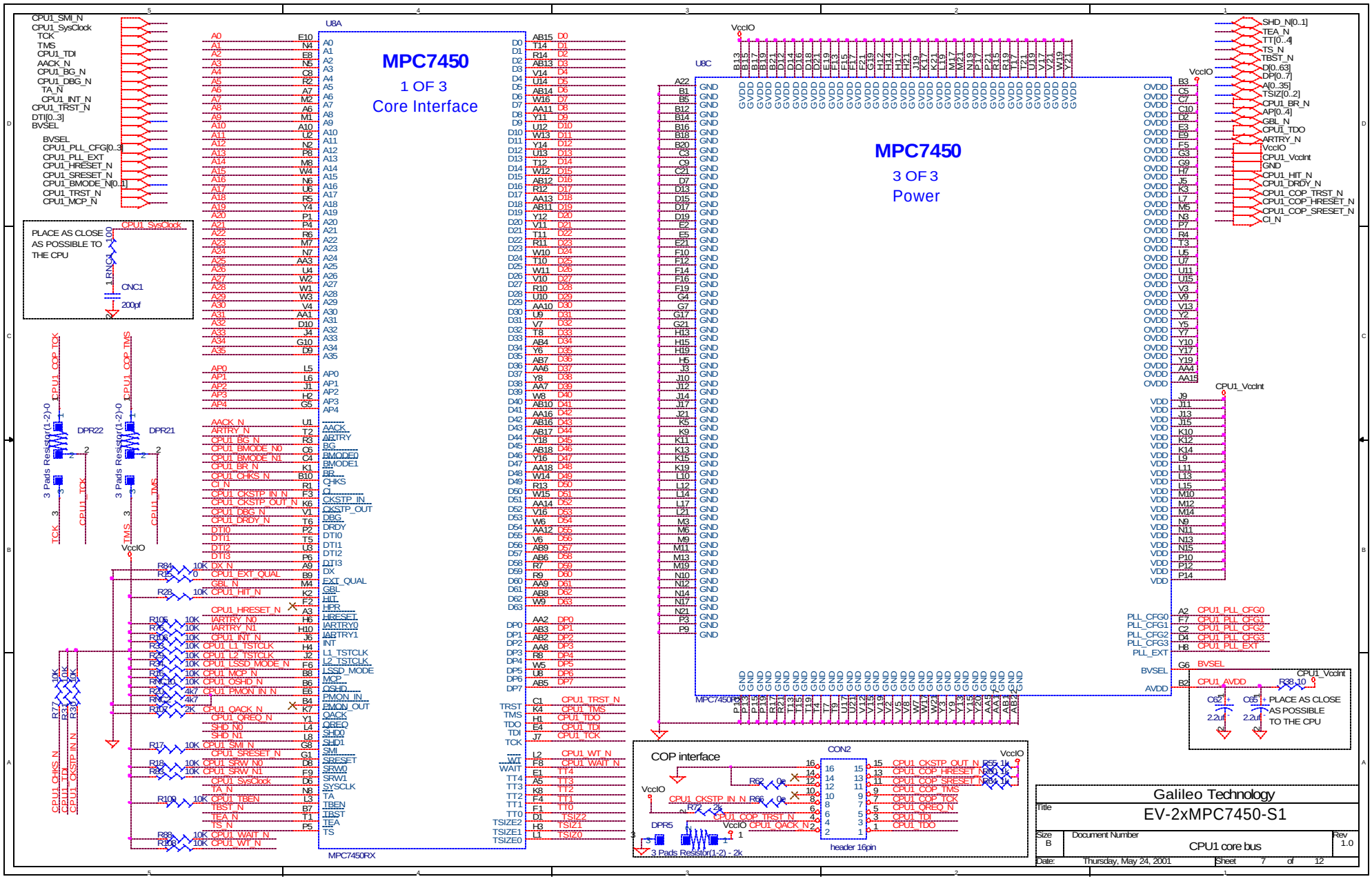
Title: EV-2xMPC7450-S1

Size	Document Number	Rev
B	Arbiter	1.0

Date: Thursday, May 24, 2001 Sheet 4 of 12


MPC7450
1 OF 3
Core Interface
MPC7450
3 OF 3
Power
COP interface
CON3
header 16pin
Galileo Technology
EV-2xMPC7450-S1
CPU0 core bus
Thursday, May 24, 2001


CPU0_L3VSEL
Following are some observations about the chip to SRAM interface.
1. The routing for the point to point signals L3_CLK(0:3), L3_DATA(0:63), L3_DATAP(0:7), and L3_ECHO_CLK(0:3)) to a particular SRAM must be delay matched.
2. For a 1MB L3, use address bits 0:16 (bit 0 is LSB).
3. No pull-up resistors are normally required for the L3 interface.
4. For high speed operations, L3 interface address and control signals should be a "T" with minimal stubs to the maximum two loads; data and clock signals should be point to point to their single load.
VccIO
3_3V
GND
U4B
MPC7450
2 OF 3
L3 Interface
MPC7450RX
U3
U2
MT58LC256L36PT_5
R51
R52
R58
R59
R67
R68
R64
R63
Cache Sram devices options
- Micron T version - MT58L256L36PT (default)
- Micron S version - MT58L256L36PS
- MoSys - MC803256K36L
- IDT - IDT71V67603
Micron & MoSys
IDT and Micron S version
Micron & IDT
MoSys
DPR18
DPR15
DPR16
DPR17
3 Pads Resistor
Galileo Technology
Title
EV-2xMPC7450-S1
Size B
Document Number
CPU0 L3 bus
Rev 1.0
Date: Thursday, May 24, 2001
Sheet 6 of 12


MPC7450
1 OF 3
Core Interface
MPC7450
3 OF 3
Power
COP interface
CON2
header 16pin
Galileo Technology
EV-2xMPC7450-S1
CPU1 core bus
Thursday, May 24, 2001

CPU1_L3VSEL

Following are some observations about the chip to SRAM interface.
1. The routing for the point to point signals L3_CLK(0:3), L3_DATA(0:63), L3_DATAP(0:7), and L3_ECHO_CLK(0:3)) to a particular SRAM must be delaymatched.
2. For a 1MB L3, use address bits 0:16 (bit 0 is LSB).
3. No pull-up resistors are normally required for the L3 interface.
4. For high speed operations, L3 interface address and control signals should be a "T" with minimal stubs to the maximum two loads; data and clock signals should be point to point to their single load.

VccIO
3_3V
GND

U8B

MPC7450
2 OF 3
L3 Interface

MPC7450RX

R1 10k R3 10k R6 0 R2 10k R4 10k R7 0 R5 0 R8 0

U7 U6

MT58LC256L36PT_5

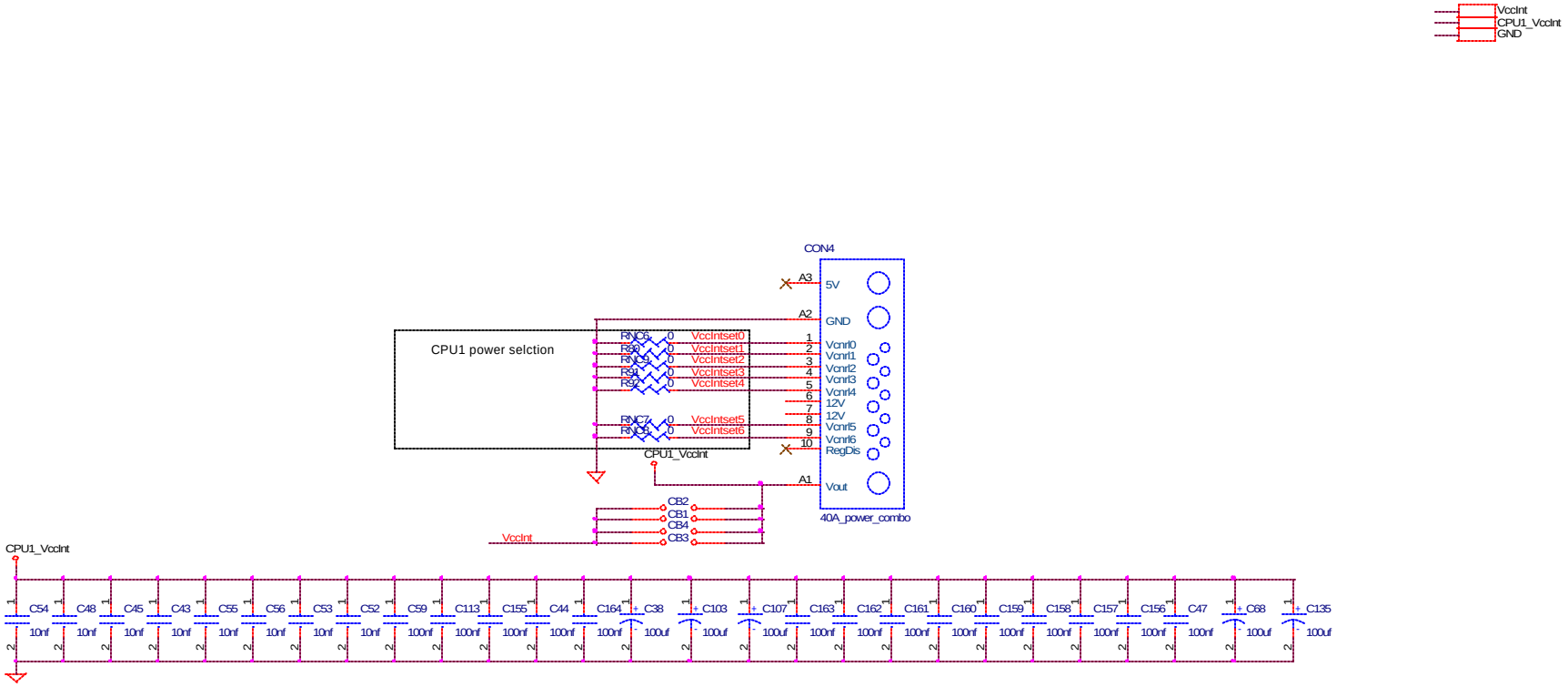
Cache Sram devices options

- Micron T version - MT58L256L36PT (default)
- Micron S version - MT58L256L36PS
- MoSys - MC803256K36L
- IDT - IDT71V67603

DPR4 DPR1 DPR2 DPR3 — 3 Pads Resistor(1/2)

Micron & MoSys
IDT and Micron S version
Micron & IDT
MoSys

Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: CPU1 L3 bus	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 8 of 12	



Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: CPU1 Power supply	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 9 of 12	

CPU0_HRESET_N
CPU1_HRESET_N

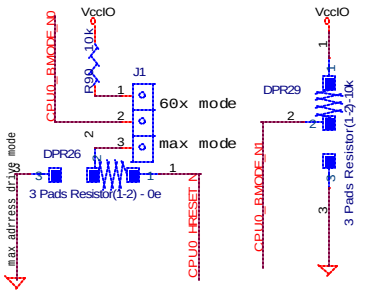
VccIO
GND
MULTI_GT

CPU0_BMODE_N[0..1]
CPU1_BMODE_N[0..1]
CPU0_L3VSEL
CPU1_L3VSEL

BUS_ID[1..0]
CPUInterfaceVol
VRefIO
60X_InternalARB

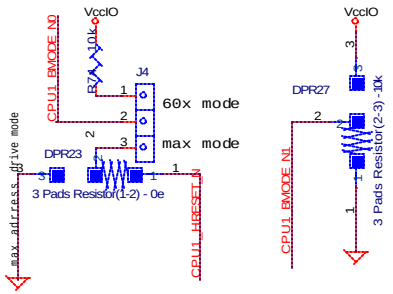
BVSEL
CPU0_PLL_CFG[0..3]
CPU1_PLL_CFG[0..3]
CPU0_PLL_EXT
CPU1_PLL_EXT

CPU0 bus mode selection:



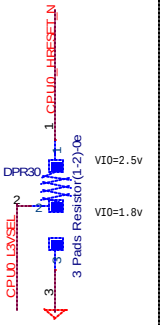
Address bus drive mode cause the V'ger to drive the address bus whenever BG is asserted independet of whether V'ger has a bus transaction to run or not.

CPU1 bus mode selection:

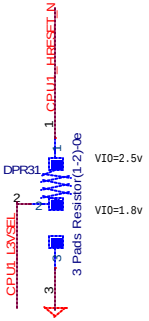


Address bus drive mode cause the V'ger to drive the address bus whenever BG is asserted independet of whether V'ger has a bus transaction to run or not.

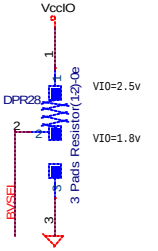
CPU0 L3 Bus voltage select:



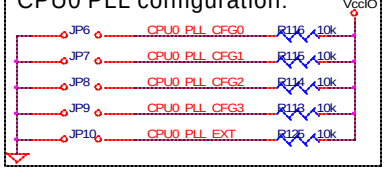
CPU1 L3 Bus voltage select:



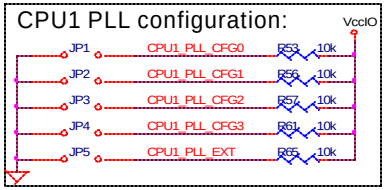
CPU Bus voltage select:



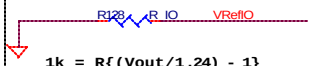
CPU0 PLL configuration:



CPU1 PLL configuration:



Power supply voltage selection:

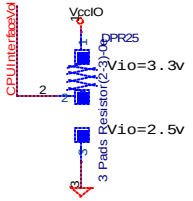


1k = R{(Vout/1.24) - 1}

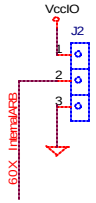
```
VccIO = 1.8v => R_IO=2.2k
VccIO = 2.5v => R_IO=1k
VccIO = 3.3v => R_IO=0.6k

VccInt = 1.8v => R_Int=2.2k
VccInt = 2.5v => R_Int=1k
VccInt = 3.3v => R_Int=0.6k
```

GT64260's CPU interface voltage selection:

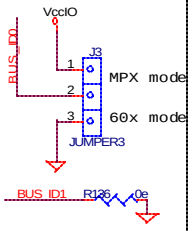


GT64260's internal arbiter selectin:



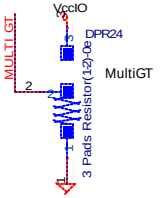
60x_InternalARB selection:
0 - internal arbiter disabled
1- internal arbiter enabled

GT64260's CPU interface bus mode:



BUS_ID[1..0] selection:
00 - 60x bus
01 - MAX bus
10 - SysADbus

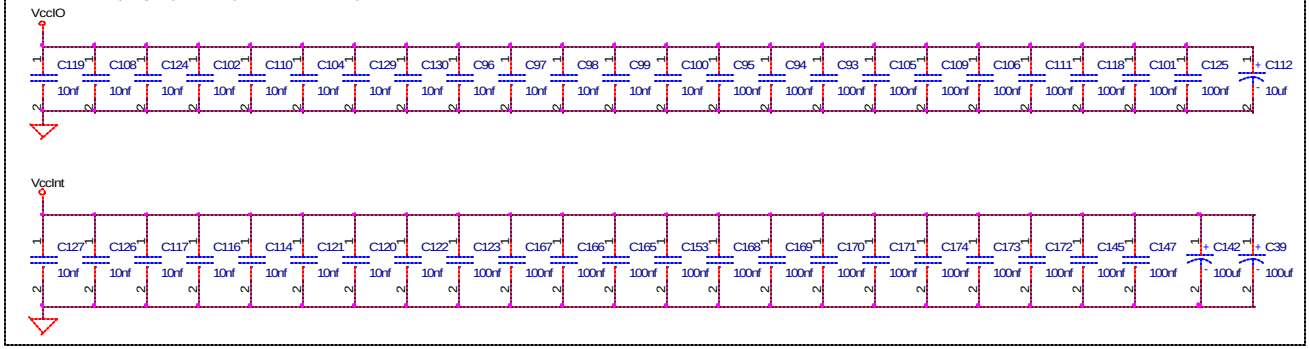
GT64260's multi GT selection:



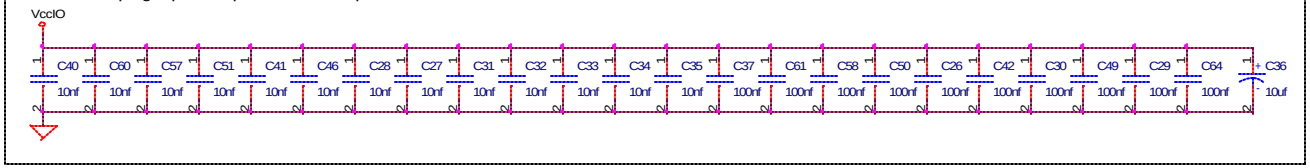
MULT_GT selection:
0 - multi GT disabled
1 - multi GT enabled

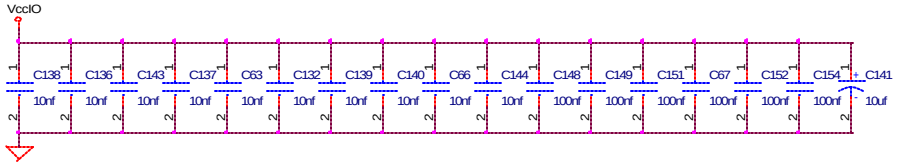
Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: Module config	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 10 of 12	

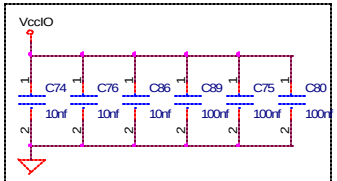
CPU0 decoupling capacitors, place as close as possible to the CPU0



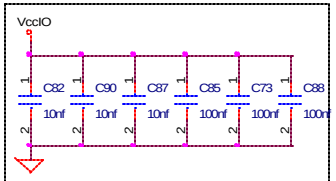
CPU1 decoupling capacitors, place as close as possible to the CPU1



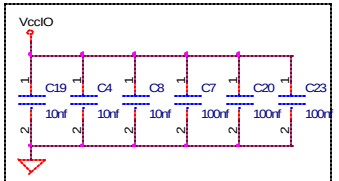




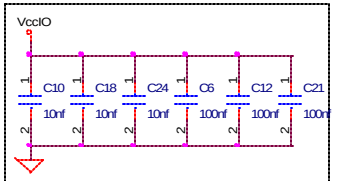
U17 decoupling capacitors, place as close as possible to U17



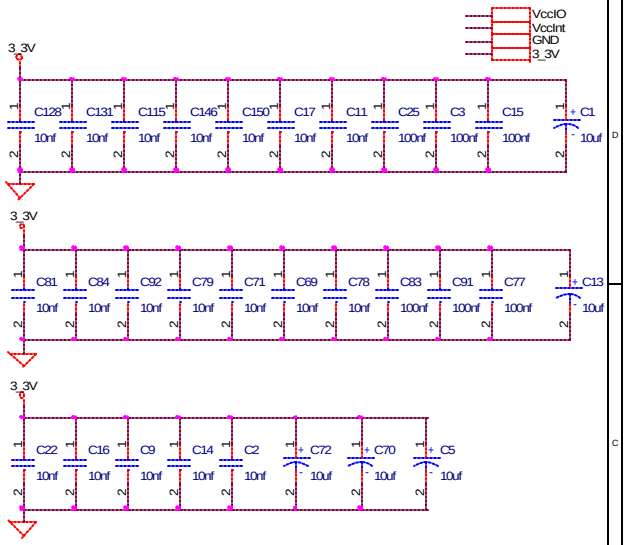
U18 decoupling capacitors, place as close as possible to U18



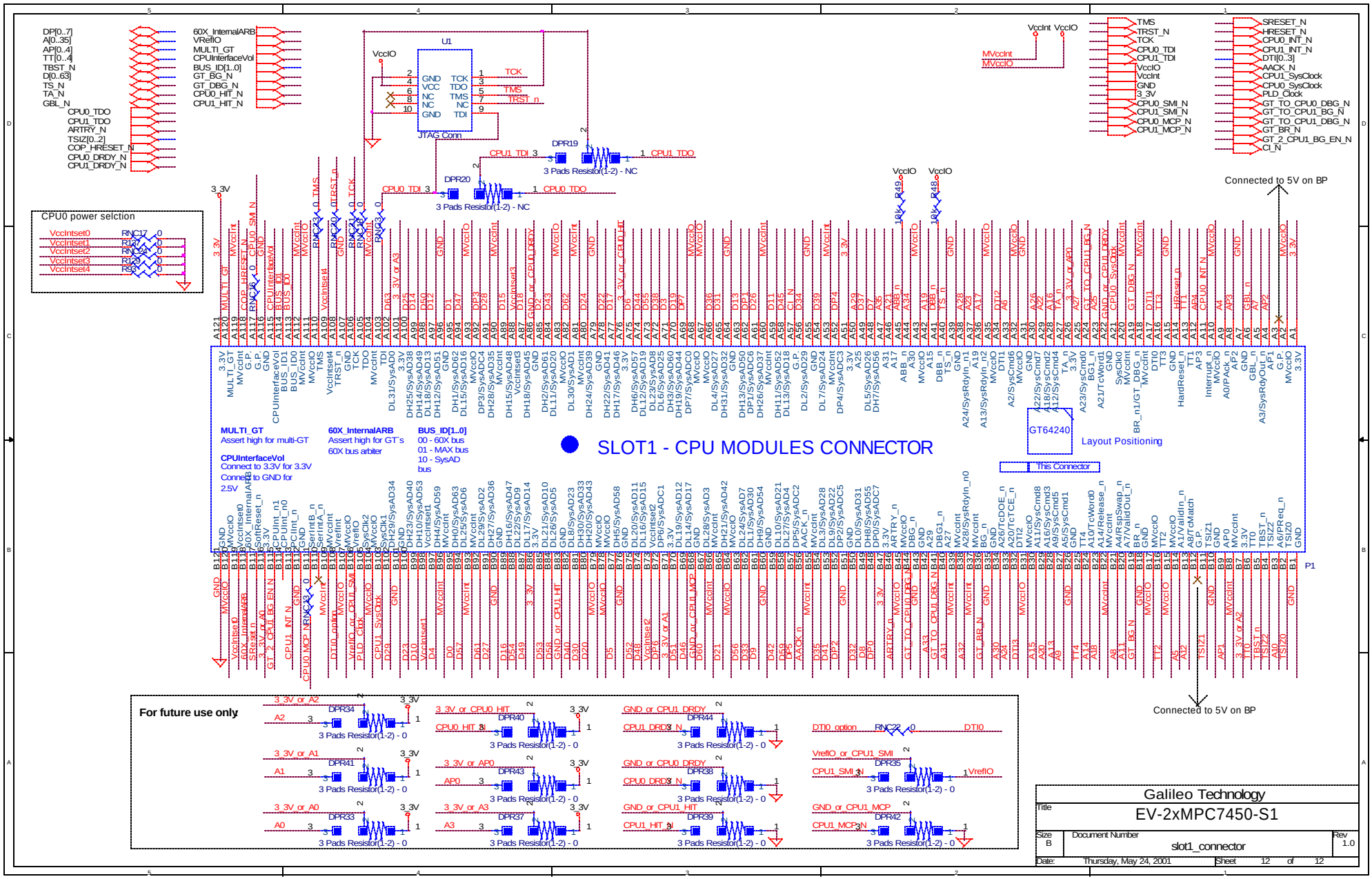
U19 decoupling capacitors, place as close as possible to U19



U20 decoupling capacitors, place as close as possible to U20



Galileo Technology		
Title: EV-2xMPC7450-S1		
Size: B	Document Number: Power	Rev: 1.0
Date: Thursday, May 24, 2001	Sheet 11 of 12	


SLOT1 - CPU MODULES CONNECTOR
MULTI_GT
Assert high for multi-GT
CPUInterfaceVol
Connect to 3.3V for 3.3V
Connect to GND for 2.5V
60X_InternalARB
Assert high for GT`s 60X bus arbiter
BUS_ID[1..0]
00 - 60X bus
01 - MAX bus
10 - SysAD bus
GT64240
Layout Positioning
This Connector
Connected to 5V on BP
Connected to 5V on BP
CPU0 power selction
For future use only
JTAG Conn
3 Pads Resistor(1-2) - NC
3 Pads Resistor(1-2) - 0
Galileo Technology
EV-2xMPC7450-S1
slot1_connector
Thursday, May 24, 2001