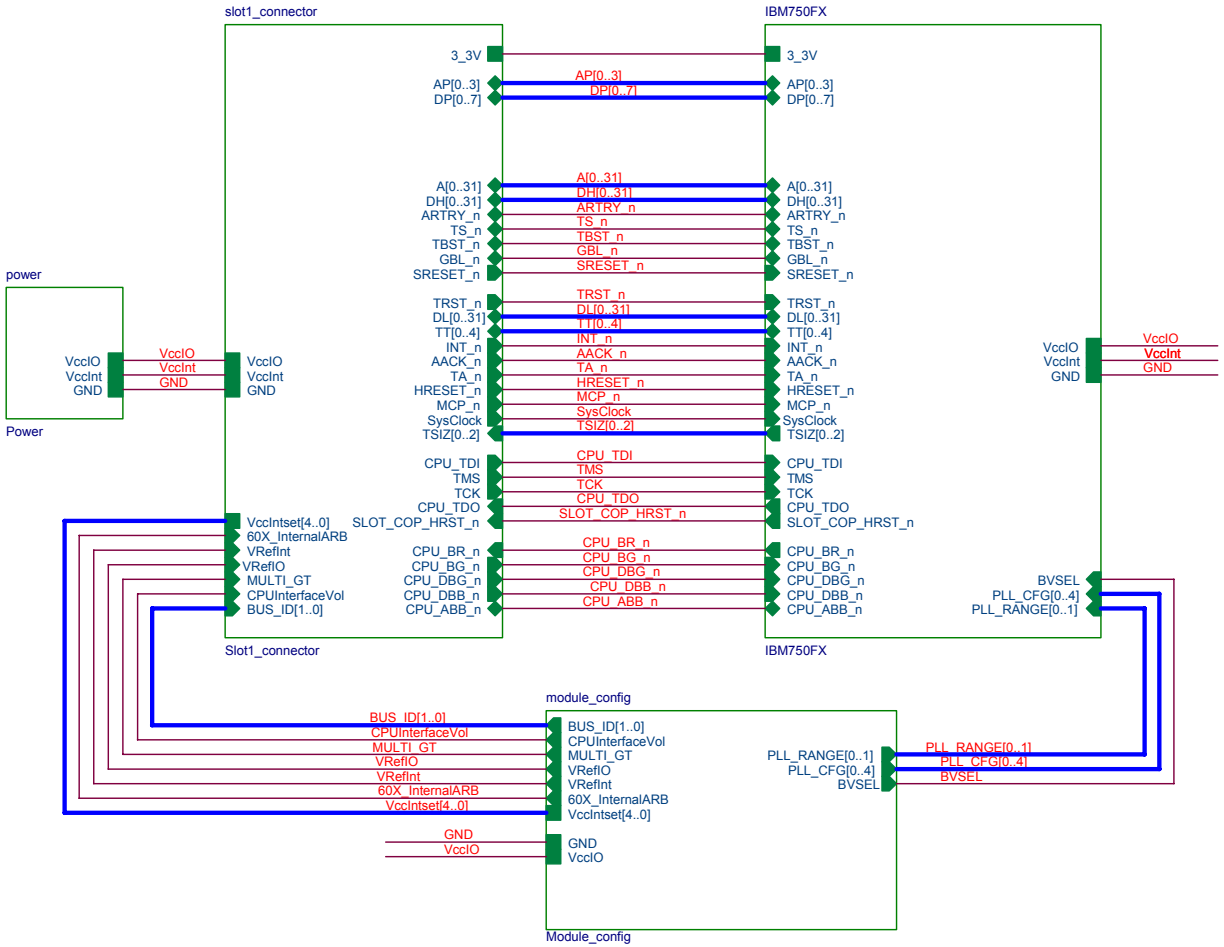

Galileo Technology		
Title: DB-IBM750FX-S1		
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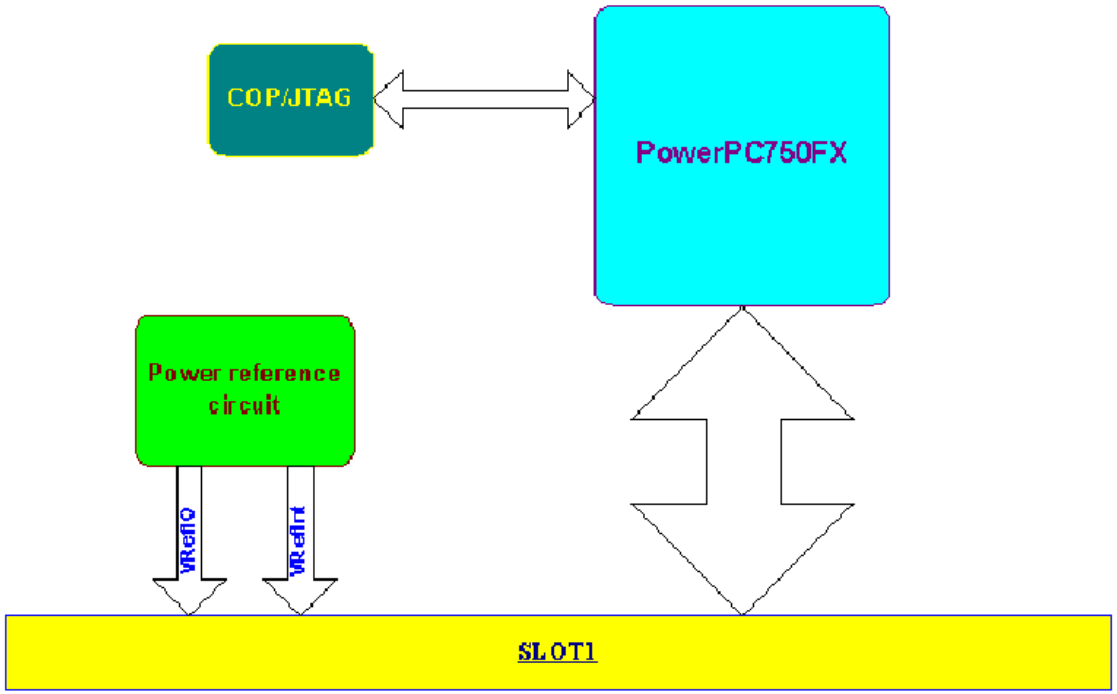
Date: Tuesday, March 25, 2003	Sheet 1 of 6	



Sheet Number:	Content:
1	Info page
2	Module - Top hierarchy.
3	PLD - 60x bus optional external arbiter
4	IBM PPC750CX
5	Module configurations
6	Decoupeling capacitors.
7	SLOT1 connector
Rev Number 0.9	Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 0.91	After rename. Preliminary release. Please make sure you have latest revision when referencing this schematic.
Rev Number 2.0	change list: 1. New PLD device. 2. mechanical space for heat sink. Preliminary release. Please make sure you have latest revision when referencing this schematic.

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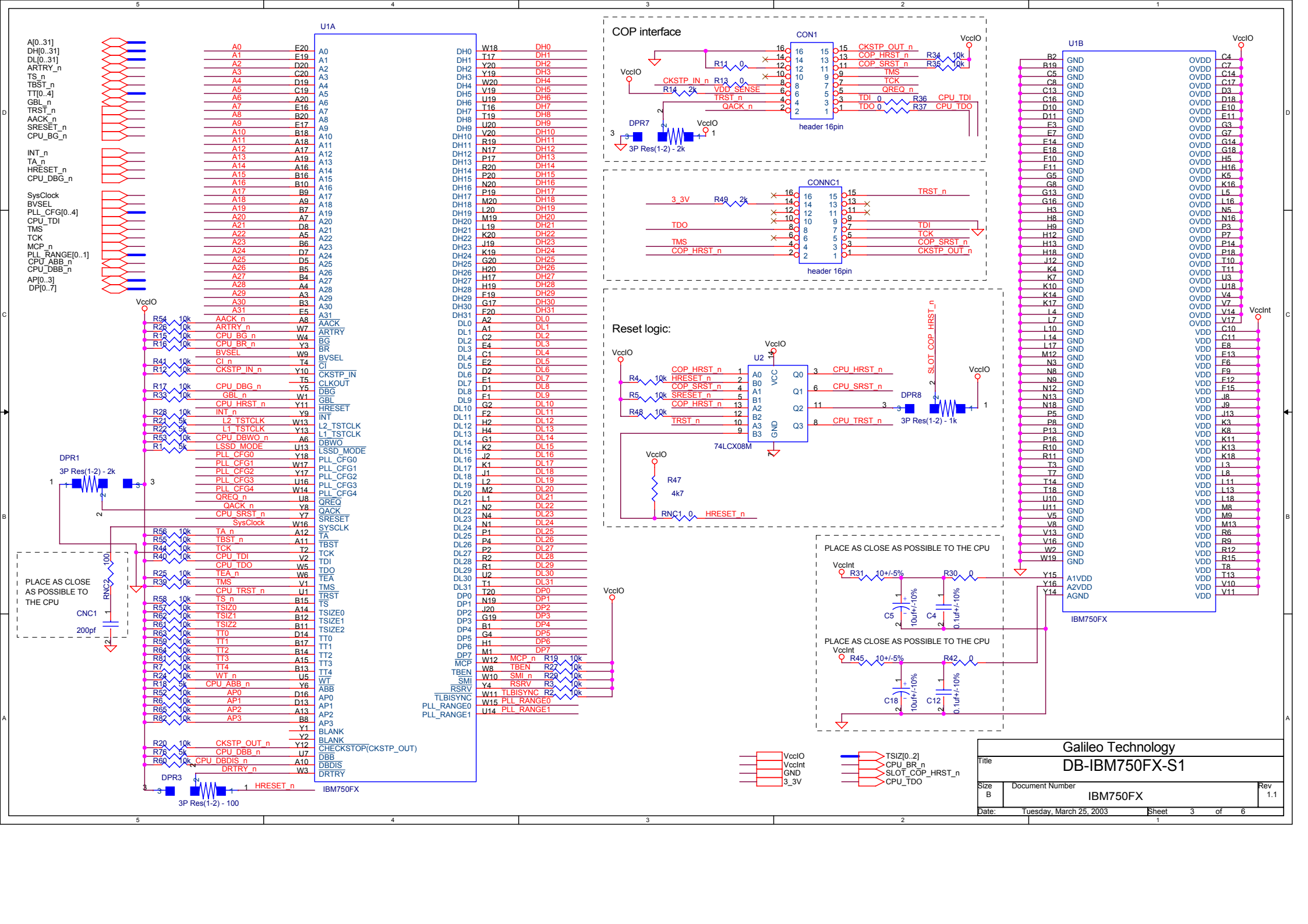
Title: EV-IBM750FX-S1		
Size: B	Document Number: block_diagram	Rev: 2.0
Date: Wednesday, November 21, 2001	Sheet 2 of 6	


COP interface
CON1
header 16pin
CKSTP_OUT_n
COP_HRST_n
COP_SRST_n
TMS
TCK
QREQ_n
TDI
TDO
CPU_TDI
CPU_TDO
CKSTP_IN_n
VDD_SENSE
TRST_n
QACK_n
DPR7
3P Res(1-2) - 2k
CONNC1
3_3V
TRST_n
TDO
TDI
TCK
TMS
COP_SRST_n
COP_HRST_n
CKSTP_OUT_n
Reset logic:
74LCX08M
SLOT_COP_HRST_n
DPR8
3P Res(1-2) - 1k
HRESET_n
U1A
IBM750FX
U1B
A[0..31]
DH[0..31]
DL[0..31]
ARTRY_n
TS_n
TBST_n
TT[0..4]
GBL_n
TRST_n
AACK_n
SRESET_n
CPU_BG_n
INT_n
TA_n
HRESET_n
CPU_DBG_n
SysClock
BVSEL
PLL_CFG[0..4]
CPU_TDI
TMS
TCK
MCP_n
PLL_RANGE[0..1]
CPU_ABB_n
CPU_DBB_n
AP[0..3]
DP[0..7]
DPR1
3P Res(1-2) - 2k
DPR3
3P Res(1-2) - 100
CNC1
200pf
RNC2
PLACE AS CLOSE AS POSSIBLE TO THE CPU
PLACE AS CLOSE AS POSSIBLE TO THE CPU
PLACE AS CLOSE AS POSSIBLE TO THE CPU
VccIO
VccInt
GND
3_3V
TSIZ[0..2]
CPU_BR_n
SLOT_COP_HRST_n
CPU_TDO
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IBM750FX
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750FX Microprocessor PLL Configuration

PLL_RANGE[0..1]

VccIO
GND
VccIntset[4..0]

BUS_ID[1..0]
CPUInterfaceVol
VRefIO
VRefInt

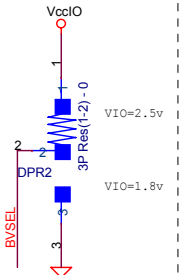
PLL_CFG[0..4]
BVSEL
MULTI_GT
60X_InternalARB

PLL_CFG [0:4]		Processor to Bus Frequency Ratio	Frequency Range Supported by VCO having an example range of VCO_{MIN} = 1000 to VCO_{MAX} = 2400MHz[6]			
			SYSCLK		Core	
bin	dec		Min	Max	Min	Max
00000	0	OFF	N/A	N/A	Off	Off
00001	1	OFF	N/A	N/A	Off	Off
00010	2	PLL Bypass[3]	N/A	N/A	N/A	N/A
00011	3	PLL Bypass[3]	N/A	N/A	N/A	N/A
00100	4	2x[1]	-	-	-	-
00101	5	2.5x[1]	-	-	-	-
00110	6	3x[1]	-	-	-	-
00111	7	3.5x	143	150[5]	500	525
01000	8	4x	125	150[5]	500	600
01001	9	4.5x	111	150[5]	500	675
01010	10	5x	100	150[5]	500	750
01011	11	5.5x	91	150[5]	500	825
01100	12	6x	83	150[5]	500	900
01101	13	6.5x	77	150[5]	500	975
01110	14	7x	71	142	500	1000
01111	15	7.5x	66	133	500	1000
10000	16	8x	63	125	500	1000
10001	17	8.5x	59	118	500	1000
10010	18	9x	55	111	500	1000
10011	19	9.5x	52	105	500	1000
10100	20	10x	50	100	500	1000
10101	21	11x	45[2]	91	500	1000
10110	22	12x	41[2]	83	500	1000
10111	23	13x	38[2]	77	500	1000
11000	24	14x	35[2]	71	500	1000
11001	25	15x	33[2]	66	500	1000
11010	26	16x	31[2]	62	500	1000
11011	27	17x	29[2]	59	500	1000
11100	28	18x	27[2]	55	500	1000
11101	29	19x	26[2]	52	500	1000
11110	30	20x	25[2]	50	500	1000
11111	31	Off[4]	N/A	N/A	N/A	N/A

Note:

1. The 2X- 3X Processor to Bus Ratios are currently not supported.
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see Table 6, "Clock AC Timing Specifications" on page 17 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock - off mode, no clocking occurs inside the 750FX regardless of the SYSCLK input.
5. The SYSCLK limit is 150MHz, as specified in Table 6 on page 16. Applications requiring SYSCLK over 150MHz will be investigated by application conditions.
6. The VCO to core clock ratio is 2X for the 750FX. VCO_{MAX} is specified in this table by the maximum core processor speed. The VCO maximum of 2400MHz reflects a processor core speed of 1200MHz, which is not currently supported.

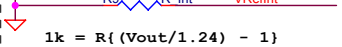
Bus voltage select:



GT64240's CPU interface bus mode:

BUS_ID[1..0] selection:
00 - 60x bus
01 - MAX bus
10 - SysADbus

Power supply voltage selection:



1k = R{(Vout/1.24) - 1}

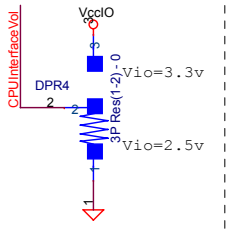
```
VccIO = 1.8v => R_IO=2.2k
VccIO = 2.5v => R_IO=1k
VccIO = 3.3v => R_IO=0.6k

VccInt = 1.4v => R_Int=7.75k
VccInt = 1.8v => R_Int=2.2k
VccInt = 2.5v => R_Int=1k
VccInt = 3.3v => R_Int=0.6k
```

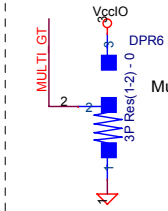
750FX PLL Range [0:1] Definitions

PLL_RNG[0:1]	PLL Frequency Range
00	700-1000 MHz
01	900-1200 MHz
10	500-800 MHz
11	Reserved.

GT64240's CPU interface voltage selection:



GT64240's multi GT selection:

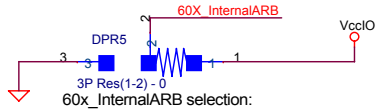


MULT_GT selection:
0 - multi GT disabled
1 - multi GT enabled

CPU power selction - configuration depends on CPU internal voltage

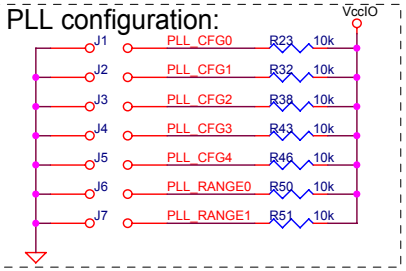
VccInt	R10	R73	R74	R72	R66
1.8v	In	In	Out	In	Out
1.65v	In	Out	In	In	In
1.4v	In	Out	Out	In	Out
1.45v	In	Out	Out	In	In

GT64240's internal arbiter selection:



60x_InternalARB selection:
0 - internal arbiter disabled
1- internal arbiter enabled

PLL configuration:



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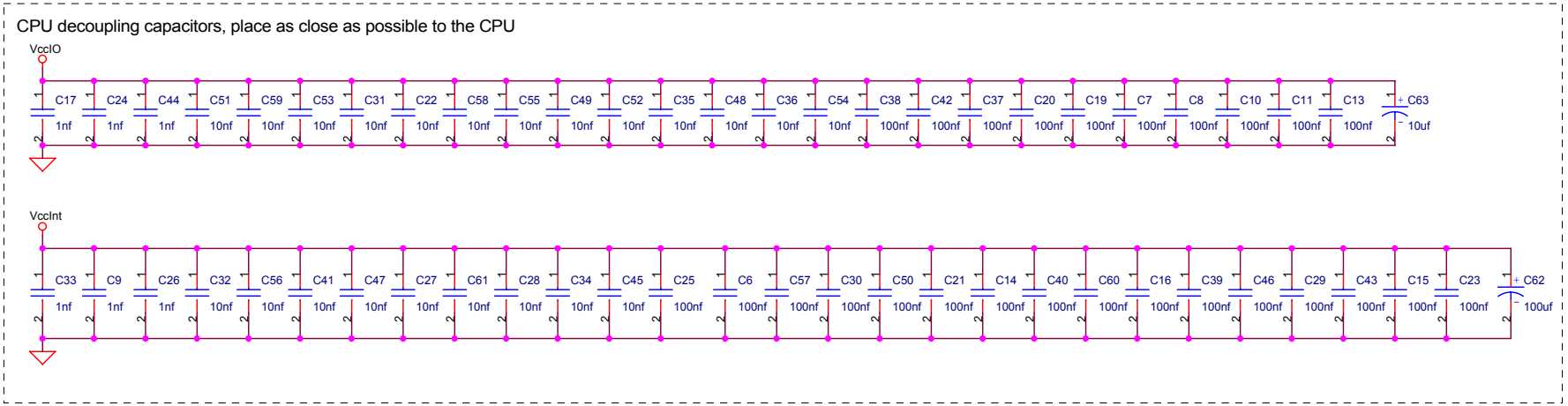

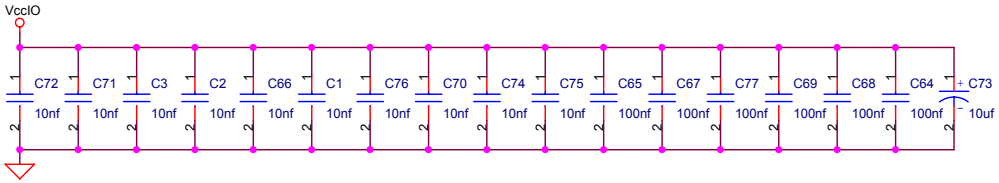

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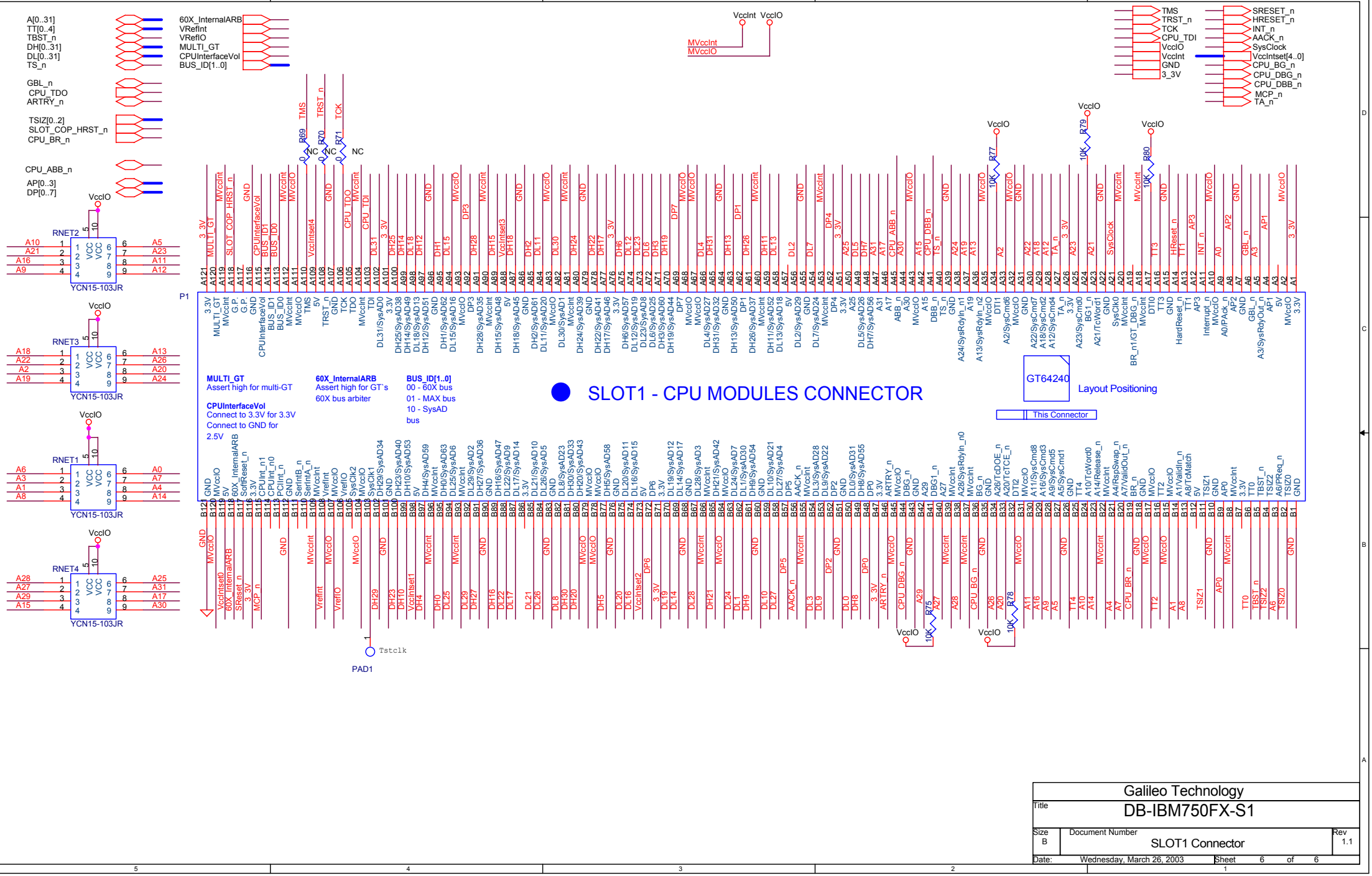

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Title: DB-IBM750FX-S1		
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