Documentation Updates and Changes

GT-64260A System Controller for PowerPC Processors Datasheet Rev. A, Dated August 29, 2001

DCU-GT-64260A

Introduction

This document provides changes to the *GT-64260A System Controller for PowerPC Processors,* datasheet, Rev. A, dated August 29, 2001.

These changes will be incorporated in a future revision of the datasheet.

Revision History

Revision	Date	Change Number and Reference to Datasheet Section	
Rev. A	October 17, 2001	Change #1	Throughout datasheet Six Pipeline Transaction Depth
		Change #2	Revised Initial Values
		Change #3	AACK Delay Clarification Section 4.7 Transactions Flow Control (page 69)
		Change #4	Correct IntDecode Field Definition Section 4.20.1 CPU Address Decode Registers Table 74. Internal Space Decode Register (page 90)
		Change #5	Correct SDClkOut/SDClkIn Section 25. Reset Configuration Table 722. Reset Configuration (page 540
		Change #6	SData[63:0] Section 27. DC Characteristics Table 730: DC Electrical Characteristics Over Operating Range (page 550)
		Change #7	AC Timing for ABB* and DBB* Section 28. AC TIMING Table 732: 100 MHz AC Timing (page 556)
Rev. B	January 14, 2002	Change #8	Pin Information Updates Section 2. Pin Information Table 4: PCI Bus 0 Interface Pin Assignments (page 35)
		Change #9	Operating in Multi-GT mode Section 4.14 PowerPC Multi-GT Mode (page 75)
		Change #10	FastClk and AACK Delay_2 Setting Section 4.20.2 CPU Control Registers Table 97: CPU Configuration, Offset: 0x000 (page 94)
		Change #11	SDRAM Refresh Frequency Section 5.9 SDRAM Refresh (page 123)
		Change #12	SDRAM Command Execution Procedure Section 5.11 SDRAM Operation Mode Register (page 125)
		Change #13	ALE Signal High Section 7. Device Controller (page 149)
		Change #14	TurnOff=2 Section 7.2.3 Acc2Next Figure 23. Device Read Parameters Example (page 150)
		Change #15	ALE2Wr Minimum Setting Inconsistency Section 7.2.4 ALE2Wr (page 151)
		Change #16	Extension of Some Device Bank Parameters Section 7.8.1 Device Control Registers Table 169: Device Bank 0 Parameters (page 158)
		Change #17	MBurst Field Setting Section 8.8.2 PCI Read Operation (page 174)

Revision	Date	Change Number and Reference to Datasheet Section	
Rev. B Continued	January 14, 2002	Change #18	Additional PD Field Details Section 8.20.2 PCI Control Registers Table 260. PCI Arbiter Control (page 222)
		Change #19	Queue Control Register Section 9.4 Messaging Unit Registers Table 395: Queue Control (page 283)
		Change #20	Ethernet Packet Transmitting Section 14.3.2 Transmit Operation (page 359)
		Change #21	PCI Pins Reset Section 24. Reset Pins (page 539)
		Change #22	Reset Configuration Corrections/Updates Section 25. Reset Configuration (page 540)
		Change #23	Unused Interfaces
		Change #24	I2C Initialization Strapping Section 25.2 Serial ROM Initialization (page 543)
		Change #25	AC Timing Measurement and Changes Section 28. AC Timing (page 556)
		Change #26	JTag AC Timing

Datasheet Updates/Changes

Change #1 Throughout datasheet Six Pipeline Transaction Depth

Description

The GT-64260A supports up to six pipelined transactions on the CPU bus.

There are several places in the datasheet incorrectly states that the pipeline depth is eight transactions.

Change #2 Revised Initial Values

Description

The following table contains the correct initial value for the following fields.

Register	Field and Bits	Revised Initial Value
CPU Master Control register, Offset: 0x160	Reserved [7:0]	0x35
Device Bankx Parameters registers, Offset: 0x45c, 0x460, 0x464, 0x468	BAdrSkew [29:28] Reserved [31:30]	0x0 0x2

Change #3 AACK Delay Clarification Section 4.7 Transactions Flow Control (page 69)

Description

The following needs to be added when working with the Motorola MPC7450:

For the Motorola MPC7450, the GT-64260A does not support 2:1 or 2.5:1 clock ratio.

Also, disregard the note:

The GT-64260A does not support AACK* delay, in MPX bus mode.

This only applies to the previous silicon revision. It does not apply to the revision A silicon.

Change #4 **Correct IntDecode Field Definition**
Section 4.20.1 CPU Address Decode Registers
Table 74. Internal Space Decode Register (page 90)

Description

The IntDecode field is incorrectly defined. The correct definition is:

Bits	Field Name	Function	Initial Value
15:0	IntDecode	GT-64260A Internal Space Base Address	0x140 or 0x01f0 The initial value is dependent on the reset strapping.
23:16	Reserved	Reserved.	0x0

Change #5 **Correct SDClkOut/SDClkIn**
Section 25. Reset Configuration
Table 722. Reset Configuration (page 540

Description

The datasheet incorrectly states the reset settings for AD[23]. The correct settings are:

- 0 = SDClkOut
- 1 = SDClkIn

This also means that the description for the SDRAM clock output and input is changed. The new description in Section 5.13.1 SDRAM Clock Output on page 128 is:

> If AD[23] pin is sampled Low during reset, the GT-64260A SDClkOut/SDClkIn pin is configured as SDClkOut (see reset configuration section).

The new description in Section 5.13.3 SDRAM Clock Input is:

> If AD[23] is sampled High during reset, the GT-64260A SDClkOut/SDClkIn pin is configured as SDClkIn. Under this configuration, the SDRAM Timing Parameters register's RdDelay [12] must be set to '1'. Setting RdDelay enables the additional sampling stage.

Change #6 **SData[63:0]**
Section 27. DC Characteristics
Table 730: DC Electrical Characteristics Over Operating Range (page 550)

Description

The SData signal is only defined as [31:0]. It should be SData[63:0]

Change #7 AC Timing for ABB* and DBB*
Section 28. AC TIMING
Table 732: 100 MHz AC Timing (page 556)

Description

The ABB* and DBB* signals are mistakenly listed with other setup and hold signals.

The ABB* and DBB* signals are not inputs and don't belong with the setup and hold signals. They are listed correctly with the output delay signals.

Change #8 Pin Information Updates
Section 2. Pin Information
Table 4: PCI Bus 0 Interface Pin Assignments (page 35)

Description

- P64En should appear as P64En*.
  Also, when 64En* appears in the document it should be P64En*.
- In the description for CSTiming, add that this pin is in High-Z during reset assertion and for two cycles after reset de-assertion. A pull up may be added to avoid an erroneous qualification of the Device_CS* signals.

Change #9 Operating in Multi-GT mode
Section 4.14 PowerPC Multi-GT Mode (page 75)

Description

Add the following notes:

Operating in multi-GT mode affects the AC Timing. Before implementing multi-GT support, consult with your local FAE.

Multi-GT mode can be used to connect a slave unit other than the GT-64260A. Before attempting to connect an alternate slave unit, consult with your local FAE.

Change #10 FastClk and AACK Delay_2 Setting
Section 4.20.2 CPU Control Registers
Table 97: CPU Configuration, Offset: 0x000 (page 94)

Description

For the FastClk bit [23] setting, the following note must be included:

If the system clock is higher than 100Mhz, must be set to '1'. The AC timing for the two pipe stages mode ('0') is TBD.

For the AACK Delay_2 bit [25] setting in Table 97: CPU Configuration register, the following note must be included:

Not supported in MultiGT mode. If MultiGT is enabled, it is impossible to interface CPUs in which the ARTRY* window is delayed. For example: If a system is using MPC7450 CPU, the CPU core clock ratio must be selected to be higher than or equal to 1:5.

Change #11 SDRAM Refresh Frequency
Section 5.9 SDRAM Refresh (page 123)

Description

Section incorrectly states the refresh sequence as occurring every 5.12us, if the TClk cycle is 133MHz. In fact, at 133MHz, a refresh sequence occurs every 3.84us.

Change #12 SDRAM Command Execution Procedure
Section 5.11 SDRAM Operation Mode Register (page 125)

Description

In the procedure to execute a command on the SDRAM, add the following step between step #2 and #3:

Write the new configuration data to the SDRAM Timing Parameters register (offset: 0x4b4).

Change #13 ALE Signal High
Section 7. Device Controller (page 149)

Description

Several timing figures in this section incorrectly show the ALE signal not in a high state for the minimum four clock cylces. This is incorrect. The minimum amount of clock cycles that ALE will be high is four (4).

Figures 26, 27 and 28 show the Ready* signal as "don't care" during the begining of the Xaction. The Ready* signal must reflect the state of the data (ready or not ready) From the time ALE is asserted. In general, it is recommended that Ready* only be asserted when data is ready to be sampled.

Change #14 TurnOff=2
Section 7.2.3 Acc2Next
Figure 23. Device Read Parameters Example (page 150)

Description

The figure incorrectly states “TurnOff=1”. In fact, the figures should state that “TurnOff=2”

Change #15 ALE2Wr Minimum Setting Inconsistency
Section 7.2.4 ALE2Wr (page 151)

Description

The minimum setting for ALE2Wr is 0x3 (three clock cycles). This is correct.

This parameter is incorrectly written in Figure 24. Device Write Parameters Example.

Change #16 Extension of Some Device Bank Parameters
Section 7.8.1 Device Control Registers
Table 169: Device Bank 0 Parameters (page 158)

Description

The timing parameters in this register can be extended by using their counterpart extension parameters, also located in this register.

Timing Parameter	Extension Timing Parameter
TurnOff [2:0]	TurnOffExt [22]
Acc2First [6:3]	Acc2FirstEx [23]
Acc2Next [10:7]	Acc2NextExt [24]
ALE2Wr [13:11]	ALE2WrExt [25]
WrLow [16:14]	WrLowExt [26]
WrHigh [19:17]	WrHighExt [27]

Change #17 MBurst Field Setting
Section 8.8.2 PCI Read Operation (page 174)

Description

This section incorrectly states that the single burst transaction size depends on the setting in RdBurst.

MBurst is the correct name of the field that sets the single burst transaction size. MBurst is bits [21:20] in the PCI Access Control Base x (Low) register.

Change #18 Additional PD Field Details
Section 8.20.2 PCI Control Registers
Table 260. PCI Arbiter Control (page 222)

Description

The following details need to be included in the description of the PD field, bits [20:14]:

- PD0 corresponds to the internal master.
- PD1 corresponds to GNT0.
- PD2 corresponds to GNT1, and so on

Additionally, in Section 8.3.2 Internal PCI Arbiter, the bit range for the PD field is mistakenly stated as [21:14]. The correct bit range is [20:14].

Change #19 Queue Control Register
Section 9.4 Messaging Unit Registers
Table 395: Queue Control (page 283)

Description

Bit 8 in this register is not reserved. The correction is:

Bits	Field Name	Function	Initial Value
8	Polarity	Polarity Select 0 - Inbound and Outbound Mask register bits are active high (1 means that interrupt is masked), Inbound and Outbound Doorbell registers bits toggle when writing 1, Inbound and Outbound Interrupt Cause registers bits are cleared by writing '1'. 1 - Inbound and Outbound Mask register bits are active low (0 means that interrupt is masked), Inbound and Outbound Doorbell registers bits toggle when writing 0, Inbound and Outbound Interrupt Cause registers bits are cleared by writing '0'.	0x0

Also, there is a change to bits in the Inbound Interrupt Mask and Outbound Interrupt Mask registers. In the description, include:

If set to the same value as the Queue Control register's Polarity bit [8], the interrupt is enabled.

Change #20 Ethernet Packet Transmitting
Section 14.3.2 Transmit Operation (page 359)

Description

Add information that the Ethernet unit pre-fetches the next packet to transmit before the current packet transmission ends. This is to ensure low Tx latency. This means that a Tx descriptor that points to itself must never be used. This type of structure might cause the packet to be transmitted twice.

Also, the first step in the procedure for the CPU to initialize a transmit operation should read:

Prepare a chained list of **multiple** descriptors and packet buffers.

Note

When handling Tx or Rx queues, the DMA only stops processing the queue after the packet with the Next Descriptor Pointer field equaling NULL is processed. The descriptor is closed properly and its buffer is transmitted. No resource error interrupt is generated.

Change #21 PCI Pins Reset
Section 24. Reset Pins (page 539)

Description

Add to the following note for resetting the PCI pins.

- PCI reset may be de-asserted at or after SysRst de-assertion.
- SysRst MUST be asserted AT or AFTER PCI reset assertion.

Change #22 Reset Configuration Corrections/Updates
Section 25. Reset Configuration (page 540)

Description

It must be noted that after reset de-assertion there must be a period of at least ten (10) TClk cycles before the first access from the CPU can take place.

In Table 722. Reset Configuration, note the following changes or corrections.

Pin	Change or Update
AD[8]	Disregard the note for AD[8] that states: **NOTE:** If using the MPX bus mode, AD[8] must be set to 1. This note is not applicable to the GT-64260A.
AD[13]	AD[13] must be pulled low (set to ‘0’). This setting means that the UMA is configured as the master. Even if AD[12] is set to not support (disable) the SDRAM UMA, AD[13] must be set to ‘0’. Otherwise, the SDRAM interface is inactive and the external signals are not driven. **NOTE:** Only systems that ARE going to use the UMA function may set this bit to ‘1’.
AD[29:28]	Only pull down is needed.

Change #23 Unused Interfaces

Description

The following table shows the pin strapping if an interface is not in use.

Unused Interface	Strapping
CPU	GND: SysClk Pull Up: A[31:0], AP[0:3], BR0, BR1, TS, TBST, TSIZ[0:2], TT[0:4], ARTRY Pull down AD[5] and AD[9:6].

Unused Interface	Strapping
Ethernet	If not using port E0, pull down all of its inputs. To minimize the number of pull downs, configure the port to MII and pull down pins E0[1] and E0[14:6]. If not using port E1, pull down all of its inputs. To minimize the number of pull downs, configure the port to MII and pull down pins E1[1] and E1[14:6].
MPSC	If not using port S0, configure the port to MPSC and pull down pins S0[6:0]. If not using port S1, configure the port to MPSC and pull down pins S1[1] and S1[6:3].
I^2C	Pull up I2CSCK and I2CSDA.
MPP	All signals must be configured as outputs. **NOTE:** It is recommended to pull these signals either high or low so the hardware will be protected from software errors.
SDRAM	The following reset pins must be configured as follows: • Set AD[12] and AD[13] to '0' to disable UMA support. • Set AD[23] to '0' to support SDClkOut.
Device	Pull down the Ready* pin.
PCI	To bypass the need of putting pull ups on the data signals (AD[63:0], CBE0/1[7:0], PAR0/1, PAR640/1). 1) Connect the PCI Rst0/1 to the Sysrst*. 2) Pull down the GNT0/1*. 3) Connect the PCI Clk0/1 to a clock (could be a very slow clock, need just several cycles). DevSel, Trdy, Stop, Ack64,PERR, SERR, HS, P64En

Change #24 I2C Initialization Strapping
Section 25.2 Serial ROM Initialization (page 543)

Description

There are additional required strapping to those currently listed in the datasheet.

All of the following pins must be configured to the intended value during Serial ROM initialization.

Pin	Description
AD[1]	Serial ROM Byte Offset Width
AD[3:2]	Serial ROM Address
AD[4]	CPU Data Endianess
AD[7:6]	CPU Bus Configuration.
AD[8]	Internal 60x bus Arbiter.
AD[9]	Multiple GT-64260A Support.

Pin	Description
AD[11:10]	Multi-GT-64260A Address ID
AD[12]	SDRAM UMA.
AD[13]	UMA Device Type.
AD[16]	PCI Retry.
AD[23]	SDClk select.
AD[24]	Internal Space Default Address
AD[28:30]	PLL Settings
AD[31]	CPU Interface Voltage.

Change #25 AC Timing Measurement and Changes
Section 28. AC Timing (page 556)

Description

The measurements are made from the mid-point of the clock, to the mid-point of the output signal (50% -> 50%).

The note explaining about the timing impact on the setup, hold, and output delay parameters when using a CPU interface with SysClk no longer applies. Disregard this note.

Also, note the following changes to the CPU interface 133 MHz AC timing.

Note

The following AC timing numbers are an addition to the CPU interface numbers in the current data sheet. These additions apply to cases when the device is working in the mode that SysClk and Tclk are NOT synchronized (AD[5] is sampled low at reset). In this case, the internal PLL is not used for the CPU interface. This results in improved setup timing and larger hold and clock-to-out numbers.

Signals	Description	133MHz		Units	Loading
		Min.	Max.		
Clock					
SysClk	Frequency	20	125	MHz	
SysClk	Cycle Time	8	50	ns	
SysClk	Clock High	3.6	4.4	ns	
SysClk	Clock Low	3.6	4.4	ns	
SysClk	Rise Time		2	ns	

SysClk	Fall Time		2	ns	
CPU Interface NOTE: All CPU interface Output Delays, Setup, and Hold times are referred to SysClk rising edge. Skewing of the SysClk coming into the GT-64260A, in reference to the the clock going to the CPU, may be needed and can help achieve higher frequencies.					
DH[31:0], DL[31:0]	Setup	-0.8		ns	
AP[3:0], TSIZ[2:0]	Setup	-1.7		ns	
DP[7:0], TBST*	Setup	-1.1		ns	
A[31:0]	Setup	-0.98			
TS*, TT[4:0]	Setup	-0.7		ns	
BR0*/GT_BG*, BR1*/GT_DBG*	Setup	-0.5		ns	
NOTE: GT_BG* and GT_DBG* are only relevant when using an external arbiter.					
ARTRY*	Setup	0.39		ns	
AACK*, TA* NOTE: Only relevant for multi-GT configurations.	Setup	0.95		ns	
TS*, A[31:0], AP[3:0], TT[4:0], TBST*, TSIZ[2:0], ARTRY*, DL[31:0], DH[31:0], DP[7:0], BR0*/GT_BG*, BR1*/GT_DBG*, AACK*, TA*	Hold	1.15		ns	
NOTE: AACK*, TA* are only relevant for multi-GT configurations. GT_BG*, and GT_DBG* are only relevant when using an external arbiter.					
BG0*, BG1*, DBG0*, DBG1*, TS*	Output Delay	3.1	6.5	ns	15pF
AACK*, TA*	Output Delay	3.23	6.85	ns	15pF
AP[3:0], TBST*, TSIZ[2:0], TT[4:0]	Output Delay	2.85	6.9	ns	15pF
DTI[2:0]	Output Delay	2.9	6.2	ns	15pF
ABB*	Output Delay	3.12	6.67	ns	15pF
DBB*	Output Delay	3.2	6.6	ns	15pF
A[31:0], GBL*	Output Delay	3.2	7.75	ns	20pf

DH[31:0], DL[31:0], DP[7:0],	Output Delay	3.45	7.8	ns	20pF
GT_BR* NOTE: Only relevant when using an external arbiter.	Output Delay	3.1	6.45	ns	20pF

Change #26 JTag AC Timing

Description

The following parameters must be added to the 133 MHz AC Timing table.

		133MHz			
Signals	**Description**	**Min.**	**Max.**	**Units**	**Loading**
Clock					
TClk	Frequency	66	133	MHz	
TClk	Clock Period	7.5	15	ns	
TClk	Duty Cycle	40	60	%	
TClk	Slew Rate		1	V/ns	
TCK	Frequency	0	3	MHz	
TDI	SetUp	15		ns	
TDI	Hold	10		ns	
TDO	Output Delay (from falling edge of TCK)	2	20	ns	

Marvell, 2350 Zanker Road
San Jose, CA 95131
Phone: 1 408 367-1400, Fax: 1 (408) 367-1401
http:\\www.marvell.com