Introduction

This document provides changes to the GT–64240 and GT–64260 Datasheets Rev. 1.1, Dated Dec. 18, 2000.

These changes will appear in a future release of these datasheet.

Datasheet Corrections/Updates

Change #1: Section 2. Pin Information (GT–64240 Only) Table 3: CPU Interface Pin Assignments (page 25)

Description

The following information must be noted when working with these pins:

Table 1: Additional CPU Pin Information

Pin Name/ Ball #	Type	Full Name	Description
PReq* A26	I	Processor Request	CPU requests from the GT–64240/60 for SysAD bus mastership. **NOTE:** If interfacing with a CPU that does not support Preq*, pull up is required on this pin.
TcTCE* G30	I	Ternary Cache Tag RAM Chip Enable	The CPU L3 cache controller signals that it is accessing L3 cache. **NOTE:** If interfacing with a CPU that does not support TcTCE*, pull up is required on this pin.
TcMatch C29	I	Ternary Cache Tag Match	Asserted by tag RAM on L3 cache tag match. **NOTE:** If there is no L3 cache, connect the TcMatch input to GND.

Change #2: Table 97: CPU Configuration, Offset: 0x000 (GT–64260 Only) (page 90)

Description

The `AACK Delay bit` [11] is not supported in the MPX mode. The GT–64260 always asserts `AACK*` on the cycle after `TS*`, as if `AACK Delay` is set to ‘0’.

Change #3: Section 4.21.2 CPU Control Registers (GT–64260 Only) Table 99: CPU Master Control, Offset: 0x160 (page 93)

Description

Clarification that when running in MPX mode the `IntArb` bit [8] must be set to ‘1’.

Change #4: Section 5.15.1 SDRAM Configuration Registers (GT–64240) Table 127: SDRAM Configuration, Offset 0x448(page 120)

Section 5.15.1 SDRAM Configuration Registers (GT–64260) Table 144: SDRAM Configuration, Offset 0x448 (page 130)

Description

Bits [15:14] are reversed in the datasheet rev. 1.1. The correct functionality is as follows:

Table 2: Enable Virtual and Enable Physical Banks Settings

Bits	Field Name	Function	Initial Value
14	VInterEn	Enable Virtual banks (within the same SDRAM device) Interleaving 0 - Interleaving enabled 1 - Interleaving disabled	0x0
15	PhInterEn	Enable Physical banks (SCS[3:0]*) Interleaving 0 - Interleaving enabled 1 - Interleaving disabled	0x0

Change #5: Section 7. Device Controller (GT–64240) (page 136)

Section 7. Device Controller (GT–64260) (page 146)

Description

In future revisions, a new note will be added to this section that states:

> All device controller signals, including `CSTiming*`, are floated for the entire reset assertion period and an additional five `TClk` cycles after reset deassertion. Since the device chip select is qualified with `CSTiming*`, this signal must be pulled up or driven for the five additional cycles by some external logic, to prevent undesired accesses to the device.

Change #6: **Section 14.6.4 Channel Registers (CHxRx) for HDLC Mode (GT–64240)**
Table 597: CHR10 - Event Status Register (ESR) (page 407
Section 14.8.5 Channel Registers (CHxRx) for UART Mode)
Table 611: CHR10 - UART Event Status Register (ESR) (page 432

Section 15.6.4 Channel Registers (CHxRx) for HDLC Mode (GT–64260)
Table 637: CHR10 - Event Status Register (ESR) (page 428)
15.8.5 Channel Registers (CHxRx) for UART Mode
Table 651: CHR10 - UART Event Status Register (ESR) (page 453)

Description

For field RHS bit [5], the following settings apply:

Table 3: Rx in Hunt State Mode Settings

Mode	Setting '0'	Setting '1'
HDLC	Rx out of hunt state.	Rx in hunt state
UART	Rx in hunt state	Rx out of hunt state.

Change #7: **Section 15.1 SDMA Overview (GT–64240) (page 441)**

Section 16.1 SDMA Overview (GT–64260) (page 462)

Description

Incorrectly states that there are three SDMA channels.

The part contains only two SDMA channels.

Change #8: **Section 19.4 MPP Interface Registers (GT–64240) (page 468)**

Section 20.4 MPP Interface Registers (GT–64260) (page 489)

Description

In the MPP Control2 register table, the correct offset is **0xf008**. The published offset 0xf0008 is incorrect.

The correct offset for the MPPControl3 is 0xf00c.

Change #9: Section 24.1 Pins Sample Configuration (GT–64240) Table 683: Reset Configuration (page 505)

Section 25.1 Pins Sample Configuration (GT–64260) Table 723: Reset Configuration (page 526)

Description

The setting for AD[30] Bypass PLL are:

- 0: PLL Enabled (pull down)
- 1: PLL Disabled (pull up)

Also, for GT–64240 only, `AD[7:6]` must be strapped to 10.

Change #10: Section 24.2 Serial ROM Initialization (GT–64240) (page 508)

Section 25.2 Serial ROM Initialization (GT–64260) (page 529)

Description

When using serial ROM, the pins `AD[3:0]` and `AD[31:28]` must be configured (pulled up or pulled down) as specified in the reset configuration table. These pins that control the serial ROM initialization, PLL configuration, and the CPU interface voltage.

Change #11: Section 26.4 Thermal Data (GT–64240) Table 688: Thermal Data for The GT–64240 in BGA 665 (page 516)

Section 27.4 Thermal Data (GT–64260) Table 728: Thermal Data for The GT–64260 in BGA 665 (page 537)

Description

Disregard all the information about thermal management contained in this section before the thermal data table. For further information, see AN-63: Thermal Management for Galileo Technology Products.

Corrected the junction to ambient thermal resistance symbol. The following table uses the correct symbols.

Note

The values are unchanged from the datasheet. The only change was to the junction to ambient thermal resistance symbol.

Table 4: Thermal Data for The GT–64240/60 in BGA 665

Airflow	Definition	Value		
		0 m/s	1 m/s	2 m/s
Θja	Thermal resistance: junction to ambient.	13.3 C/W	12.1 C/W	10.8 C/W
Ψjt	Thermal characterization parameter: junction to case center.	0.28 C/W	0.31 C/W	0.38 C/W
Θjc	Thermal resistance: junction to case (not air-flow dependent)	4.7 C/W		

Change #12: Section 27 AC Timing (GT–64240) Table 689: AC Timing (page 520)

Section 28 AC Timing (GT–64260) Table 729: AC Timing (page 537)

Description

In the Device Interface section of the AC Timing table, the 3ns setup parameter for Ready* only applies if the Device Interface Control register's ReadyS* field (bit[18]) is set to '1'.