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TR-800 GSM/GPRS Module
Customer Design Guide

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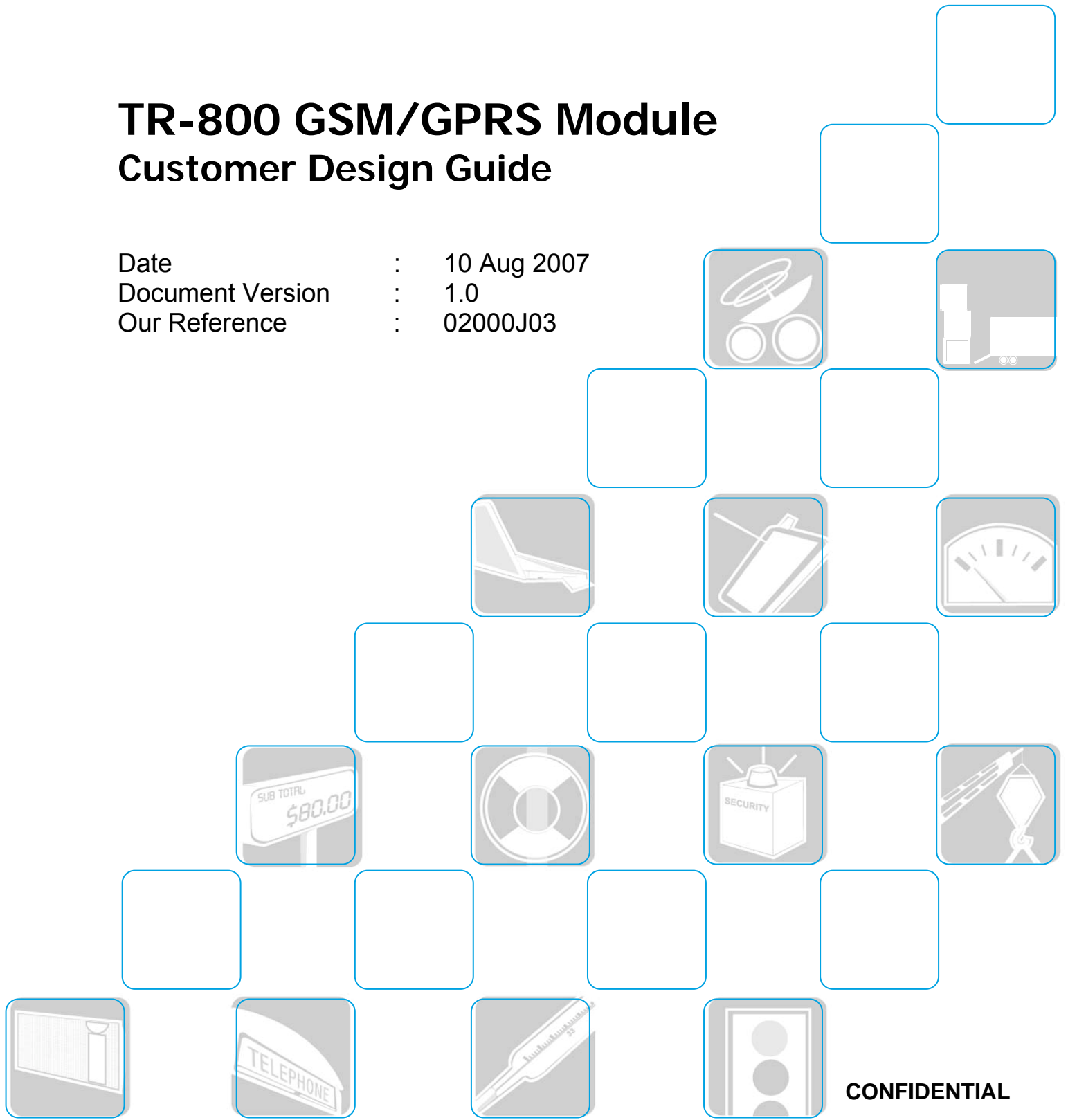
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1. INTRODUCTION

The TR-800 GSM/GPRS module is a quad-band module that is specifically design to meet the demands and stringent requirements in the M2M market. Its ease of integration into a new product or existing designs as a replacement makes this module extremely user-friendly.

The purpose of this document is to provide the user with some recommendations and general guidelines during design of TR-800 GSM/GPRS module into the product.

General Information provided includes;

- Baseband Design
- RF Design
- PCB Design
- Mechanical Recommendations

However, it is important to take note that these are guidelines and should be used as reference only. Ultimately, a design engineer has to understand how the product works, in order to achieve a good PCB layout that will work to its optimum performance.

A good RF design layout is the foundation to a successful project rollout. It is advisable to have at least 1 pilot print before mass production.

The **Customer Design Guide** is to be used with reference to the **Product Technical Specifications**.

1.1. Reference documents

S/N	Document	Our Reference	File
1	Product Technical Specifications	02000B06	TR800_PdtTechSpecsv2.4

2. BASEBAND DESIGN

2.1. Digital IO and Peripherals Design

2.1.1. GPIOS

There are 8 GPIOs available on the modules.

Description	Pin	Default Configuration	Alternate Function
GPIO1	29	O	RI
GPIO2	30	O	DCD
GPIO3	31	O	DTR
GPIO4	35	I	RESETOUT
GPIO5	34	I	MTXD
GPIO6	32	I	MRXD
GPIO7	28	I	MCLK
GPIO8	33	I	MFSYNCH

Ensure ESD protection diodes are in placed whenever it is possible. Check the default values for GPIOs, for inputs, tie to ground. Refer to electrical characteristics table below for more information on maximum and minimum voltage ratings.

Electrical Characteristics:

Parameters	Conditions	Min	Nom	Max	Unit
High level input voltage, V_{IH}		0.7VIO	-	VIO+0.5	V
Low level input voltage, V_{IL}		-0.5	-	0.3VIO	V
High level output voltage, V_{OH}	At rated current	0.8VIO	-	-	V
Low level output voltage, V_{OL}	At rated current	-	-	0.22VIO	V
Rated output high current, I_{OH}		-	-	1	mA
Rated output low current, I_{OL}		-	-	1	mA

2.1.2. Parallel Bus Interface

The 16 bit parallel buses are high speed data lines that can be used for controlling external peripherals such as LCD display.

Design Considerations:
- It is important to maintain symmetrical traces as much as possible and with proper shielding.
- Ensure that the traces do not interfere with other RF traces. These traces are a source of noise and can have severe impact on module performance.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.1.3. I²C Interface

I²C is a half-duplex serial port for data transmission with software configurable address device. The interface is compliant with Philips (NXP) standards. The main features are:
- single master only
- standard speed (100KHz) and fast (400KHz) transmission modes
- support both burst write, single read and combine read modes
- transmit burst buffer of 16 words

- 3 bits programmable spike filtering logic
- Error handling capability during I2C bus access

For additional information, refer to PCB Design Guideline in clause 5.
Refer to product specifications for maximum and minimum voltage ratings.

2.1.4. SPI Interface

The module does not support SPI interface.

2.1.5. 5X5 Keypad Interface

There are 5 columns and 5 rows pins which are typically 3.3V signal. KBR (4:0) are input pins for row lines and KBC (4:0) are output pins for column lines. If the button on the matrix is pressed, the corresponding row and column lines are shorted together.
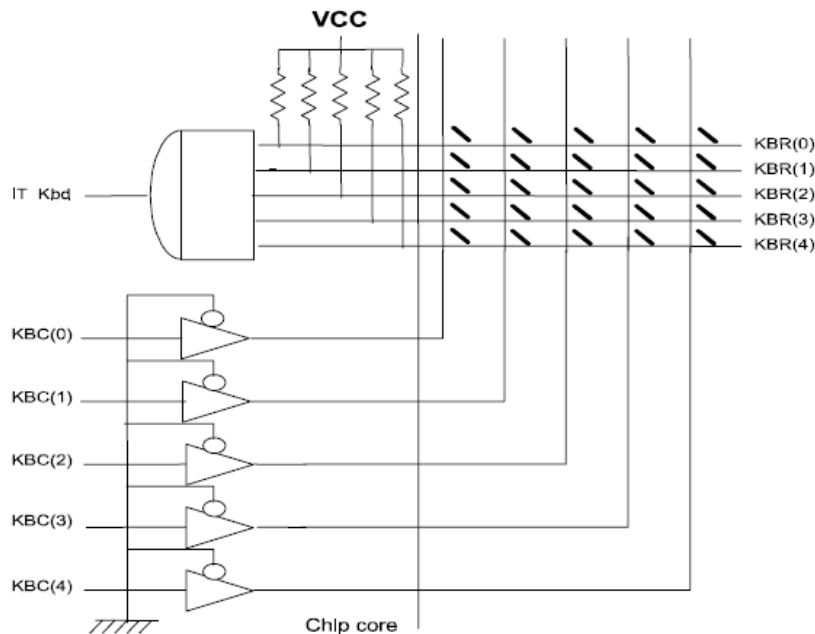

Figure 1 : Keypad Interface

KBRs are internally tied to VCC and KBCs are driving a low level. When a button is pressed, it will be detected accordingly as an interrupt. This will be sent to the micro-controller which will scan the column lines with the following sequences. It is possible to allow detection of several pressed actions on several key buttons.

A 33pF capacitor is recommended at each keypad input to eliminate ghosting effect.

	Reset	Idle	Keyboard Scanning						Idle
KDC(0)	1	0	1	0	1	1	1	1	0
KDC(1)	1	0	1	1	0	1	1	1	0
KDC(2)	1	0	1	1	1	0	1	1	0
KDC(3)	1	0	1	1	1	1	0	1	0
KDC(4)	1	0	1	1	1	1	1	0	0

Refer to PCB Design Guideline in clause 5.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.1.6. SIM Interface

The SIM card interface is fully compliant with the GSM 11.11 and ISO/IEC 7816-3 standards.

The SIM card interface can be programmed for 1.8V or 3V SIM card. To allow the use of 1.8V and 3V SIM cards, a SIM level shifter is required to interface TR-800 GSM/GPRS module to the SIM signals at contact V-IO level. An LDO will generate a 1.8V or 2.9V supply at the V_SIM terminal from the main battery supply.

5V adaptation will be based on external level shifters.

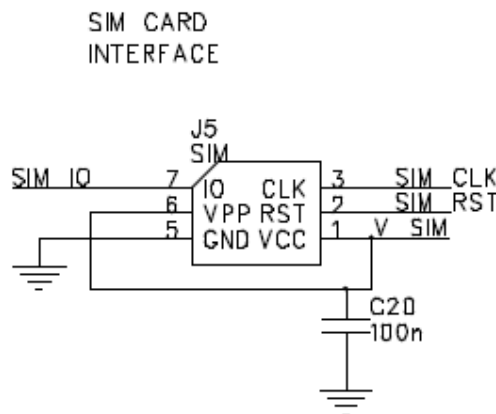See schematic for typical SIM interface connection in figure 2.

Figure 2: SIM Card Interface

Design Recommendations:
- Capacitors should be placed as close as possible to the SIM card interface
- The length of traces should be kept as short as possible.
- Ensure ESD protection diodes are placed whenever possible at signals connected to SIM socket.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.1.7. UART Interface

The UART interface is compatible with NS 16C750 device. Refer to EIA-232 interface standards for pin connections. Baud rate is configurable from 1200 to 115.2Kbits/s.

UART1, which is the modem port, is the primary UART serial link and is used for upgrading of firmware and for normal communication.

UART2 is the secondary UART serial link and is used as the debug port. It can be configured to become an auxiliary UART port.

UART1 – Pin Description:

Signal	Pin Number	Type	Description
TXD	51	Input	DCE Data Receive
RXD	52	Output	DCE Data Transmit
CTS	53	Output	Clear To Send. Hardware flow control
RTS	54	Input	Ready To Send. Hardware flow control

UART2 – Pin Description:

Signal	Pin Number	Type	Description
TXD2	49	Input	DCE Data Receive 2
RXD2	50	Output	DCE Data Transmit 2

The block diagram in figure 3 below shows how the module can be connected to other peripherals using the 2nd UART.
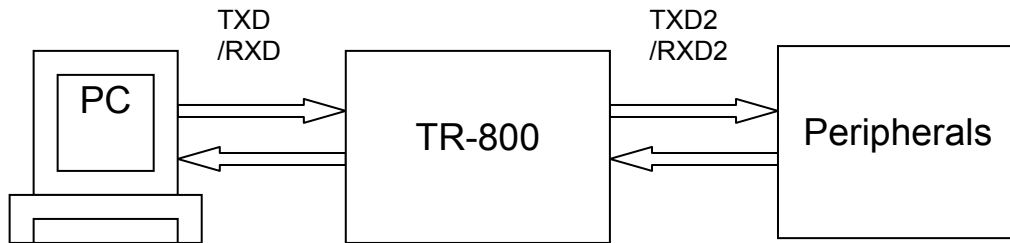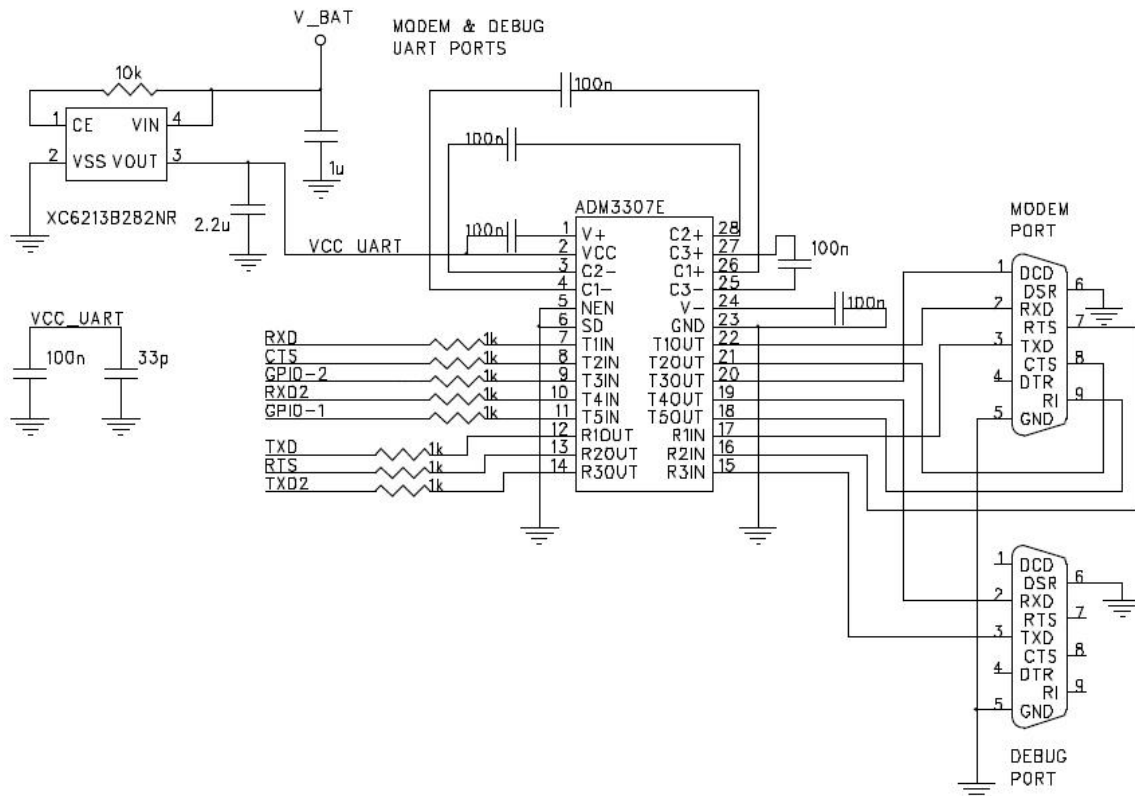

Figure 3: Interfacing with UART

Figure 4: Level-shifter connection to RS232

Ring Indicator (RI), Data Carrier Detect (DCD) and Data Terminal Ready (DTR) can be implemented using GPIO 1,2,3 respectively by connecting the signals to a level shifter before interfacing with RS-232.

Do note that DCD and DTR can be set via AT-commands AT&C and AT&D respectively.

For additional information, refer to PCB Design Guideline in clause 5.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.1.8. PCM Interface

PCM is digital representation of digital signal. There are 4 traces available. Please refer to the table below.

These traces have been configured to support GSM DAI, with the capability to synchronize DAI with the voice frame signal.

Refer to Audio Guideline of the PCB Design guide in clause 5.

Description	Pin	Default Configuration	Alternate Function
GPIO5	34	I	MTXD
GPIO6	32	I	MRXD
GPIO7	28	I	MCLK
GPIO8	33	I	MFSYNCH

2.2. Analogue IO Implementation

2.2.1. Battery Charging Interface

The main function of the Battery Charging Interface ("BCI") is to control the charging of Lithium-Ion/Lithium-Polymer batteries.

The BCI can also perform battery pre-charging and backup battery charging.

The charging scheme for Lithium batteries is constant current first follow by constant voltage charging once a certain threshold voltage is reached (4.2V typical).

Another scheme is applied when the battery charger is connected to a switched off module: a charging current is supply to the battery if the battery voltage is less than 3.6V. If the battery is lower than 3.2V (battery partially discharge or fully discharge), the module will not start until the battery get sufficiently recharged to greater than 3.2V by hardware pre-charging.

When this happens, fast charging begins.

4 signal traces are required for battery charging interface.

Battery charging current is sensed by the 200 milli-ohm external resistor, which is connected across VCCS and VBAT.

BCI- Pin Description:

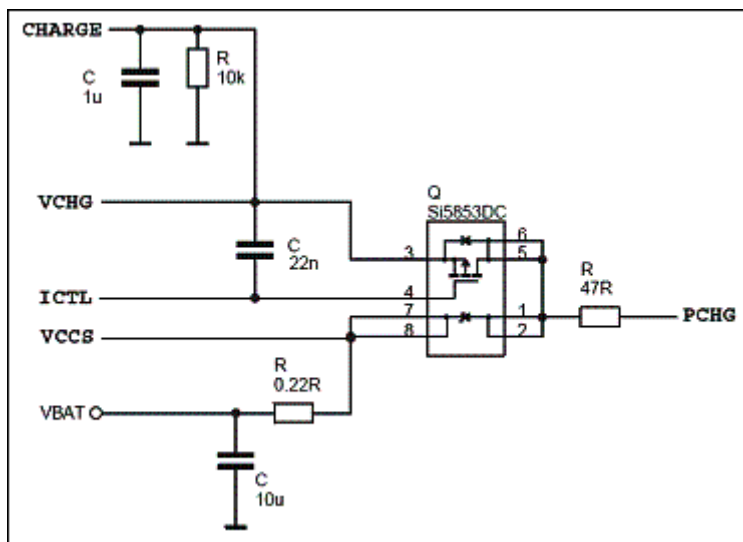| Pin	Description	Default Configuration	I/O
14	PCHG	Battery Pre-charge output Current	O
15	VCHG	Charger Voltage Output	I
16	ICTL	Charger External Transistor Control	O
17	VCCS	Charging Current Sense	I

Figure 5: Battery Charging Interface

Refer to clause 5.3 Power Supply Guideline for power recommendations.

Refer to product technical specifications for Battery Charging Interface for maximum and minimum voltage ratings.

2.2.2. PWON and RESET Interface

The PWON or RESET functions are debounced by hardware. At any point of time, only one can be pressed. PWON pin is used as an ON/OFF control. An interrupt will be triggered in the module at the falling edge of this pin.

Switch-ON Condition
To switch on the module, the module must first be in OFF state. The debounce time at which the signal will remain low is approximately 30ms.

When using batteries, a charging voltage is detected at VCHG pin. The voltage must be above VBAT+0.4 V for the switch-ON to occur. This switch-ON condition is only possible with the Battery Charging Interface.

There are 2 cases when these conditions do not start the sequence:
- When the main battery is below 3.2V.
- When the system is in backup mode (Power is supplied by backup battery).

Switch-OFF Condition
To switch off the module, the module must first be in ON state. The debounced time at which the signal will remain low is approximately 900ms. The PWON signal must be released back to high after the module is switched off.

The PWON pin is active low and the typical application can be seen in the schematic together with the RESET. Additional capacitors can be placed close to these pins for ESD shielding.
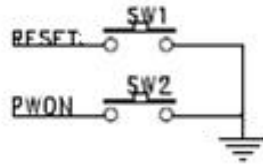

Figure 6: Power On Pins

Pin Description:

Signal	Pin Number	Type	Description
PWON	18	Input	Module switch ON/OFF

Reset Signal

The RESET pin is internally pulled up. When this is pulled down, there will be an unconditional reset to the module. This pin can be left unconnected if not used. To improve ESD shielding, a capacitor of about 15nF can be placed close to the pin.

Pin Description:

Signal	Pin Number	Type	Description
RESET	21	Input	Module reset input. Test only.

Refer to Clause 5 PCB Design Guideline.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.2.3. VIO Interface

A voltage regulator provides the power supply to peripherals, generating a regulated 2.8V from the module. Rated output current is maximum 100mA.

In addition, this VIO pin also supplies to peripherals inside the module. It is advisable to place an external capacitor of 10uF near this pin.

Refer to Clause 5 PCB Design Guideline.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.2.4. VBACKUP Interface

Backup battery connected on VBACKUP should not exceed 3.6V. It is advisable to place an external capacitor near to the pin.
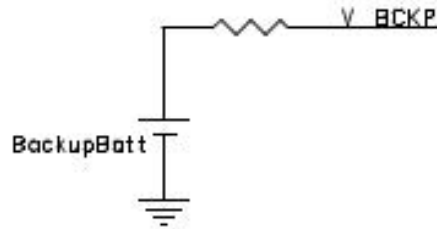

Figure 7: Voltage Backup connection

Refer to Clause 5 PCB Design Guideline.

Refer to product technical specifications for maximum and minimum voltage ratings.

2.2.5. ADC

Read only registers ADC consist of a 10-bit monitoring analog-to-digital converter for both ADIN1 and ADIN2.

Note: Ensure that voltages at these pins are safely scaled down by resistive dividers to fit into the dynamic range of the ADC.

Parameter	Test Conditions	Min	Typ	Max	Units
Resolution			10		Bit
MADC voltage reference			1.75		V
Input leakage current ADINx				1	µA
Differential nonlinearity	Input range 0 to 1.75V	-2		2	LSB
Integral nonlinearity	Best fitting, input range 0 to 1.5V	-1		1	LSB
	Best fitting, input range 1.5V to 1.75V	-3		3	LSB

ADIN1 is for monitoring ADC input 1 and battery type current source.
(Min is 8µA and max is 12µA). Default is set at 10µA.

ADIN2 is for monitoring ADC input 2 and battery temperature current source.
There are 8 selectable possible ranges, which are programmable.
The default is set at 30µA (i.e. Code=2)

Code R(IBIAS) = 100kohm, ADIN2 = 1V	Min Current	Max Current	Unit
0	8	12	
1	16	24	
2	26	34	
3	36	44	
4	46	54	µA
5	55.5	64.5	
6	65.5	74.5	
7	75	85	

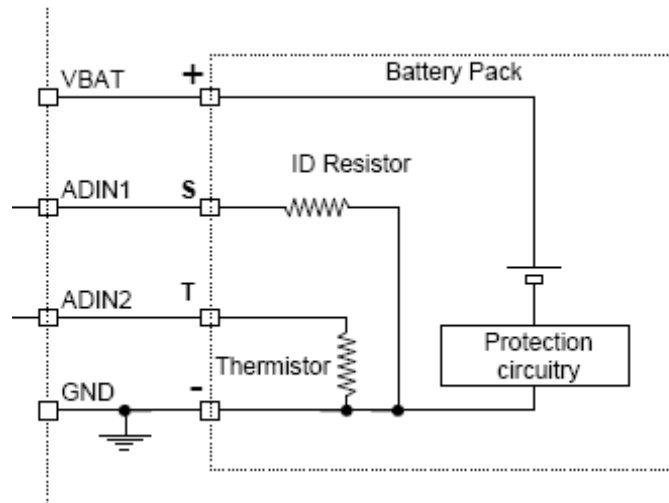Figure 8 below shows how a battery pack can be connected with the monitoring ADC pins.

Figure 8: ADC connections to Battery Pack

3. RF DESIGN

3.1. Antenna Characteristic: Recommended Antenna Specifications

There is no recommended antenna as this is subjective to usage. It is dependent on applications as in what frequency band(s) provided by the network operator.

Please note that the antenna loss will affect the sensitivity of the module at very low signal as well as the current consumption.

Placement Recommendations:
- The antenna should be placed in an area away from any interference.
- In a harsh environment, antenna with high gain is preferred such as Amphenol. http://www.amphenol-saa.com/

The following specifications of a high gain antenna can be used as a reference.

Frequency Range	VSWR	Polarization	Impedance	Gain
890-960 /1710-1880 MHz	≤2	Vertical	50Ω	>5dBi

3.2. Antenna Implementation: Electrical Design Guide Line for RF

The module has three (3) methods of RF interface (Please refer to product technical specifications for more information).

3.2.1. Coaxial Receptacle

The recommended method that is most reliable is to connect through a coaxial receptacle. Harwin's UMC series connector has been chosen for this receptacle and its reference part number is **UMCR-2250005R**.

Figure 9 shows how to connect the RF cable to the Coaxial Receptacle on the module.

3.2.2. RF pad

If antenna RF pad is preferred, ensure there is minimum exposure for the conducting RF cable. It is critical to ensure excellent ground connection with the braid to ensure proper shielding of the RF cable.

Figure 10 & 11 shows the RF pad and ground positions on the module.

Figure 12 shows the recommended RF cable soldering dimensions.

Note: During manual soldering process, it is critical to ensure that high temperature soldering do not melt away the insulator covering the conductor.
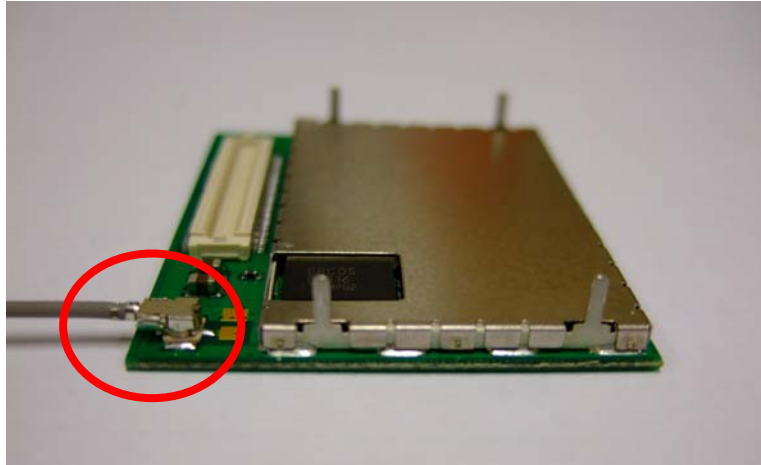
Figure 9: Coaxial Receptacle connection to RF antenna
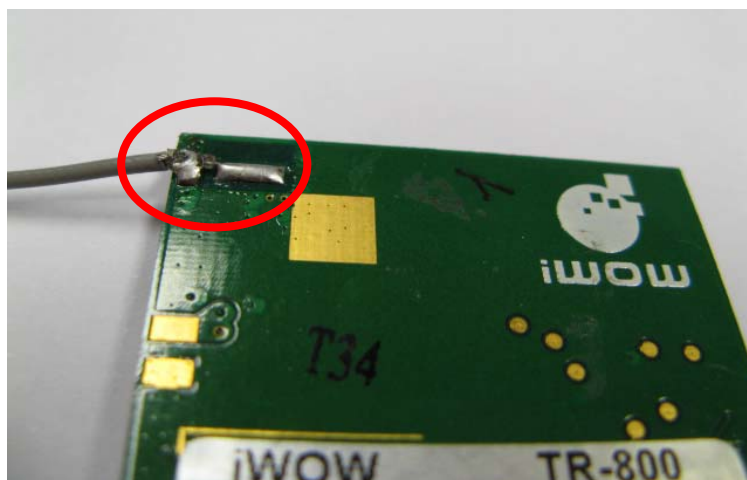

Figure 10: RF and Ground pad on TR-800

Figure 11: Connection of Antenna to RF pad

Below is a reference of how an RF cable with the recommended dimensions of exposed shielding, dielectric core as well as the center conductor to be soldered onto the RF pad.
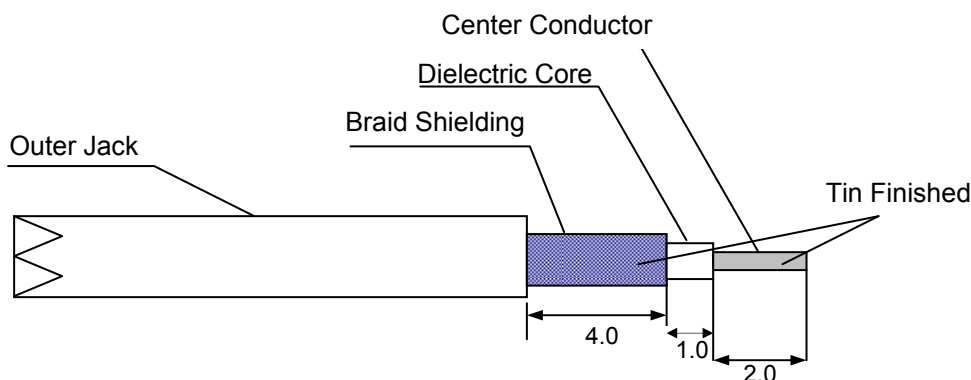

Figure 12: RF cable recommended soldering dimensions

RF Cable Dimensions:

Item		Unit	Specified Value
Inner Conductor	Material	-	Silver coated annealed copper wire
	Stranding	No./mm	7/0.08
	Dia. (approx.)		0.24
Dieelectric Core	Material	-	FEP
	Thick. (nom.)	mm	0.22
	Dia.	mm	0.68±0.05
	Color	-	Natural
Outer Conductor	Material	-	Silver coated annealed copper wire
	Type	-	Braid (16/4/0.05)
	Dia. (approx.)	mm	0.93
Jacket	Material	-	FEP
	Thick. (nom.)	mm	0.10
	Dia.	mm	0.13 +0.10 / -0.06
	Color	-	Standard colors are white, black, blue, brown and gray

There are several types of RF cables available from single shielding to double shielding. Depending on different applications requirements, standard RF cables for example, RG-213, RG-174 or RG-58 can be used.

Design Considerations:
1. Ensure that the RF cable is ground cleanly otherwise the cable will radiate noise.
   ▪ To minimize this, the connections between the ground plane and the RF cable shield should have as low inductance as possible.
   ▪ The shield grounding should be shortened to minimum length possible and soldered directly to the dedicated exposed ground plane on the module.
2. Design the shortest possible path from antenna to feed.
3. Avoid routing RF cables under the module, above the module and near noisy circuitries.
4. Ensure that the feedline is 50 Ohm characteristic impedance. Matching circuit is desired, as this will ensure proper matching.
5. Ensure a good ground plane around the feedline.

It is also important to consider where the final product will be placed or used, as such additional steps can be taken to ensure that the module will be properly shielded in an area full of EMI.

4. MECHANICAL SPECIFICATIONS

Figure 13 below shows the overall dimension of TR-800 GSM/GPRS module.

Do take attention to the following
- The Antenna cable connection at RF pad or RF receptacle in terms of bending, length and position
- Legs of module to be soldered firmly to ground plane

Note: For the insertion of module ground legs onto PCB Board, the spacer is recommended to be 4mm in diameter.
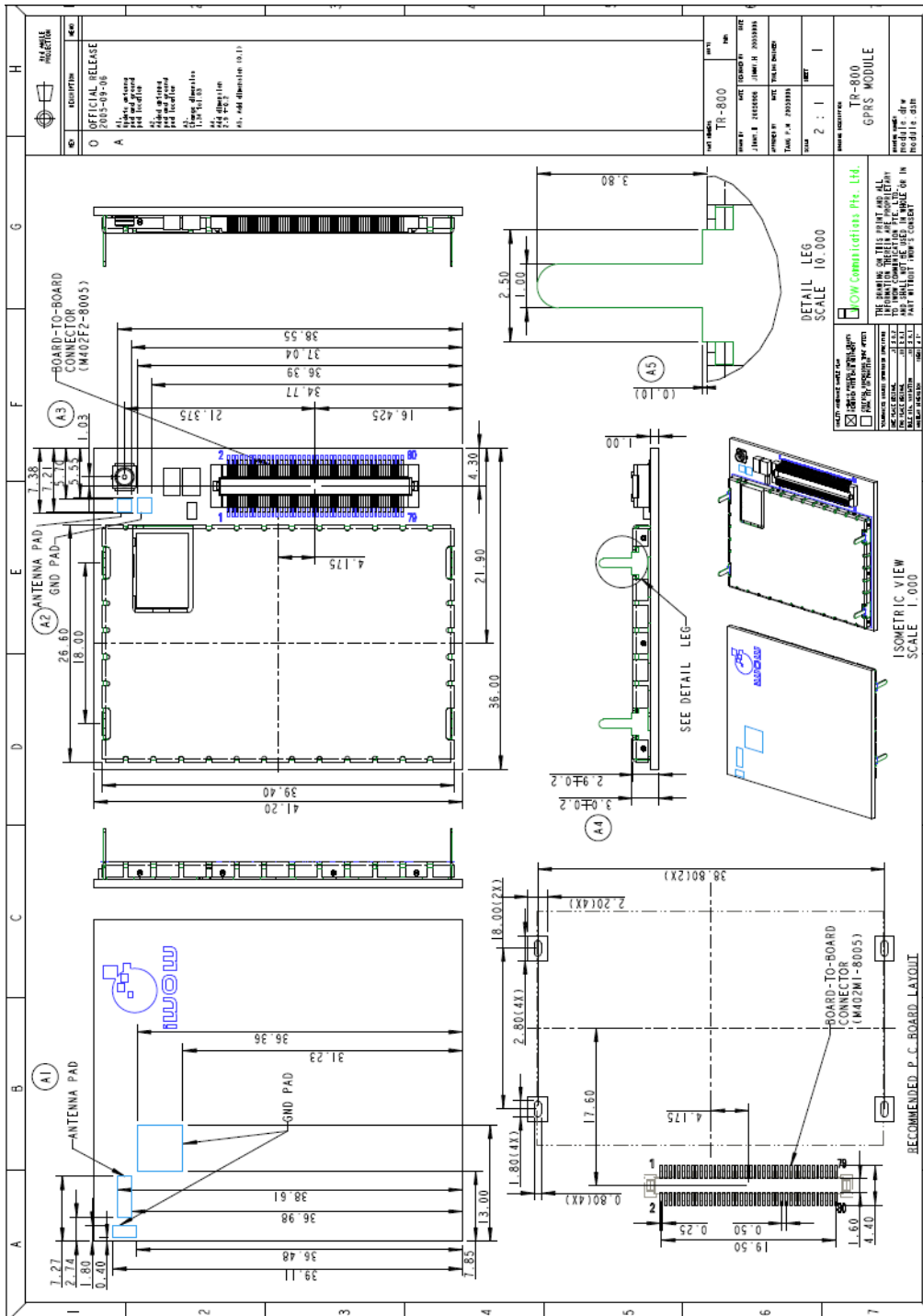

Figure 13

5. PCB DESIGN

5.1. General Guide

Ensure the RF signals are routed with 50 ohm characteristic impedance. Calculation have to be carried out to ensure that thickness of the trace is 50 ohm impedance and ensure impedance control for RF trace during PCB manufacturing if necessary.

The choice of stripline or microstrip is dependent on the designer.

Ensure the RF traces are isolated from noisy signals (digital, bus, supply).

*Note: Ensure that all **unused pins** of the module are shorted to GND. (i.e. RTS, CTS, DSR etc.)*

5.2. General Layout Guideline

- It is advisable to use a 4 layer PCB with minimum 1 layer of uniform ground plane as this will help to eliminate any ESD or EMC interferences.

- Stack-ups should also be planned carefully to ensure proper shielding of critical traces. (Decision should be made on the number of signals layers and plane such as power, ground, analogue, digital and RF).

- Good PCB layout comes with good placement of components. EMI is usually caused by poor PCB layout.

- Identify all the critical parts of the components before layout. After which, routing of the traces will be neater and less susceptible to interference.

- The mechanical portion of the TR-800 GSM/GPRS module should be soldered onto the main ground.

- All ground should be continuous. This provides better grounding and return path. Good ground plane also helps in heat removal and provide good shielding.

- Ensure all ground planes are connected with multiple vias to avoid creating ground loop. This will reduce the trace impedance to ground.

- All ground planes should have low impedances connections.

- If the module is connected to a daughter board, ensure that the daughter board is properly grounded to the motherboard or chassis. Do not only rely on 1 or 2 ground pins in the connectors for the grounding.

- Ensure the power supply lines to the pin connectors can sufficiently deliver the required current to the module.

- Design the pin connectors with proper isolation between the RF signals and noisy traces.

- Analogue and digital ground should be separated to prevent noise coming from digital ground thus contaminating the analogue performance. A common ground point needs to be placed correctly to allow all grounds to meet at a common junction, which can minimize any circulating of currents and noise.

- Remove unnecessary unconnected copper fills.

- Avoid unnecessary traces, as this will build up stray capacitances or inductance in the design.

- It is important to take note of the vias used, as it can also become unnecessary capacitances.

- Do not route any traces under the module. A ground plane is preferred underneath the module to provide optimum shielding.

- Use shortest possible traces whenever it is possible. Avoid long and thin loop traces, as this will form an unwanted antenna.

- Use striplines for signal traces.

- Ensure that there are no sharp corners (90degree traces) as shown in figure 14. Use 45 degree turn instead.

45 DEGREES

(a) Incorrect   (b) Correct

Figure 14

- When routing near sensitive circuitries, use ground guard or fills whenever possible.

- Avoid running digital traces close to analog traces. Avoid parallel runs with sensitive traces.

- When analog switches are used in audio/data traces, ensure selection of low-on resistance and small $R_\triangle$.

- Ground for decoupling capacitor should be short and close to main ground.

- If radiated problem still occurs, conduct first layer troubleshooting with a set of tweezers to identify the problem areas.

5.3. Power Supply Guideline

- Do not connect main power input directly to the module. Ensure the filtering components are in place. Add a ferrite bead if necessary.

- A low ESR capacitor, preferably tantalum of > 1mF, is to be placed as close as possible to the module's voltage supply input. Other filtering capacitors should also be placed nearby if necessary.

- It may be necessary to place additional 33pF close to the module when there are RF interferences.

- Power supply must be able to deliver high current because of the GSM/GPRS burst emission. To achieve that, the traces must be sufficiently wide enough to support the current peak. It is

recommended that pins 1,2,3,4 and 5 should all be routed into one big copper trace as the power supply line as shown below.
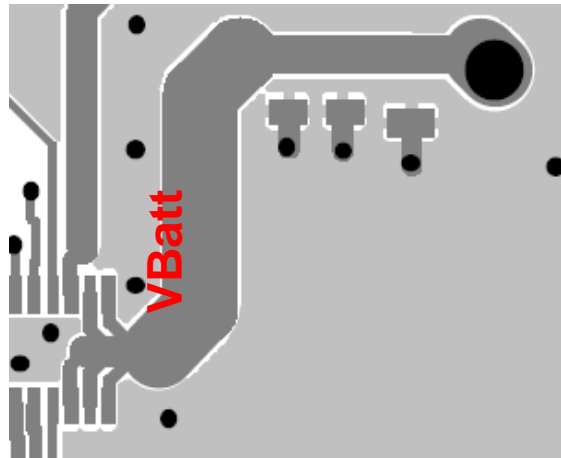

Figure 15

- If voltage drop during peak current is high, an audible 217Hz will be heard through the audio jack during calls. This is known as TDMA noise.

In worst-case scenario, when voltage drops to below the minimum voltage rating, the module may shut down.

- Typical voltage drop should be less than 200mV with good PCB layout.

During GPRS connection, GSM/GPRS Class 2 (2RX/1TX) takes up only 1 uplink slot out of 8 slots, while a Class 10 (3RX/2TX) takes up 2 uplink slots out of 8 slots.

Thus the module may have to transmit at maximum current for approximately 577us every 4.615ms for 1 uplink and, the Power Amplifier will transmit at maximum current for 1154us every 4.615ms for 2 uplinks.

- According to electrical and GSM specifications, the power supply must be able to handle high peak currents (2A in EGSM) burst in a short time.

As such, it is important to ensure minimum voltage drop as this may compromise the module's performance.
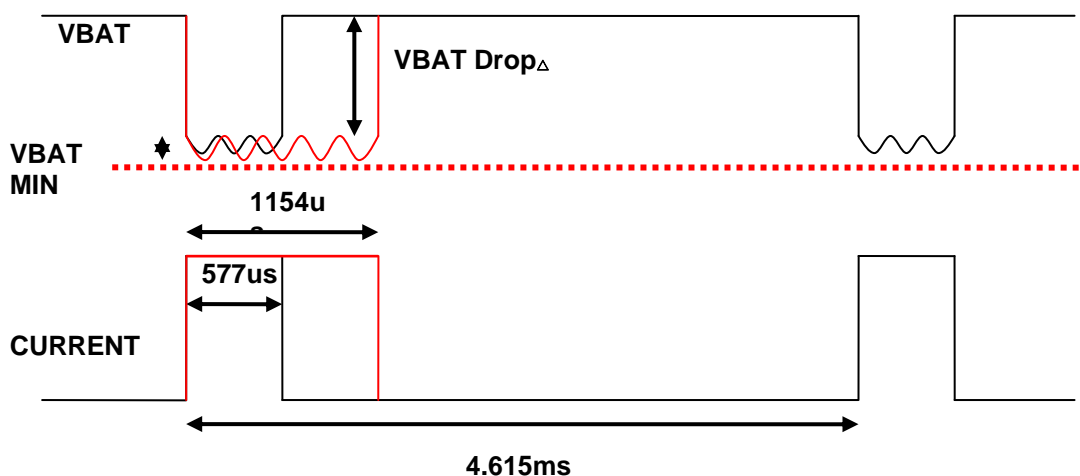

Figure 16: GPRS Voltage drop and Burst Current Duration

Power Supply Voltage:

Parameters	Min	Nom	Max	Unit
VBAT	3.4*	3.8	5.5	V

Must be guaranteed to ensure compliance with the GSM certification requirements.

- If no audio circuitries are required, typical voltage drop can be higher as long as it meets the minimum voltage rating.

- A good ground plane should be placed closed to power trace.

- Use multiple vias to ensure good grounding on a multiple layer PCB board.

- Use big vias size to connect between layers so as to reduce the impedances of the trace.

- Improper layout and vias usage will result in high impedance and thus power loss could occur.

5.4. Audio Guideline

The unwanted interference on the audio (commonly referred as "TDMA noise"), may be picked up from the earpiece due to interference. The other possible interferences are on the microphones and speakers. Typical suppression techniques include the use of capacitors.

- TDMA noise at GSM900 can be suppressed with a 33Pf capacitor across the microphone or with one end to ground.

- For TDMA noise occurring at 1800, capacitor value of 12Pf can be added at the same position. The capacitors can also be connected to the earphone traces with one side shorted to ground.

2 different audio inputs and outputs are available on the module for hand free operations.

Pin	Name	Description	Function
19	AUXI	Auxiliary Speech Input	INPUT
25	AUXOP	Auxiliary Speech Output (+ve)	Z
27	AUXON	Auxiliary Speech Output (-ve)	Z
20	MICIN	Microphone Amplifier Input (-ve)	INPUT
22	MICIP	Microphone Amplifier Input (+ve)	INPUT
23	MICBIAS	Microphone Bias Supply	Z
24	EARP	Earphone Amplifier Output (+ve)	Z
26	EARN	Earphone Amplifier Output (-ve)	Z

- Ensure the frequency response for microphone and speakers are compatible with GSM specifications.

- Traces should be symmetrical. Route these traces, shielded and close to a ground plane.

- Audio circuitries should be placed close to the headset jack.

- Audio lines should be kept away from noisy traces such as power supply traces.

- Biasing should be done according to the microphone specifications, which can be obtained from microphone manufacturer. MIC biasing voltage is selectable via AT-command +MICB which represents the values in the table below

MIC BIAS Voltage:

$I_{MICBIAS}$ = 0 – 2 Ma	Min Voltage	Max Voltage	Unit
MICBIAS BIT = 0	1.9	2.1	V
MICBIAS BIT = 1	2.4	2.6	

The block diagram in Figure 17 shows the audios traces going in and out of the voice band codec.

The voice band codec includes an input amplifier for microphone as well as an output amplifier for speaker. It can perform programmable gain (+ATXG, +ARXG), volume control (+ARXV) and side-tone (+ASTN) functions. It can be set by using the respective AT-Commands.
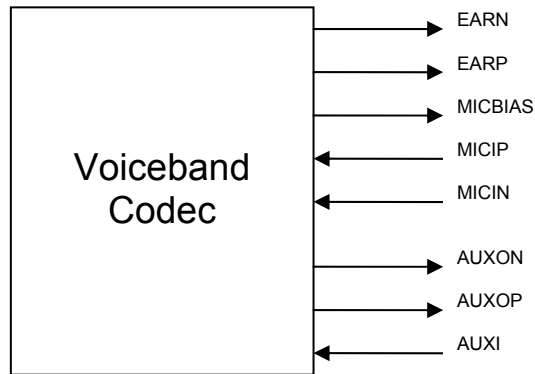
Figure 17: Block Diagram of audio connection

Connections can be either single ended or differential.

The differential connection is recommended for better rejection of TDMA noises.

If single ended connection is preferred, ensure good filtering circuits on both sides and good shielding of the traces.

Ensuring the proper placement of the audio jack and filtering circuitries is most importance.

Please refer to the respective recommended audio circuitries in the following few pages.

Single Ended Connection

Earphone

Micro-amplifier gain (MICIP-MICIN) is 25.6dB. Earphone output amplifier provides a differential signal on EARN and EARP.

Capacitors should be placed near to the earpiece and the pins.
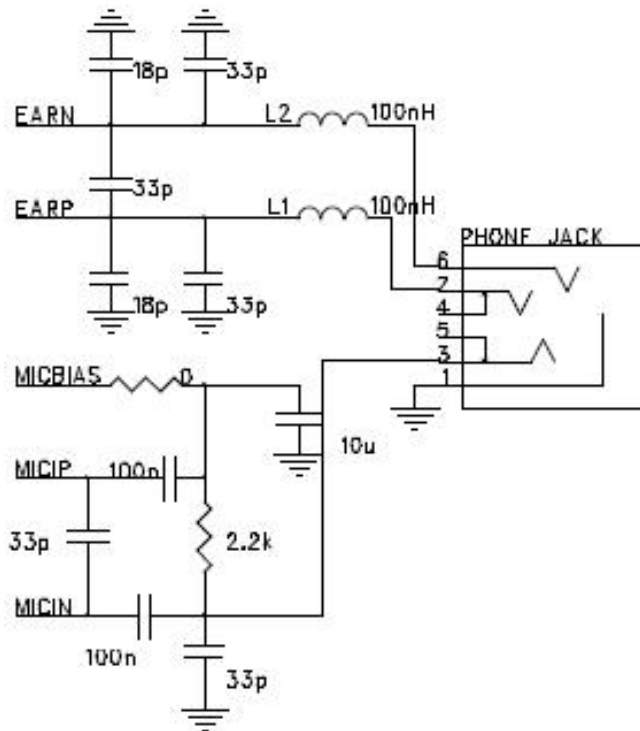
Figure 18: Single Ended Circuit Connection for Earphone

Auxiliary Output

Auxiliary output amplifier provides a differential signal on AUXON and AUXOP.
The capacitors should be placed near to the auxiliary outputs as well as near to the pins. Auxiliary input resistance (AUXI) is typically 160K ohm. Auxiliary gain amplifier (AUXI) is selectable between 4.6dB and 28.2dB.
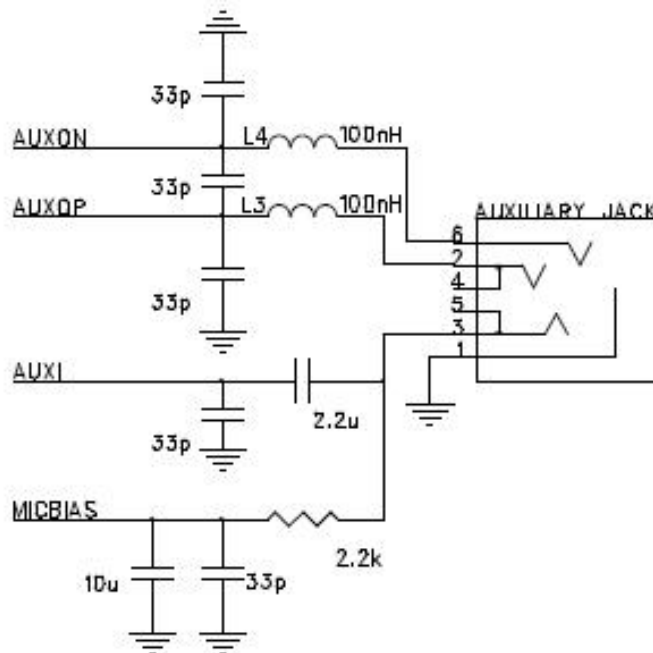
Figure 19: Single Ended Circuit Connection for Auxiliary Out

Differential Connection

Differential input resistance (MICIP-MICIN) is 36K ohm. The capacitors should be placed near to the mic inputs as well as near to the pins.
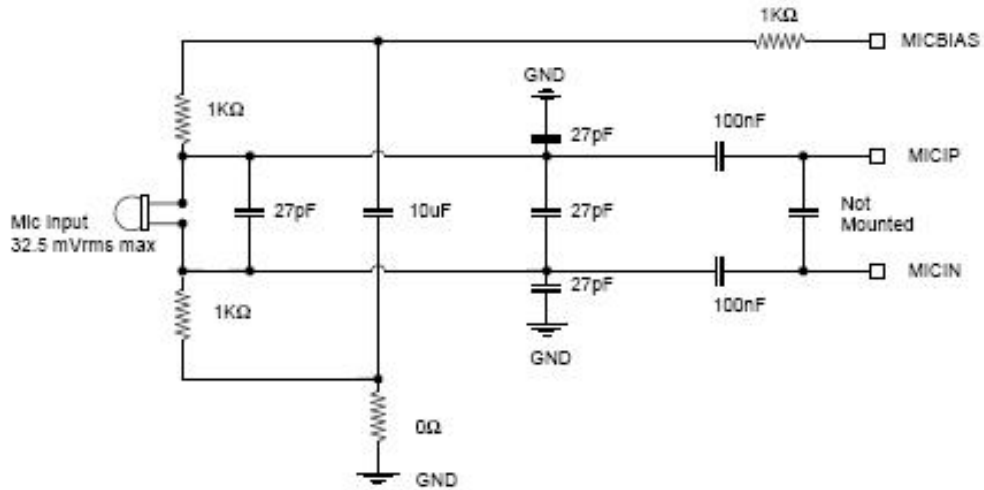
Figure 20: MIC input Differential Circuit

6. VERIFICATIONS OF MODULE'S PERFORMANCE

To check the module for compliancy to standards and specifications, it is advisable to have a proper shield box to conduct the test as the shield box will help to eliminate interferences.

The test should be carried using good quality conducted RF cables connected between the module and the test equipment.

The test is best carried out using a standard TR-800 Development Starter Kit ("DSK") with connections as shown in Fig 21.

Typical test equipments available in the market are Rohde & Schwarz's CMU200 and Agilent's 8960. A test SIM card from ORCA will be necessary to register onto the test network of the test equipment.
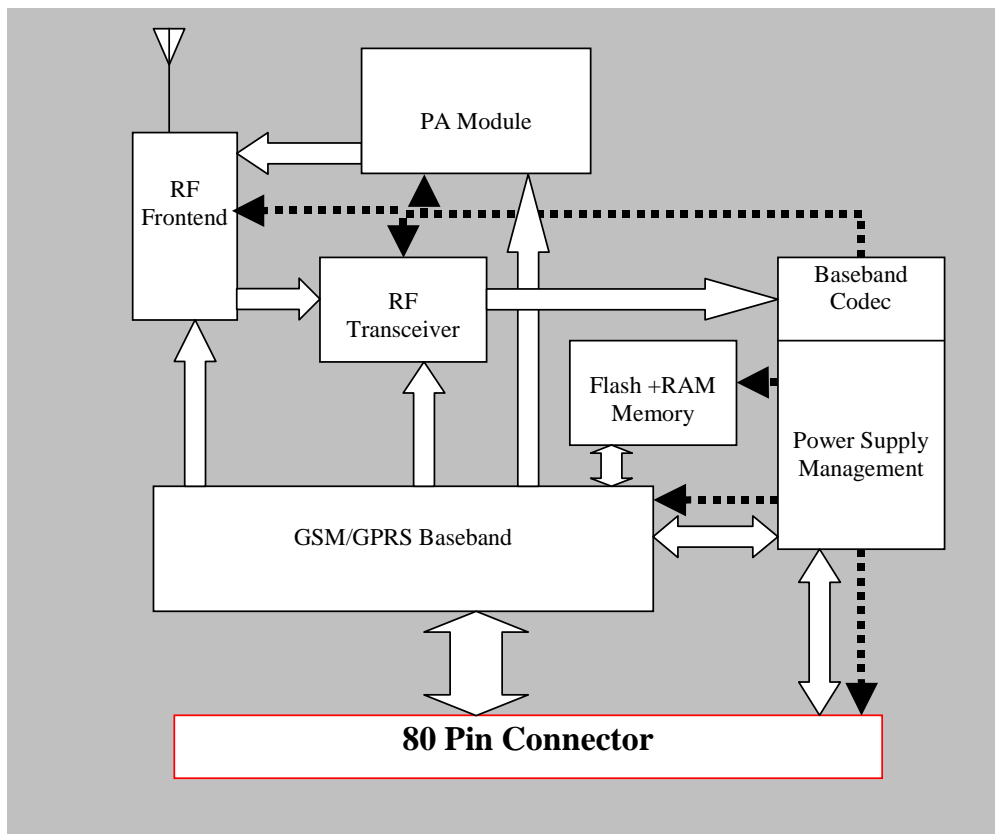
Figure 21: Block Diagram of TR-800 GSM/GPRS Module

7. PART REFERENCES AND SUPPLIERS

The following part references and suppliers are suitable for use with the TR-800 GSM/GPRS modules.

7.1. General Purpose Connector

The General Purpose Connector is an 80 pin connector with 0.5mm pitch from Harwin having the reference number:
M402F2-8005

The mating connectors reference:
M402M1-8005

The stacking height is 2.0mm

Please refer to General Purpose Connector datasheet at Appendix for further details.

For more information on the Connectors, please visit http://www.harwin.com.

7.2. SIM Card Reader

- Cannon ITT CCM03-3503 (http://ittcannon.com)

7.3. Audio Headset Jack

- Hosiden (http://www.hosiden.com)

7.4. RF cable

The following cable references can be used on TR-800 GSM/GPRS module

Harwin
- UMCA-XXX-SMA
- UMCA-XXXXX1-035
- UMCA-XXXXX-000

7.5. RF receptacle

- Harwin SMT UMCR-2250005R

7.6. DC Jack

Possible Supplier
- Hosiden

APPENDIX A : TR-800 80-PIN CONFIGURATION

Pin	Name	I/O	Description	Reset
1	VBAT	I	Battery input	Input
2	VBAT	I	Battery input	Input
3	VBAT	I	Battery input	Input
4	VBAT	I	Battery input	Input
5	VBAT	I	Battery input	Input
6	VBACKUP	I	Backup battery/supply input	Input
7	ADIN1	I	ADC input 1 (Battery type)	Input
8	ADIN2	I	ADC input 2 (Battery temperature)	Input
9	VIO	O	Digital supply output	N/A
10	SIMIO	I/O	SIM data input/output	0
11	VSIM	O	SIM voltage supply	N/A
12	SIMCLK	O	SIM clock	0
13	SIMRST	O	SIM reset	0
14	PCHG	O	Battery pre-charge output current	
15	VCHG	I	Charger voltage input	Input
16	ICTL	O	Charger external transistor control	
17	VCCS	I	Charging current sense	Input
18	PWON	I	On button input	Input
19	AUXI	I	Auxiliary speech signal input	Input
20	MICIN	I	Microphone amplifier input (-ve)	Input
21	RESET	I	Reset input (Test mode only)	Input
22	MICIP	I	Microphone amplifier input (+ve)	Input
23	MICBIAS	O	Microphone bias supply	
24	EARP	O	Earphone amplifier output (+ve)	Z
25	AUXOP	O	Auxiliary speech signal output (+ve)	Z
26	EARN	O	Earphone amplifier output (-ve)	Z
27	AUXON	O	Auxiliary speech signal output (-ve)	Z
28	MCLK or GPIO7	I/O I/O	Bit synchronization clock. *Alt. function: GPIO7*	Input
29	GPIO1	I/O	General purpose IO	Input
30	GPIO2	I/O	General purpose IO	Input
31	GPIO3	I/O	General purpose IO	Input
32	M_RXD or GPIO6	I I/O	Receive serial data. *Alt. function: GPIO6*	Input
33	M_FSYNCH or GPIO8	I/O I/O	Frame synchronization clock or SS reset. *Alt. function: GPIO8*	Input
34	M_TXD or GPIO5	O I/O	Transmit serial data. *Alt. function: GPIO5*	Input
35	RESETOUT or GPIO4	O I/O	Reset output. *Alt. function: GPIO4*	Input
36	KBC0	O	Keypad column 0	1
37	KBC1	O	Keypad column 1	1
38	KBC2	O	Keypad column 2	1
39	KBC3	O	Keypad column 3	1
40	KBC4	O	Keypad column 4	1
41	KBR0	I	Keypad row 0 (Interrupt input)	Input
42	KBR1	I	Keypad row 1 (Interrupt input)	Input
43	KBR2	I	Keypad row 2 (Interrupt input)	Input
44	KBR3	I	Keypad row 3 (Interrupt input)	Input
45	KBR4	I	Keypad row 4 (Interrupt input)	Input
46	SDI_SDA	I/O	I2C bi-directional data	Z
47	SCS0_SCL	O	I2C master serial clock	Z

Pin	Name	I/O	Description	Reset
48	GND	I	Ground	N/A
49	TXD2	I	Serial port 2 – Receive data (Active low)	Input
50	RXD2	O	Serial port 2 – Transmit data (Active low)	1
51	TXD	I	Serial port 1 – Receive data (Active low)	Input
52	RXD	O	Serial port 1 – Transmit data (Active low)	1
53	CTS	O	Serial port 1 – Clear to send (Active low)	1
54	RTS	I	Serial port 1 – Ready to send (Active low)	Input
55	LPG	O	Blinking LED signal output.	1
56	CLK13M	O	13MHz output clock	0
57	A1	O	Address bus	0
58	A2	O	Address bus	0
59	A3	O	Address bus	0
60	A4	O	Address bus	0
61	/RD	I/O	Read cycle from peripheral signal (Active low)	1
62	/WR	I/O	Write cycle to peripheral signal (Active low)	1
63	/CS2	O	Chip select 2 (active low)	1
64	/CS3	O	Chip select 3 (active low)	1
65	D0	I/O	Data bus	Output
66	D1	I/O	Data bus	Output
67	D2	I/O	Data bus	Output
68	D3	I/O	Data bus	Output
69	D4	I/O	Data bus	Output
70	D5	I/O	Data bus	Output
71	D6	I/O	Data bus	Output
72	D7	I/O	Data bus	Output
73	D8	I/O	Data bus	Output
74	D9	I/O	Data bus	Output
75	D10	I/O	Data bus	Output
76	D11	I/O	Data bus	Output
77	D12	I/O	Data bus	Output
78	D13	I/O	Data bus	Output
79	D14	I/O	Data bus	Output
80	D15	I/O	Data bus	Output

Note:
The reset values are defined as follows:
0: Driven low (output)
1: Driven high (output)
Z: High impedance (output disabled)
N/A: Not applicable

APPENDIX B: ELECTRICAL CHARACTERISTIC

Parameter	Description	Min	Nom	Max	Unit
Supply Input:					
VBAT	Battery Input Voltage	3.40	3.80	5.50	V
I_{BURST}	Burst peak current	-	-	2.0	A
Regulated Output:					
VIO	Internal regulated output voltage	2.70	2.80	2.90	V
I_{OUT}	Rated output current	-	-	100	mA
SIM Card Related:					
VSIM	Output voltage to 3V SIM card	2.75	2.85	3.00	V
I_{SIM}	Rated output current	-	-	10	mA
V_{OL}	SIMIO low level voltage, I_{OL} = 1mA	-	-	0.4	V
V_{OL}	SIMCLK low level voltage, I_{OL} = 20µA	-	-	0.2VSIM	V
V_{OH}	SIMCLK high level voltage, I_{OH} = 20µA	0.7VSIM	-	-	V
V_{OL}	SIMRST low level voltage, I_{OL}= 20µA	-	-	0.2VSIM	V
V_{OH}	SIMRST high level voltage, I_{OH} = 20µA	0.7VSIM	-	-	V
ON/OFF Switch:					
V_{IH}	High level input voltage	0.7VBAT	-	-	V
V_{IL}	Low level input voltage	-	-	0.3VBAT	V
Digital Signal Characteristic (GPIO,UART,LPG,Keyboard):					
V_{IH}	High-level input voltage	0.7VIO	-	VIO+0.5	V
V_{IL}	Low-level input voltage	-0.5	-	0.3VIO	V
V_{OH}	High-level output voltage at rated current	0.8VIO	-	-	V
V_{OL}	Low-level output voltage at rated current	-	-	0.22VIO	V
I_{OH}	Rated output high current	-	-	1	mA
I_{OL}	Rated output low current	-	-	1	mA

Note:
Due to the burst emission in GSM, the power supply (VBAT) must be able to handle high current peaks (2A max in EGSM band) in a short time. For a GPRS Class 2 device, the module emits a 577us radio burst every 4.615ms during communication. For a GPRS Class 10 device, the module emits two of these 577us bursts within the 4.615ms frame during communication.