AERO® II TRANSCEIVER FOR GSM AND GPRS WIRELESS COMMUNICATIONS

Features

- 5x5 mm 32-pin QFN
- Smallest solution footprint
- Highest integration
- Industry-leading performance
- Integrated GSM/GPRS transceiver including the following:
  - Digital low-IF receiver
    - Quad-band LNAs
    - Region management flexibility
  - Offset PLL transmitter
    - Integrated TX VCO, loop filter, and varactor
  - Frequency synthesizer
    - Integrated RF VCO, loop filter, and varactor
- Digitally-controlled crystal oscillator (DCXO)
- Universal analog baseband interface
- Quad-band support:
  - GSM 850 Class 4, small MS
  - E-GSM 900 Class 4, small MS
  - DCS 1800 Class 1
  - PCS 1900 Class 1
- GPRS class 12 compliant
- 3-wire serial control interface
- 2.7 to 3.0 V operation
- CMOS process technology
- Lead-free/RoHS-compliant

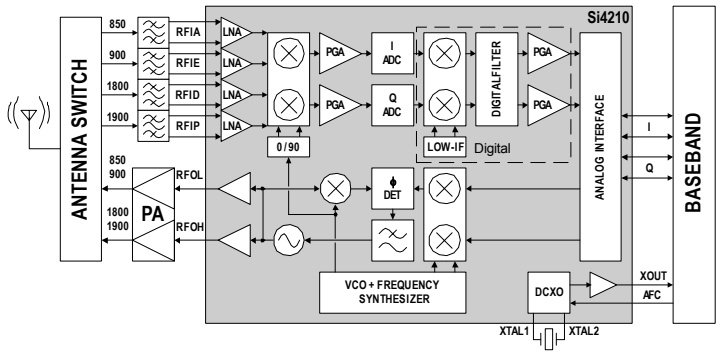
Applications

- Multi-band GSM/GPRS digital cellular handsets
- Multi-band GSM/GPRS wireless data modems

Description

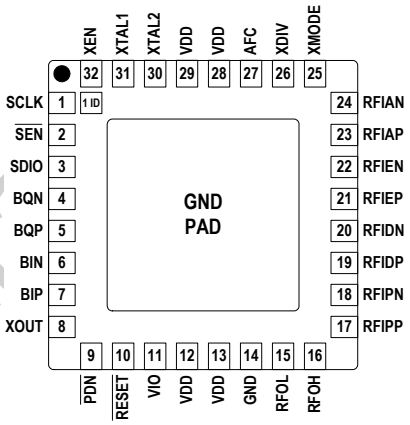
The Aero® II transceiver is a complete RF front end for multi-band GSM and GPRS wireless communications. The receive section interfaces between the RF band-select SAW filters and the baseband subsystem. The Aero II receiver leverages a proven digital low-IF architecture and enables a universal baseband interface without the need for complex dc offset compensation. The transmit section of Aero II provides a complete upconversion path from the baseband subsystem to the power amplifier (PA) using an offset phase-locked loop (OPLL) integrated with Silicon Laboratories' patented synthesizer technology. All sensitive components, such as TX/RF VCOs, loop filters, tuning inductors, and varactors are completely integrated into a single integrated circuit. The Aero II transceiver includes a digitally-controlled crystal oscillator (DCXO) and completely integrates the reference oscillator and varactor functionality.

Functional Block Diagram



Pin Assignments (Top View)

Si4210-GM
(Pin descriptions, see page 27)



Ordering Information: See page 28.

Patents pending

NOTES:

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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
DC Supply Voltage[2]	V_{DD}		2.7	2.85	3.0	V
Baseband I/O Interface Supply Voltage[3]	V_{IO}		2.7	—	3.0	V
Supply Voltages Difference[4]	V_Δ		–0.3	—	0.3	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 2.85 V and an operating temperature of 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
2. V_{DD} should be fed from a 2.85 V nominal regulator with a 150 mA minimum current rating. May require active pull-down regulator, pending on power management option chosen. Please refer to "AN150: Aero II Transceiver PCB Design Guide."
3. V_{IO} may be connected to the phone memory regulator.
4. Supply voltage difference specification applies between V_{DD} pins.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}, V_{IO}		–0.5 to 3.3	V
Input Current[3]	I_{IN}		±10	mA
Input Voltage[3]	V_{IN}		–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}		–40 to 95	°C
Storage Temperature	T_{STG}		–55 to 150	°C
RF Input Level[4]		Receive Mode	5	dBm
		Transmit Mode	10	dBm

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. **The Aero II device is a high-performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of these devices should only be done at ESD-protected workstations.**
3. For pins SCLK, $\overline{\text{SEN}}$, SDIO, $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, XMODE, XDIV, and XEN.
4. At SAW filter output for all bands.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} Supply Current[1]	I_{RX}	Receive mode	—	108	123	mA
	I_{TX}	RFOL Transmit mode	—	125	140	mA
		RFOH Transmit mode	—	120	135	mA
	I_{PDN}	$\overline{PDN}$ = GND, XEN = GND, SDIO = GND	—	10	50	µA
	I_{VDD}	XEN = V_{DD}, f_{XOUT} = 13 MHz	—	4.2	5.4	mA
	I_{VDD}	XEN = V_{DD}, f_{XOUT} = 26 MHz	—	4.8	6	mA
V_{IO} Supply Current[1]	I_{VIO_PDN}	$\overline{PDN}$ = GND, SDIO = GND	—	1	50	µA
High Level Input Voltage[2]	V_{IH}		0.7xV_{IO}	—	V_{DD}+0.3	V
Low Level Input Voltage[2]	V_{IL}		–0.3	—	0.3xV_{IO}	V
High Level Input Current[2]	I_{IH}	V_{IH} = V_{DD} = 3.0 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD} = 3.0 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OUT} = –100 µA	0.8xV_{IO}	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OUT} = 100 µA	—	—	0.2xV_{IO}	V
High Level Output Voltage[4]	V_{OH}	10 pF load on XOUT	0.7xV_{DD}	—	—	V
Low Level Output Voltage[4]	V_{OL}	10 pF load on XOUT	—	—	0.3xV_{DD}	V

Notes:
1. Measured with 10 pF load on XOUT pin and f_{XOUT26} = 26 MHz. Limits with XEN = V_{DD} guaranteed by characterization.
2. For input pins SCLK, $\overline{SEN}$, SDIO, $\overline{PDN}$, $\overline{RESET}$, XMODE, XDIV, and XEN.
3. For output pin SDIO.
4. For output pin XOUT.

Table 4. AC Characteristics

(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Input Pin Capacitance[1,3]			—	—	5	pF
Output Load Capacitance[2,3]			—	—	10	pF
$\overline{\text{RESET}}$ Delay from V_{DD}[3]	t_{RST}		100	—	—	ns
XOUT Rise/Fall Time[3]	t_{XRF}	10 pF load on XOUT	2	—	10	ns
XOUT Hi/Low Time[3]	t_{XHI}, t_{XLO}		9	—	—	ns
SCLK Cycle Time	t_{CLK}		38	—	—	ns
SCLK High/Low Time	t_{HI}, t_{LO}		15	—	—	ns
$\overline{\text{SEN}}$↓ to SCLK↑	t_{FRSEN}		10	—	—	ns
$\overline{\text{SEN}}$↑ from SCLK↑	t_{RRSEN}		12	—	—	ns
SDIO Delay Time from SCLK↓[4]	t_{DSW}	Write	—	—	10	ns
SDIO Setup Time to SCLK↑[4]	t_{SUW}	Write	3	—	—	ns
SDIO Hold Time from SCLK↑[4]	t_{HW}	Write	3	—	—	ns
SDIO Delay from SCLK↓[5]	t_{DSR}	Read	3	—	15	ns
SDIO Setup Time to SCLK↓[5]	t_{SUR}	Read	6	—	—	ns
SDIO Hold Time from SCLK↓[5]	t_{HR}	Read	3	—	—	ns

Notes:
1. For input pins SCLK, $\overline{\text{SEN}}$, SDIO, $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, XMODE, XDIV, and XEN.
2. For output pins SDIO and XOUT.
3. Specifications guaranteed by design.
4. In write mode, SDIO should be clocked into the transceiver on SCLK↑.
5. In read mode, SDIO should be clocked into the baseband on SCLK↓.

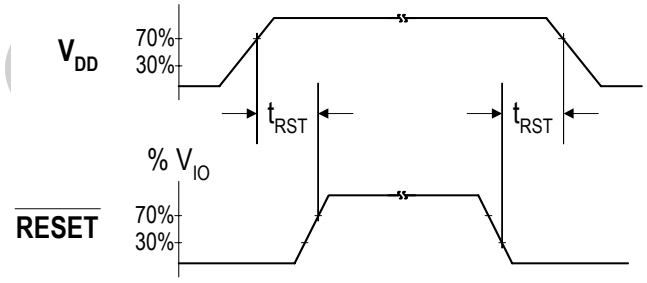


Figure 1. $\overline{\text{RESET}}$ Timing

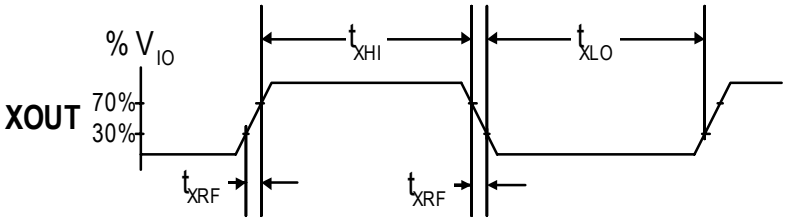


Figure 2. XOUT Timing Parameters

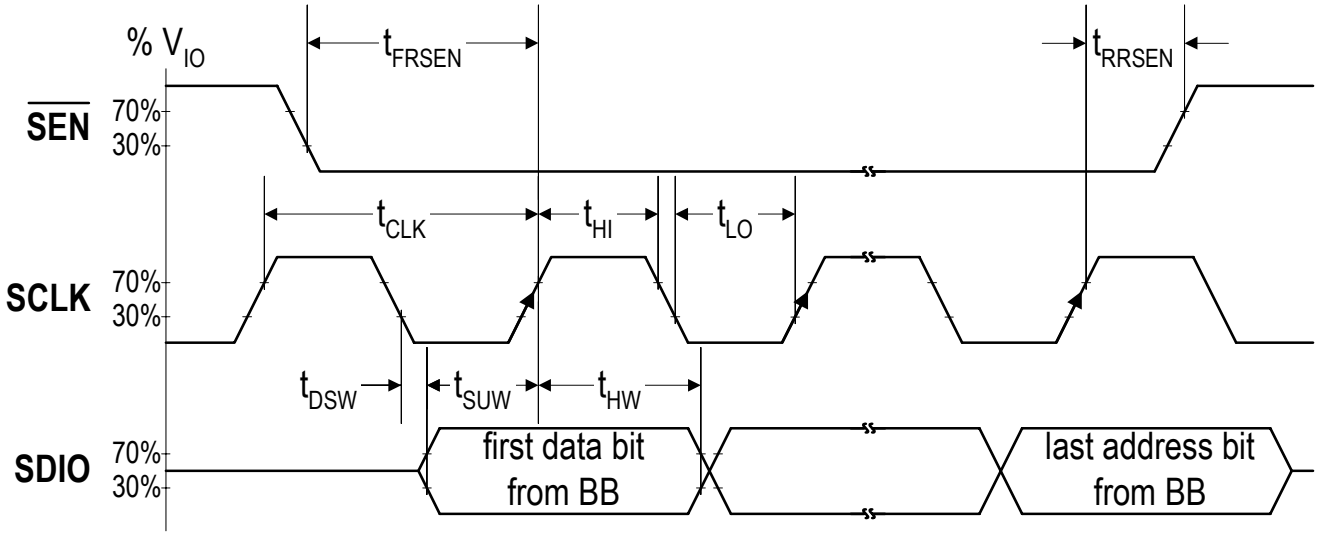


Figure 3. Serial Control Interface Write Timing Parameters

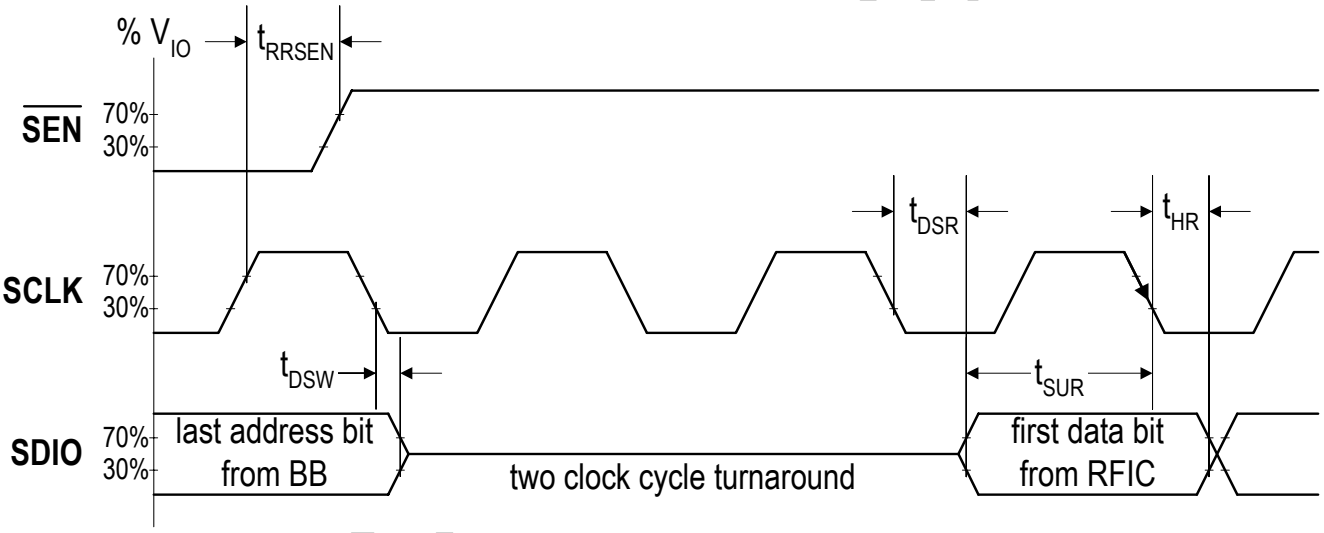


Figure 4. Serial Control Interface Read Timing Parameters

Table 5. Receiver Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency[1]	F_{IN}	GSM 850 band	869	—	894	MHz
		E-GSM 900 band	925	—	960	MHz
		DCS 1800 band	1805	—	1880	MHz
		PCS 1900 band	1930	—	1990	MHz
Noise Figure at 25 °C[2,3]	NF_{25}	GSM 850 band	—	2.1	2.5	dB
		E-GSM 900 band	—	2.3	3.2	dB
		DCS 1800 band	—	2.4	3.0	dB
		PCS 1900 band	—	2.5	3.2	dB
Noise Figure at 85 °C[2,3]	NF_{85}	GSM 850 band	—	2.9	3.2	dB
		E-GSM 900 band	—	3.1	4.0	dB
		DCS 1800 band	—	3.3	4.1	dB
		PCS 1900 band	—	3.5	4.6	dB
3 MHz Input Desensitization[2,3,4]	DES_3	GSM bands	–25	–21	—	dBm
		DCS/PCS bands	–28	–25	—	dBm
20 MHz Input Desensitization[2,3,4]	DES_{20}	GSM bands	–20	–16	—	dBm
		DCS/PCS bands	–17	–15	—	dBm
Input IP2[2]	IP2	$\|f_{1,2} - f_0\| \geq 6$ MHz, $\|f_2 - f_1\| = 200$ kHz	29	40	—	dBm
Input IP3[2]	IP3	$\|f_2 - f_1\| \geq 800$ kHz, $f_0 = 2f_1 - f_2$	–18	–12	—	dBm
Image Rejection[2]	IR		50	55	—	dB
1 dB Input Compression[2,5]	CP_{MAX}	GSM bands	–28	–22	—	dBm
		DCS/PCS bands	–28	–22	—	dBm
1 dB Input Compression[2,6]	CP_{MIN}	GSM bands	–23	–18	—	dBm
		DCS/PCS bands	–23	–18	—	dBm
Minimum Voltage Gain[2,6,7]	G_{MIN}	GSM bands	4	8	12	dB
		DCS/PCS bands	11	16	19	dB
Maximum Voltage Gain[2,7]	G_{MAX}	GSM bands	98	102	106	dB
		DCS/PCS bands	96	101	104	dB
LNA Gain Control Range	ΔG_{LNA}	GSM bands	11	15	19	dB
		DCS/PCS bands	3	7	11	dB
Analog PGA Control Range	ΔG_{APGA}		13	16	19	dB
Analog PGA Step Size			3.1	4.0	4.8	dB
Digital PGA Control Range	ΔG_{DPGA}		—	63	—	dB
Digital PGA Step Size			—	1	—	dB

Table 5. Receiver Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Differential Output Voltage[8]		DACFS[1:0] = 00	0.8	1.0	1.2	V_{PPD}
		DACFS[1:0] = 01	1.6	2.0	2.4	V_{PPD}
		DACFS[1:0] = 10	2.8	3.5	4.2	V_{PPD}
Output Common Mode Voltage[8]		DACCM[1:0] = 00	0.8	1.0	1.2	V
		DACCM[1:0] = 01	1.05	1.25	1.45	V
		DACCM[1:0] = 10	1.15	1.35	1.55	V
Differential Output Offset Voltage[8,9,10,11]			—	—	20	mV
Differential Output Offset Voltage Drift[3,8,9,11]			—	—	5	mV
Baseband Output Gain Error[8,11‘]			—	—	1	%
Baseband Output Phase Error[8,11‘]			—	—	1	deg
Output Load Resistance[8]	R_L	Single-ended	10	—	—	kΩ
Output Load Capacitance[8]	C_L	Single-ended	—	—	10	pF
Group Delay[12,14]		FILTSEL = 0	—	9.0	—	µs
		FILTSEL = 1	—	11.5	—	µs
Group Delay Variation[12,14]		FILTSEL = 0	—	1.0	—	µs
		FILTSEL = 1	—	0.1	—	µs
Powerup Settling Time[13,14]		From powerdown	—	—	182	Qb

Notes:

1. GSM 850 input pins RFIAP and RFIAN. E-GSM 900 input pins RFIEP and RFIEN. DCS 1800 input pins RFIDP and RFIDN. PCS 1900 input pins RFIPP and RFIPN.
2. Measurement is performed with a 2:1 balun (50 Ω input, 200 Ω balanced output) and includes matching network and PCB losses. Measured at max gain (AGAIN[2:0] = max = 100, LNAG = max = 1) unless otherwise noted. Noise figure measurements are referred to 290 °K. Insertion loss of the balun is removed.
3. Specifications guaranteed by characterization.
4. Input signal at balun output is –102 dBm. SNR at baseband output is 9 dB.
5. AGAIN[2:0] = min = 000, LNAG = max = 1.
6. AGAIN[2:0] = min = 000, LNAG = min = 0.
7. Voltage gain is defined as the differential rms voltage at the BIP/BIN pins or BQP/BQN pins divided by the rms voltage at the balun input with DACFS[1:0] = 01. Minimum and maximum values do not include the variation in the baseband DAC full-scale voltage. (Also see Maximum Differential Output Voltage specifications.)
8. Pins BIP, BIN, BQP, and BQN.
9. Specified as root sum square: $\sqrt{(RXIP - RXIN)^2 + (RXQP - RXQN)^2}$. Drift specification applies to dc offset calibration and is guaranteed by characterization. See RXODEL[2:0] in register 08h.
10. For DACFS[1:0] = 00.
11. The baseband receive signal path is entirely digital. Gain, phase, and offset errors at the analog baseband outputs are due to the receive I/Q D/A converters. Offsets can be measured and calibrated out. See RXODEL[2:0] in register 08h.
12. Group delay is measured from antenna input to baseband outputs. Group delay variation is the difference between minimum and maximum values measured in-band.
13. Includes settling time of the frequency synthesizer and transceiver operations. Settling to better than 5 degrees peak phase error and 0.1 ppm frequency error measured at BIP, BIN, BQP, and BQN pins.
14. Specifications guaranteed by design.

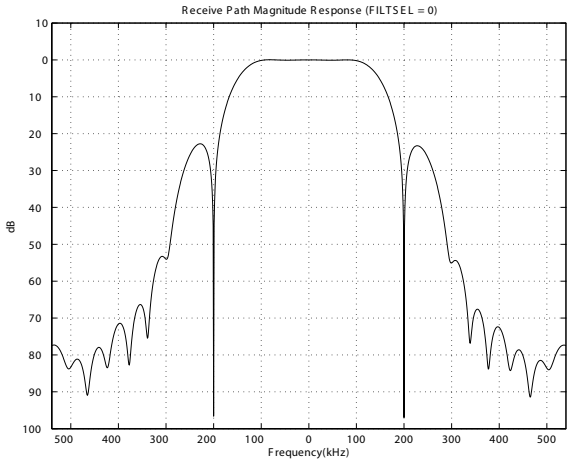


Figure 5. Receive Path Magnitude Response (FILTSEL = 0)

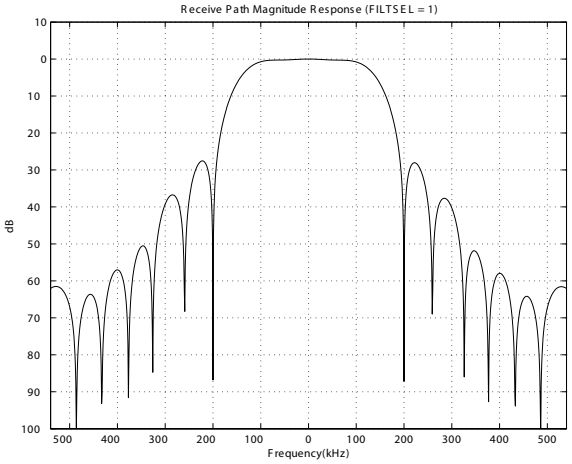


Figure 8. Receive Path Magnitude Response (FILTSEL = 1)

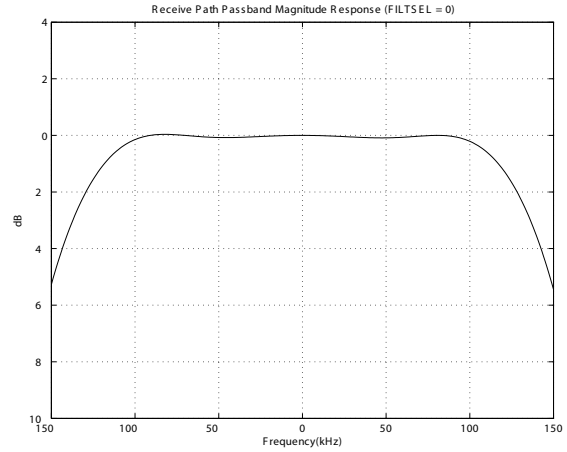


Figure 6. Receive Path Passband Magnitude Response (FILTSEL = 0)

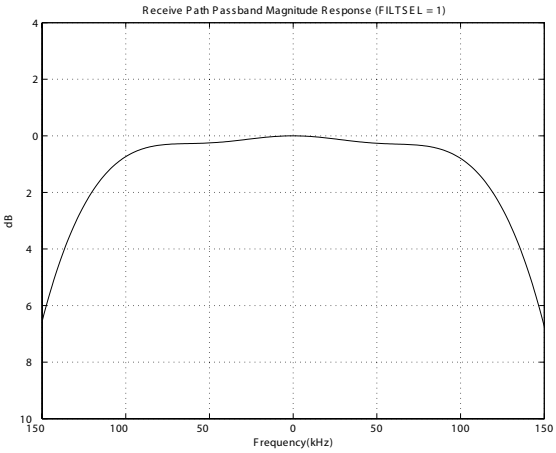


Figure 9. Receive Path Passband Magnitude Response (FILTSEL = 1)

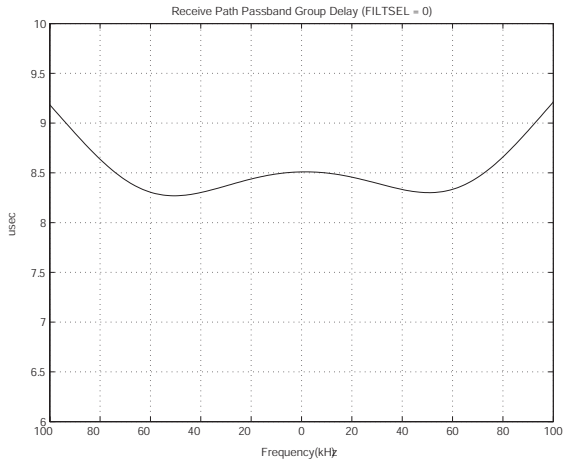


Figure 7. Receive Path Passband Group Delay (FILTSEL = 0)

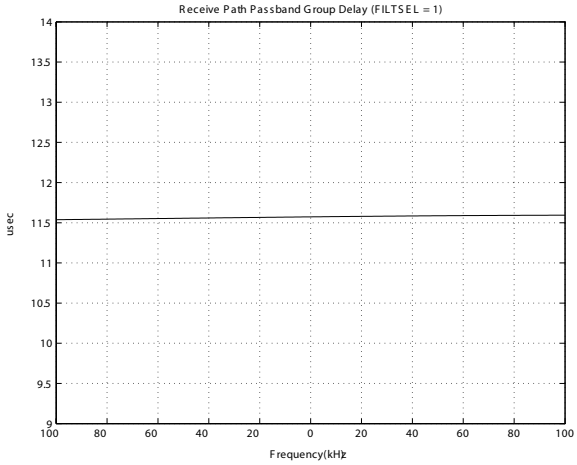


Figure 10. Receive Path Passband Group Delay (FILTSEL = 1)

Table 6. Transmitter Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RFOL Output Frequency[1]		GSM 850 band	824	—	849	MHz
		E-GSM 900 band	880	—	915	MHz
RFOH Output Frequency[2]		DCS 1800 band	1710	—	1785	MHz
		PCS 1900 band	1850	—	1910	MHz
Sideband Suppression		67.7 kHz sinusoid	—	–46	–34	dBc
Carrier Suppression		67.7 kHz sinusoid	—	–48	–33	dBc
IM3 Suppression		67.7 kHz sinusoid	—	–57	–50	dBc
Phase Error[4]		RFOL Transmit Mode	—	1.5	3.0	$^{o}_{rms}$
		RFOH Transmit Mode	—	1.9	3.0	$^{o}_{rms}$
			—	5	10	$^{o}_{PEAK}$
TXVCO Pulling[1,2,4]		VSWR 2:1, all phases, open loop	—	50	—	kHz_{PP}
RFOL Output Modulation Spectrum[1,5]		400 kHz offset	—	–66	–63	dBc
		1.8 MHz offset	—	–70	–68	dBc
RFOH Output Modulation Spectrum[2,5]		400 kHz offset	—	–65	–63	dBc
		1.8 MHz offset	—	–70	–65	dBc
RFOL Output Phase Noise[1,3,6]		10 MHz offset	—	–160	–155	dBc/Hz
		20 MHz offset	—	–165	–164	dBc/Hz
RFOH Output Phase Noise[2,3,6]		20 MHz offset	—	–160	–157	dBc/Hz
RFOL Output Power Level[1]		Z_L = 50 Ω	6.0	7.0	8.0	dBm
RFOH Output Power Level[2]		Z_L = 50 Ω	5.0	6.0	7.0	dBm
RF Output Harmonic Suppression[1,2]		2nd harmonic	—	—	–20	dBc
		3rd harmonic	—	—	–10	dBc
I/Q Input Common-Mode[7]			1.1	—	1.4	V
I/Q Differential Input Swing[7,8]		BBG[1:0] = 00	1.70	1.95	2.20	V_{PPD}
		BBG[1:0] = 01	1.35	1.52	1.70	V_{PPD}
		BBG[1:0] = 10	1.00	1.18	1.35	V_{PPD}
		BBG[1:0] = 11	0.80	0.90	1.00	V_{PPD}

Table 6. Transmitter Characteristics (Continued)

(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I/Q Differential Input Resistance[7,8]	R_{IN}	BBG[1:0] = 00	24.0	28.5	33.5	kΩ
		BBG[1:0] = 01	20.5	24.5	29.0	kΩ
		BBG[1:0] = 10	17.5	21.0	24.5	kΩ
		BBG[1:0] = 11	15.0	18.0	21.0	kΩ
		Powered down	85	100	115	kΩ
I/Q Input Capacitance[4,7]	C_{IN}		—	—	5	pF
I/Q Input Bias Current[4,7]	I_B		–1	—	1	µA
Powerup Settling Time[4,9]		From powerdown	—	—	166	Qb

Notes:

1. Measured at RFOL pin.
2. Measured at RFOH pin.
3. Specifications guaranteed by characterization.
4. Specifications guaranteed by design.
5. Measured with pseudo-random pattern. Carrier power and noise power < 1.8 MHz measured with 30 kHz RBW. Noise power ≥ 1.8 MHz measured with 100 kHz RBW.
6. Measured with all 1s pattern.
7. Pins BIP, BIN, BQP, and BQN.
8. Differential Input Swing is programmable with the BBG[1:0] bits in register 05h. Program these bits to the closest appropriate value. The I/Q Input Resistance scales inversely with the BBG[1:0] setting.
9. Includes settling time of the frequency synthesizer. Settling time measured at the RFOL and RFOH pins to 5 degrees peak phase error and for TXODEL[2:0] = 010h in Register 05h. This specification ensures that the average frequency error across the burst will be less than 0.1 ppm. Specification guaranteed by design.

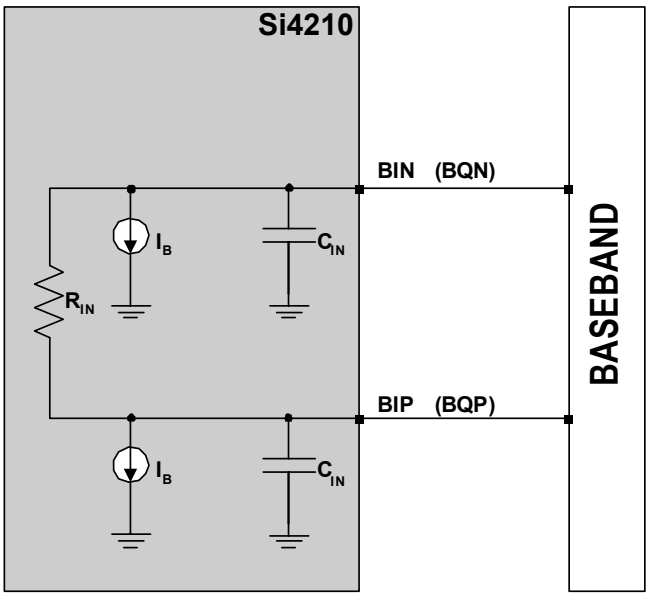


Figure 11. BB I/Q Input Equivalent Circuit

Table 7. Transmitter Carrier Wave Characteristics (CW Mode) for 8-PSK EGPRS[1]

(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RFOL Output Phase Noise[2,4]		400 kHz offset, CW = 1	—	–123	–121	dBc/Hz
		10 MHz offset, CW = 1	—	–157	–155	dBc/Hz
		20 MHz offset, CW = 1	—	–164	–162	dBc/Hz
RFOH Output Phase Noise[3,4]		400 kHz offset, CW = 1	—	–119	–117	dBc/Hz
		20 MHz offset, CW = 1	—	–158	–156	dBc/Hz
RFOL Output Power Level[2]		Z_L = 50 Ω, CW = 1	6.0	7.0	8.0	dBm
RFOH Output Power Level[3]		Z_L = 50 Ω, CW = 1	5.0	6.0	7.0	dBm
I/Q Differential Input Resistance[5]		CW = 1	85	100	115	kΩ
I/Q Input Capacitance[5,6]		CW = 1	—	—	10	pF
Mode Switch Settling Time[6,7,8]		Transition between CW = 0 and CW = 1, after register latch	—	20	—	Qb

Notes:

1. Set CW = 1, Register 23h to generate a carrier wave output.
2. Measured at RFOL pin.
3. Measured at RFOH pin.
4. Specifications guaranteed by characterization.
5. Pins BIP, BIN, BQP, and BQN.
6. Specifications guaranteed by design.
7. Includes settling time of the frequency synthesizer. Settling time measured at the RFOL and RFOH pins to 5 degrees peak phase error and for TXODEL[2:0] = 010h in Register 05h. This specification ensures that the average across the burst will be less than 0.1 ppm. Specification guaranteed by design.
8. Timing refers to GMSK bits.

Table 8. Reference Oscillator Characteristics: Digitally-Controlled Crystal Oscillator (DCXO) Mode
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillation Frequency[1]	f_{XTAL}		—	26	—	MHz
Oscillator XOUT Frequency	f_{XOUT13}	XDIV = V_{DD}	—	13	—	MHz
	f_{XOUT26}	XDIV = GND	—	26	—	MHz
Analog AFC Input Voltage	V_{AFC}	XMODE = V_{DD}, AFCREF = 0	0.0	—	2.1	V
	V_{AFC}	XMODE = V_{DD}, AFCREF = 1	0.0	—	2.5	V
CAFC Differential Capacitance Range[2]	C_{AFC_FS}	XMODE = V_{DD}	—	2.4	—	pF
CDAC Differential Capacitance Range[2]	C_{DAC_FS}	XMODE = V_{DD}	—	4.8	—	pF
Fixed Differential Capacitance[2]	C_{FIX}	XMODE = V_{DD}	—	4.2	—	pF
Powerup Settling Time[3]	t_{DCXO}	XMODE = V_{DD}, f_{XTAL} = 26 MHz V_{CTL} = 0 to 1.25 V	—	1.0	—	ms

Notes:
1. Specifications set by crystal manufacturer.
2. Parameters relate to reference oscillator frequency tuning range. See "AN152: Selecting a Crystal for Aero II Designs" for detailed instructions on crystal selection.
3. Specifications guaranteed by design.

Table 9. Reference Oscillator Characteristics: VC-TCXO Mode[1]
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency[1]	f_{XTAL}		—	26	—	MHz
Oscillator XOUT Frequency	f_{XOUT13}	XDIV = V_{DD}	—	13	—	MHz
	f_{XOUT26}	XDIV = GND	—	26	—	MHz
XTAL1 Input Resistance	R_{XTAL1}	XMODE = GND	—	300	Hi-Z	kΩ
XTAL1 Input Capacitance[3]	C_{XTAL1}	XMODE = GND	—	8.4	10	pF
XTAL1 Input Sensitivity	V_{REF}	XMODE = GND	0.7	1	V_{DD}	V_{PP}

Notes:
1. Specifications set by VC-TCXO manufacturer.
2. The VC-TCXO output should be input into XTAL1, and XTAL2 should be connected to GND. XTAL1 is internally AC coupled and no external AC capacitor is needed.
3. Specifications guaranteed by design.

2. Typical Application Schematic

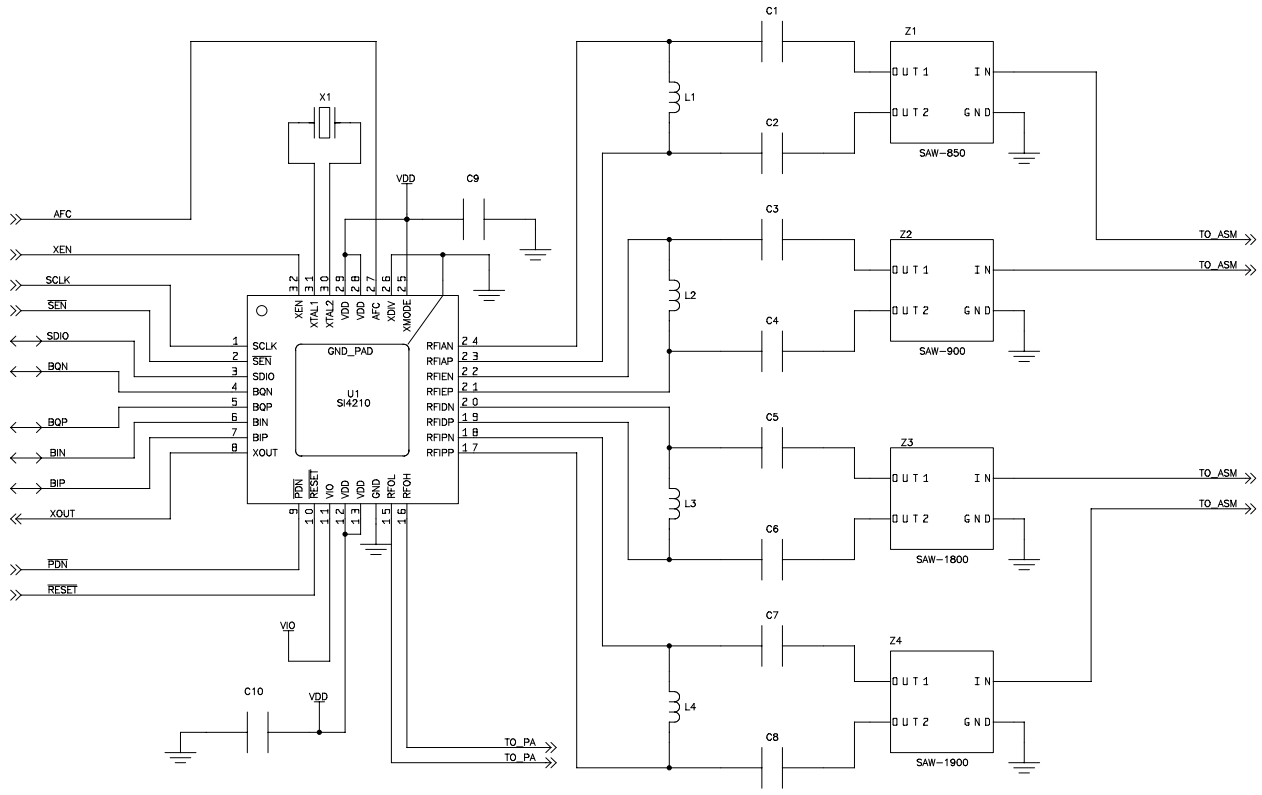


Figure 12. Typical Quad-Band Application Circuit

Notes:

1. Connect GND pad on bottom of U1 to GND plane.
2. All transceiver (U1) V_{DD} pins may be fed from a single supply or regulator. May require active pull-down regulator, depending on power management option chosen. Please refer to "AN150: Aero II Transceiver PCB Design Guide."
3. V_{IO} pin may be connected to the phone memory regulator.
4. For dual and tri-band designs, unused LNA pins should be differentially shorted.
5. See "AN150: Aero II Transceiver PCB Design Guide" for details on the following:
   - LNA matching network (C1–C8, L1–L4). Values should be custom tuned for a specific PCB layout and SAW filter to optimize performance.
   - Differential traces between SAW filters (Z1–Z4) and transceiver (U1) pins 17–24.
   - Layout of XTAL1 and XTAL2 lines between crystal (X1) and transceiver (U1) pins 30–31.
   - Power management design options.
6. See "AN152: Selecting a Crystal for Aero II Designs" for details on the selection of X1.

3. Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1–C2	1.0 pF, ±0.1 pF, COG GSM 850 matching capacitor	
C3–C4	1.2 pF, ±0.1 pF, COG E-GSM 900 matching capacitor	
C5–C6	0.9 pF, ±0.1 pF, COG DCS 1800 matching capacitor	
C7–C8	0.75 pF, ±0.1 pF, COG PCS 1900 matching capacitor	
C9, C10	0.10 µF, ±20%, Z5U/X7R	
L1	30 nH GSM 850 matching inductor	
L2	27 nH E-GSM 900 matching inductor	
L3	8.7 nH DCS 1800 matching inductor	
L4	8.2 nH PCS 1900 matching inductor	
U1	Quad-Band GSM/GPRS Transceiver	Silicon Laboratories Si4210-GM
X1	26 MHz crystal	Kyocera CX3225SB-H2827 NDK W-168-405 KDS 1B326000AA0B Toyocom TSX-3225 26 MHz, TN4-26245 SEMCO SQ3D02600B2IBA
Z1	GSM 850 receive SAW filter (150 or 200 Ω balanced output)	EPCOS B39881-B9001-C710 (5-pin, 1.4 x 2.0 mm) EPCOS B39881-B9004-E710 (6-pin, 1.6 x 2.0 mm) Murata SAFEK881MFL0T00R00 (6-pin, 1.6 x 2.0 mm)
Z2	E-GSM 900 receive SAW filter (150 or 200 Ω balanced output)	EPCOS B39941-B7820-C710 (5-pin, 1.4 x 2.0 mm) Murata SAFEK942MFM0T00R00 (6-pin, 1.6 x 2.0 mm)
Z3	DCS 1800 receive SAW filter (150 or 200 Ω balanced output)	EPCOS B39182-B7821-C710 (5-pin, 1.4 x 2.0 mm) EPCOS B39182-B9013-K310 (6-pin, 1.6 x 2.0 mm) Murata SAFEK1G84FA0T00R00 (6-pin, 1.6 x 2.0 mm)
Z4	PCS 1900 receive SAW filter (150 or 200 Ω balanced output)	EPCOS B39202-B7825-C710 (5-pin, 1.4 x 2.0 mm) Murata SAFEK1G96FA0T00R00 (6-pin, 1.6 x 2.0 mm)

4. Functional Description

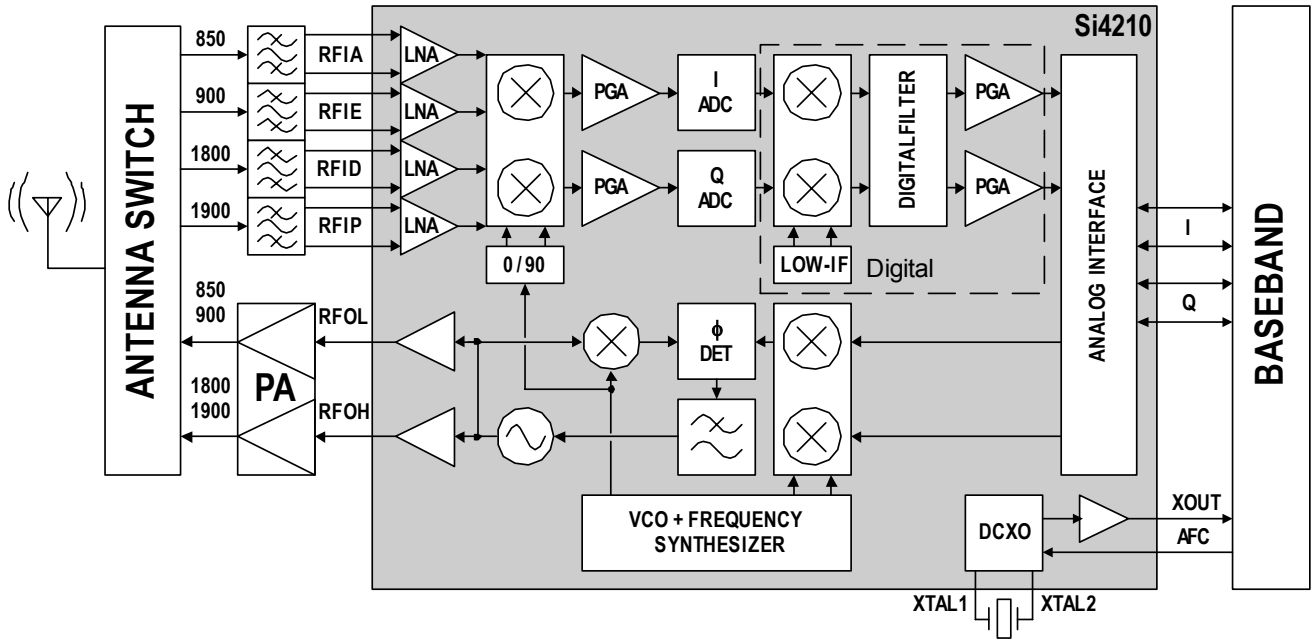


Figure 13. Si4210 Transceiver Block Diagram

The Aero II transceiver is the industry's most integrated RF front end for multi-band GSM/GPRS digital cellular handsets and wireless data modems. The high-level of integration obtained through patented and proven design architectures, fine line CMOS process technology, and high-performance quad flat no-lead (QFN) technology results in a transceiver solution with industry-leading performance, the smallest form factor, the fewest number of components, the smallest solution footprint, and the lowest bill of materials (BOM) in the industry. A quad-band RF front end using the Aero II transceiver can be implemented with 19 components in less than 1 cm^2 of board area. This level of integration is an enabling force in lowering the cost, simplifying the design and manufacturing, and shrinking the form factor in next-generation GSM/GPRS voice and data terminals.

The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering higher performance, lower solution cost, and reduced complexity. The baseband interface is compatible with any supplier's baseband subsystem.

The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (OPLL) with a fully integrated transmit VCO.

The frequency synthesizer uses Silicon Laboratories' proven technology that includes an integrated RF VCO, loop filter, and varactor. The unique integer-N PLL architecture produces a transient response superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the Aero II transceiver well suited to GPRS multi-slot applications where channel switching and settling times are critical.

The analog baseband interface is used with conventional GSM baseband ICs (BBIC). The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface. A standard three-wire serial interface is used to control the transceiver.

While conventional solutions use SiGe, BiCMOS, or other bipolar process technologies, the Aero II transceiver is Silicon Laboratories' third-generation transceiver to be implemented in a 100% CMOS process. Silicon Laboratories' focus on RF and analog mixed-signal CMOS design creates innovation in integration, space savings, and fabrication cost. This further extends the cost savings and extensive manufacturing capacity of CMOS to the GSM/GPRS market.

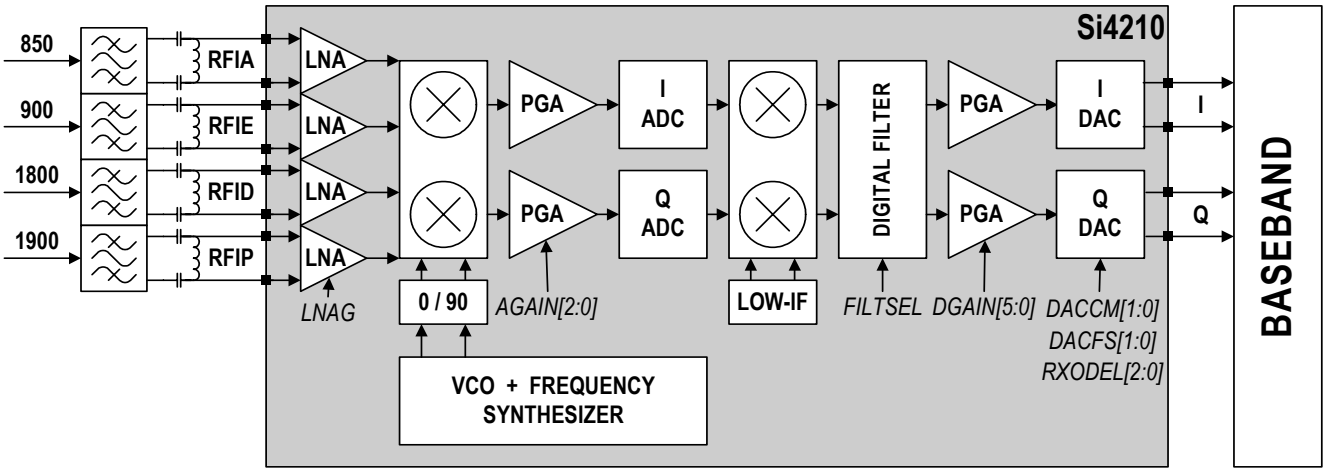


Figure 14. Receiver Block Diagram

4.1. Receiver

The Aero II transceiver uses a digital low-IF receiver architecture that allows for the on-chip integration of the channel selection filters, eliminating the external RF image reject filters, and the IF SAW filter required in conventional superheterodyne architectures. Compared with direct-conversion architectures, the digital low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, second-order distortion of blockers (AM suppression), and device 1/f noise.

The digital low-IF receiver's immunity to dc offsets has the benefit of expanding part selection and improving manufacturing. At the front end, the common-mode balance requirements on the input SAW filters are relaxed, and the PCB board design is simplified. At the radio's opposite end, the BBIC is one of the handset's largest BOM contributors. It is not uncommon for a direct conversion solution to be compatible only with a BBIC from the same supplier in order to address the complex dc offset issues. However, since the Aero II transceiver has no requirement for BBIC support of complex dc offset compensation, it is able to interface to all of the industry leading baseband ICs.

The receive (RX) section integrates four differential-input low noise amplifiers (LNAs) supporting the GSM 850 (869–894 MHz), E-GSM 900 (925–960 MHz), DCS 1800 (1805–1880 MHz), and PCS 1900 (1930–1990 MHz) bands. The LNA inputs are matched to 150 or 200 Ω balanced-output SAW filters through external LC matching networks. See "AN150: Aero II Transceiver PCB Design Guide" for implementation details. The active LNA input is automatically selected by the ARFCN[9:0] bits and the BANDIND bit in Register 21h. If performing LNA swapping, the LNASWAP bit in Register 05h is also needed. Please refer to section 4.1.1 for details. The LNA gain is controlled with the LNAG bit in Register 20h.

A quadrature image-reject mixer downconverts the RF signal to a low intermediate frequency (IF). The mixer output is amplified with an analog programmable gain amplifier (PGA) that is controlled with the AGAIN[2:0] bits in Register 20h. The quadrature IF signal is digitized with high resolution analog-to-digital converters (ADCs).

The ADC output is downconverted to baseband with a digital quadrature local oscillator signal. Digital decimation and FIR filters perform digital filtering, and remove ADC quantization noise, blockers, and reference interferers. The response of the FIR filter is programmable to a flat passband setting (FILTSEL = 0, Register 08h) and a linear phase setting (FILTSEL = 1, Register 08h). After filtering, the digital output is scaled with a PGA, which is controlled with the DGAIN[5:0] bits in Register 20h.

The LNAG, AGAIN[2:0], and DGAIN[5:0] register bits should be set to provide a constant amplitude signal to the baseband receive inputs. See "AN153: Aero II Transceiver AGC Strategy" for more details.

Digital-to-analog converters (DACs) drive differential I and Q analog signals onto the BIP, BIN, BQP, and BQN pins to interface to standard analog-input baseband ICs. The receive DACs are updated at 1.083 MHz and have a first-order reconstruction filter with a 1 MHz bandwidth. No special processing is required in the baseband for dc offset compensation. The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). The common mode level at the receive I and Q outputs is programmable with the DACCM[1:0] bits, and the full-scale level is programmable with the DACFS[1:0] bits in Register 05h.

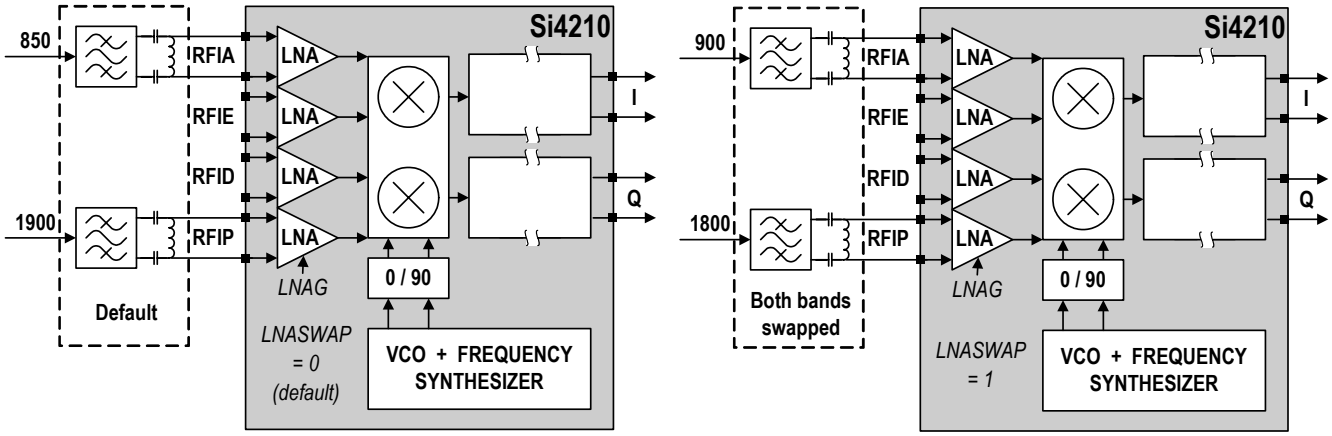


Figure 15. Example Application of Swapped LNA Inputs

4.1.1. Phone Region Management Using LNA Swapping

The Aero II LNA inputs may be swapped. The low-band LNA inputs, RFIA and RFIE, are interchangeable and may be used to receive either the GSM 850 or E-GSM 900 band. The high-band inputs, RFID and RFIP, are interchangeable and may be used to receive either the DCS 1800 or PCS 1900 band. This flexibility enables radio designers to use one PCB layout for a phone design with only a bill of materials and software change to address different regions.

For normal operation, the LNA swap bit should be set to zero; this is the default setting. In this default mode, the native pin inputs and LNA are used for the corresponding frequency band. As an example, the RFIA inputs and GSM 850 LNA are used for GSM 850 operation.

To implement LNA swapping with the Aero II transceiver, the LNA swap bit in register 05h is used. The LNA swap bit should then be set to one. In LNA swapping mode, the non-native pin inputs and LNA are used for the frequency band. As an example, the RFIA inputs and GSM 850 LNA are used for E-GSM 900 operation.

An example application is shown in Figure 15. Please refer to “AN151: Aero II Transceiver Programming Guide” for LNASWAP programming details.

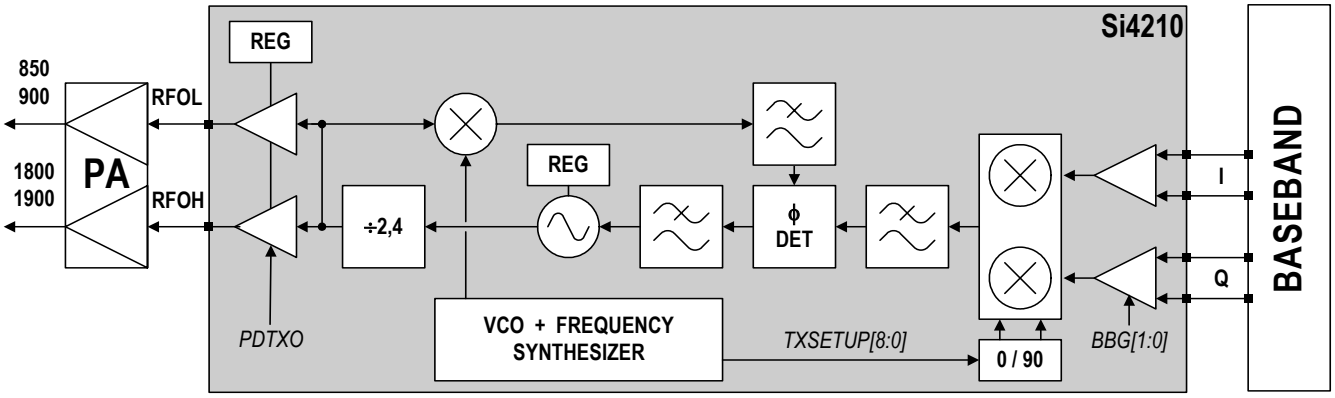


Figure 16. Transmitter Block Diagram

4.2. Transmitter

The transmit section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two output buffers that can drive an external power amplifier (PA). One output is for the GSM 850 (824–849 MHz) and E-GSM 900 (880–915 MHz) bands and one output is for the DCS 1800 (1710–1785 MHz) and PCS 1900 (1850–1910 MHz) bands.

The OPLL requires no external filtering to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. The output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA. Additionally, the TXVCO benefits from isolation provided by the transmit output buffers. This significantly minimizes any load pull effects and eliminates the need for off-chip isolation networks.

A quadrature mixer upconverts the differential in-phase (BIP, BIN) and quadrature (BQP, BQN) baseband signals to an intermediate frequency (IF) that is filtered and which is used as the reference input to the OPLL. The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs.

The transmit I/Q interface must have a non-zero input no later than 94 quarter bits after $\overline{\text{PDN}}$ is asserted for proper operation. If the baseband is unable to provide a sufficient TX I/Q non-zero input preamble, then the CWDUR bits in Register 05h can be used to provide a preamble extension.

The receive and transmit baseband I/Q pins are multiplexed together in a 4-wire interface (BIP, BIN, BQP, and BQN). In transmit mode, the BIP, BIN, BQP, and BQN pins provide the analog I/Q input from the baseband subsystem. The full-scale level at the baseband input pins is programmable with the BBG[1:0] bits in Register 05h. The transmit output path is automatically selected by the ARFCN[9:0] bits and the BANDIND bits in Register 21h. As an option for multi-slot applications, direct control of the output transmit buffers during a burst is offered through the PDTXO bit in Register 23h.

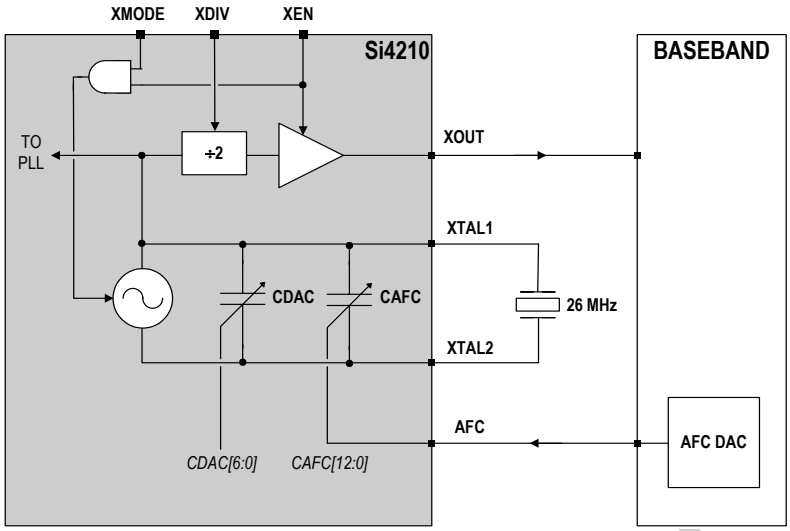


Figure 17. DCXO Block Diagram

4.3. Digitally-Controlled Crystal Oscillator (DCXO)

The Aero II transceiver integrates the DCXO circuitry required to generate a precise system reference clock using only an external crystal resonator. The DCXO replaces a discrete VC-TCXO module. The DCXO allows for the use of a standard 26 MHz crystal, which reduces both cost and area compared to using a VC-TCXO module. There are no external varactors or trim capacitors required. This simplifies the design, programming, and manufacturing compared to less integrated solutions.

The DCXO uses the CDAC and CAFC arrays to correct for both static and dynamic frequency errors, respectively. An internally digitally programmable capacitor array (CDAC) provides a coarse method of adjusting the reference frequency in discrete steps. The CDAC[6:0] bits in Register 03h are programmed to compensate for static variations in PCB design, manufacturing, and crystal tolerance, and are typically set to center the oscillator frequency during production test.

A second capacitor array (CAFC) allows for fine and continuous dynamic adjustment of the reference frequency by an external control voltage (AFC). This control voltage is supplied by the AFC DAC of the baseband and should be connected to the transceiver AFC pin (pin 27). The baseband determines the appropriate frequency adjustment based on the receipt of the FCCH burst. The baseband then adjusts the AFC voltage to correct for frequency variations caused by temperature drift.

The transceiver can be adjusted for the corresponding baseband AFC input full-scale voltage by setting the AFCREF bit in Register 04h. Additionally, the Aero II transceiver supports an optional Digital AFC mode for DCXO operation that is selected by the AFCC bit in Register 04h. In digital mode, the connection between the baseband and transceiver is eliminated and the AFC pin should be tied low. AFC control is performed directly by a register write operation. This has the benefit of further easing PCB design and enabling a DAC in the baseband to be allocated to another function. Alternatively, the BB DAC could be disabled and the BB current consumption reduced.

The Aero II transceiver can be configured in DCXO mode or VC-TCXO mode by the XMODE pin. To use the transceiver in DCXO mode, the XMODE pin is tied high. The XTAL1 and XTAL2 pins are then connected directly to the 26 MHz crystal. No additional components are required. The use of an external VC-TCXO module is also supported by tying the XMODE pin low. The VC-TCXO output should be input into XTAL1, and XTAL2 should be grounded. XTAL1 is internally AC coupled and no external AC capacitor is needed.

A buffer is available to provide a reference clock output from the XOUT pin to the baseband input. The XOUT buffer is enabled when the XEN pin is set high, independent of the $\overline{\text{PDN}}$ pin. To achieve complete powerdown during sleep, the XEN pin should be set low to disable the XOUT buffer. The XOUT buffer is specified to drive a maximum load of 10 pF. The reference clock should be set to 13 MHz or 26 MHz by the XDIV pin. When XDIV is tied low, XOUT is 26 MHz, and when it is tied high, XOUT is 13 MHz.

For a simple to follow methodology and detailed

instructions on crystal selection, see "AN152: Selecting a Crystal for Aero II Designs," or contact Silicon Laboratories Applications Support for assistance.

4.4. Serial Control Interface

A three-wire serial interface is provided for the baseband IC to read and write the control registers. The serial control word is 21 bits in length, comprised of a 15-bit data field and a 6-bit address field. The register mapping is summarized in Table 10 on page 23.

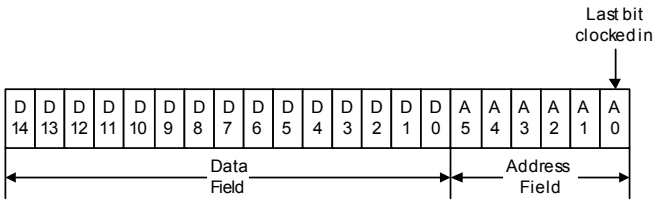


Figure 18. Serial Interface Format

All registers must be written when the $\overline{PDN}$ pin is asserted (low), except for the RX Burst register (20h) and the TX Burst register (23h), which may be written when the $\overline{PDN}$ pin is low or high. Register 20h allows the gain to be changed between multislot bursts. Register 23h allows disabling of the transmit output buffer during a transmit burst. The serial interface pins should be held at a constant level during receive and transmit bursts to minimize spurious emissions. This includes stopping the SCLK clock.

When the serial interface is enabled ($\overline{SEN}$ is low), data and address bits on the SDIO pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of $\overline{SEN}$ into the internal data register addressed in the address field. The serial interface is disabled when $\overline{SEN}$ is high. A timing diagram for the serial interface is shown in Figure 3 on page 7.

Optionally, registers can be read as illustrated in Figure 4 on page 7. The serial output data appears on the SDIO pin after writing the REV[7:0] register with the address to be read.

The V_{IO} pin should be connected to a supply that is always on when the phone is on. The V_{IO} supply should be maintained through reset events to preserve self-calibration settings when V_{DD} is removed. Both hardware and software designs must be coordinated to ensure an effective power management strategy. Detailed instructions regarding V_{IO} implementation can be found in “AN150: Aero II Transceiver PCB Design Guide” and “AN151: Aero II Transceiver Programming Guide.”

4.5. Programming

When power is first applied to the Aero II transceiver, the $\overline{PDN}$ pin should be held low. Depending on the power management strategy, the $\overline{RESET}$ pin may be driven by a baseband GPO. Please refer to “AN150: Aero II Transceiver PCB Layout Guidelines” for details. When used, the $\overline{RESET}$ pin should be held low until the V_{DD} supply has settled. When the $\overline{RESET}$ pin is low, all registers are set to their default values. Before removing V_{DD} from Aero II, $\overline{RESET}$ should be set low to safely preserve register settings. The relationship between V_{DD} and $\overline{RESET}$ is shown in Figure 1 on page 6. Additionally, before removing V_{DD} from Aero II, all pins should be brought to ground to avoid forward biasing the electrostatic discharge (ESD) protection circuitry.

Idle state is entered whenever the $\overline{PDN}$ pin is at a logic low level. In this mode, the power consumption of the transceiver is minimized while retaining all register values. Registers are written in this mode. All register writes should be completed before $\overline{PDN}$ goes high.

During normal operation, the $\overline{PDN}$ pin will be held low the majority of the time and the DCXO reference clock will be enabled by setting XEN high. $\overline{PDN}$ will then be brought high before the receive or transmit burst. $\overline{PDN}$ will be held high throughout the burst. $\overline{PDN}$ can be brought low after the receive burst or after the transmit power amplifier ramp-down.

A write to Register 20h, while $\overline{PDN}$ is low, places the transceiver into receive (RX) mode. A write to Register 23h, while $\overline{PDN}$ is low, places the transceiver into transmit (TX) mode. The Aero II transceiver supports the initiation of receive and transmit operations with only two register writes. Detailed instructions of register programming for the Aero II transceiver can be found in "AN151: Aero II Transceiver Programming Guide".

5. Control Registers

Table 10. Register Summary

Reg	Name	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	Revision/ Read	0	0	0	0	0	0	0	REV[7:0]							
03h	DCXO CDAC	0	0	0	0	0	0	1	XOUT DRV	CDAC[6:0]						
04h	DCXO Config	0	0	0	0	0	AFCREF	AFCC	0	0	0	0	0	0	0	0
05h	Config	CWDUR[1:0]		TXODEL[2:0]			1	0	BBG[1:0]		DACCM[1:0]		DACFS[1:0]		LNASWAP	INIT
08h	Config	0	0	0	1	0	0	RXODEL[2:0]			FILTSEL	CALDUR[3:0]				0
11h	Eval	0	0	0	CALC[1:0]		0	0	0	0	0	0	0	0	0	0
Master Registers																
20h	RX Burst	0	0	0	0	0	LNAG	AGAIN[2:0]			DGAIN[5:0]					
21h	Burst Freq	0	0	0	0	BAND IND	ARFCN[9:0]									
22h	Burst AFC	0	0	CAFC[12:0]												
23h	TX Burst	0	0	0	0	CW	PDTXO	TXSETUP[8:0]								

Notes:

1. Any register not listed here is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.
2. Master registers 20h to 23h simplify programming Aero II to support initiation of receive (RX) and transmit (TX) operations with only two register writes.
   See “AN151: Aero II Transceiver Programming Guide” for detailed instructions on register programming.

6. Register Descriptions

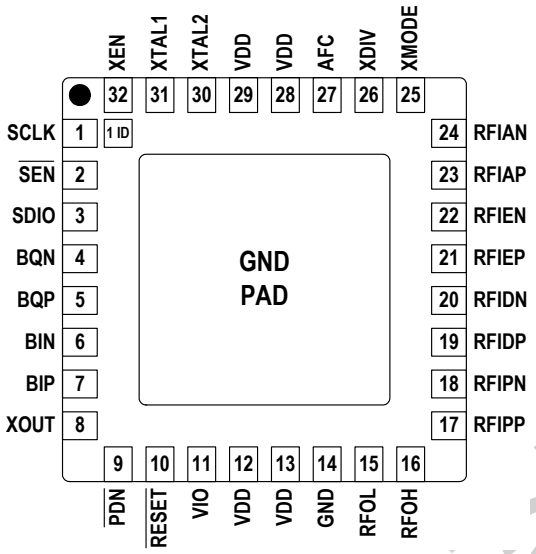
Note: The "(default)" designation in the function column refers to the state that a register takes after power-on or reset.

Reg	Bit(s)	Name	Function
00h	7:0	REV[7:0]	**Chip Revision (read only).** 10010h = Si4210 revision C **Note:** During a register read operation, this register should be written with the address of the register to be read.
03h	7	XOUTDRV	**XOUT Drive Level.** 0 = Low drive level 1 = High drive level - drive level for a maximum 10 pF load on XOUT pin (default)
03h	6:0	CDAC[6:0]	**DCXO Coarse Frequency Adjustment.** 0000000 = Lowest frequency 1000000 = Midscale frequency (default) 1111111 = Highest frequency **Notes:** **1.** Used to store factory calibration result for DCXO. **2.** The direction of CDAC[6:0] for lowest and highest frequency is different from previous products.
04h	9	AFCREF	**Analog AFC Input Voltage.** 0 = Max AFC full-scale voltage is 2.1 V (default) 1 = Max AFC full-scale voltage is 2.5 V
04h	8	AFCC	**AFC Mode.** 0 = Analog mode. Analog input sampled during the first 30 quarter bits after rising edge of $\overline{\text{PDN}}$ (default) 1 = Digital mode. AFC is controlled with the CAFC[12:0] bits **Notes:** **1.** In analog mode, connect analog baseband AFC output to pin 27. **2.** In digital mode, the connection between the baseband and transceiver is eliminated. AFC control is performed directly by a register write operation to Register 20h. The AFC pin should be tied low.
05h	14:13	CWDUR	**Duration Timer for Baseband Non-zero TX I/Q Preamble Extension.** 00 = 94 quarter bits from powerup 01 = 142 quarter bits from powerup (default) 10 = 158 quarter bits from powerup 11 = 174 quarter bits from powerup **Notes:** **1.** The transmit I/Q interface must have a non-zero input no later than 94 quarter bits after $\overline{\text{PDN}}$ is asserted. **2.** Basebands unable to provide a sufficient TX I/Q non-zero input preamble should use CWDUR to meet the 94 quarter bit non-zero input requirement.
05h	12:10	TXODEL[2:0]	**Transmit Output Delay.** These bits set the duration of zero transmit RF output for PA isolation 000 = Reserved 100 = 182 quarter bits 001 = 158 quarter bits 101 = 190 quarter bits 010 = 166 quarter bits 110 = 198 quarter bits 011 = 174 quarter bits (default) 111 = 206 quarter bits **Notes:** **1.** Transmit buffer output is inactive for this duration after $\overline{\text{PDN}}$ is deasserted. **2.** There should be a minimum of 20 Qb to the first start bit of the burst (bit 0).

Reg	Bit(s)	Name	Function
05h	9	AIF	**AIF Mode.** 0 = Fixed IF mode 1 = AIF mode. Enables high-side / low-side LO injection for alternating IF down-conversion (default).
05h	7:6	BBG[1:0]	**Transmit Baseband Input Full-Scale Differential Input Voltage.** 00 = 2.0 V_{PPD} 01 = 1.5 V_{PPD} 10 = 1.2 V_{PPD} (default) 11 = 0.9 V_{PPD} **Note:** Refer to Table 6 on page 11 for complete specifications. Set this register to the nearest value.
05h	5:4	DACCM[1:0]	**Receive Output Common Mode Voltage.** 00 = 1.0 V 01 = 1.25 V (default) 10 = 1.35 V 11 = Not supported
05h	3:2	DACFS[1:0]	**Receive Output Differential Full-Scale Voltage.** 00 = 1.0 V_{PPD} 01 = 2.0 V_{PPD} (default) 10 = 3.5 V_{PPD} 11 = Not supported
05h	1	LNASWAP	**LNA Swap Control.** 0 = Use the native LNA for the selected frequency band (example: use the GSM 850 LNA for GSM 850 operation) (default) 1 = Use the non-native LNA for the selected frequency band (example: use the GSM 850 LNA for E-GSM 900)
05h	0	INIT	**Initialization.** 0 = Normal operation (default) 1 = Self-calibration mode **Note:** Initialization band determined by ARFCN bits and BANDIND bit in Register 21h.
08h	8:6	RXODEL[2:0]	**Receive Output Delay.** These bits set the duration of zero receive BB output for BB ADC calibration. 000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100: 182 quarter bits (default) 101: 190 quarter bits 110: 198 quarter bits 111: 206 quarter bits **Note:** DAC input is at zero for this duration after $\overline{PDN}$ is deasserted.
08h	5	FILTSEL	**Digital FIR Coefficient Select.** 0 = Flat passband filter (default) 1 = Linear phase filter
08h	4:1	CALDUR[3:0]	**Self-Calibration Duration Setup.** 0100 = low-band self-calibration; pulse $\overline{PDN}$ high for 3900 quarter bits 0110 = high-band self-calibration; pulse $\overline{PDN}$ high for 12700 quarter bits
11h	11:10	CALC[1:0]	**Mode Control for Temperature and Supply Testing** 00 = Handset operation mode (default) 01 = Laboratory evaluation mode for rapid temperature and supply variation testing

Reg	Bit(s)	Name	Function
20h	9	LNAG	**LNA Gain Control.** 0 = LNA min gain (default) 1 = LNA max gain
20h	8:6	AGAIN[2:0]	**Analog PGA Gain Control.** 000 = AGAIN = 0 dB 001 = AGAIN = 4 dB 010 = AGAIN = 8 dB (default) 011 = AGAIN = 12 dB 1xx = AGAIN = 16 dB
20h	5:0	DGAIN[5:0]	**Digital PGA Gain.** 00h = 0 dB relative gain (default) 3Fh = 63 dB relative gain
21h	10	BANDIND	**Band Indicator.** 0 = Asia/Europe: DCS 1800 (default) 1 = Americas: PCS 1900 **Notes:** **1.** In the GSM system there is an overlap in the ARFCN for the DCS 1800 and PCS 1900 bands. The BANDIND bit is used to correct any potential conflict. The BANDIND bit is a “don’t care” for low-band operation. **2.** High-band band selection is determined by the ARFCN bits and BANDIND bit in register 21h.
21h	9:0	ARFCN[9:0]	**Channel Frequency.** 000h = Channel 0 (default) 3FFh = Channel 1023 **Notes:** **1.** Channel number corresponds to absolute radio frequency channel number (ARFCN). **2.** Band selection is determined by the ARFCN bits and BANDIND bit in register 21h.
22h	12:0	CAFC[12:0]	**DCXO Fine Frequency Adjustment for Digital AFC.** 0000h = Lowest frequency 1000h = Midscale frequency 1FFFh = Highest frequency **Note:** Writes to this register are effective only when AFCC = 1.
23h	10	CW	**Carrier Wave (CW) Mode (For 8-PSK EGPRS).** 0 = Normal operation (default) 1 = CW Mode
23h	9	PDTXO	**Disable Output Transmit Buffer.** 0 = Normal operation (default) 1 = Disables transmit output buffer while transmitter is running. This allows capability to improve isolation in multislot applications.
23h	8:0	TXSETUP[8:0]	**Transmit Setup.** 00Dh = GSM 850 1B0h = E-GSM 900 1D0h = DCS 1800 193h = PCS 1900 **Note:** These values must be programmed per band.

7. Pin Descriptions: Si4210-GM



Pin Number(s)	Name	Description
1 ID	—	Pin 1 ID marker (bottom). No connect; leave floating
1	SCLK	Serial clock input.
2	$\overline{\text{SEN}}$	Serial enable input (active low).
3	SDIO	Serial data input/output.
4,5	BQP, BQN	Transmit/receive Q input/output (differential).
6,7	BIP, BIN	Transmit/receive I input/output (differential).
8	XOUT	Clock output to baseband.
9	$\overline{\text{PDN}}$	Powerdown input (active low).
10	$\overline{\text{RESET}}$	Reset pin (active low). May be no connect.
11	V_{IO}	Interface supply voltage.
12, 13, 28, 29	V_{DD}	Supply voltage.
14, PAD	GND	Ground. Connect to ground plane on PCB.
15	RFOL	GSM 850 and E-GSM 900 band transmit output to power amplifier.
16	RFOH	DCS 1800 and PCS 1900 band transmit output to power amplifier.
17,18	RFIPP, RFIPN	PCS 1900 band LNA input (differential).
19, 20	RFIDP, RFIDN	DCS 1800 band LNA input (differential).
21, 22	RFIEP, RFIEN	E-GSM 900 band LNA input (differential).
23, 24	RFIAP, RFIAN	GSM 850 band LNA input (differential).
25	XMODE	DCXO or VC-TCXO mode pin enable.
26	XDIV	XOUT frequency select input.
27	AFC	Baseband analog AFC input.
30, 31	XTAL2, XTAL1	Crystal output and input.
32	XEN	XOUT pin enable.

8. Ordering Guide

Part Number	Description	Package Type	Operating Temperature
Si4210-X-GM	Quad-Band GSM/GPRS Transceiver GSM 850, E-GSM 900, DCS 1800, and PCS 1900 bands	QFN (Lead-Free RoHS-Compliant)	–20 to 85 °C
Note: "X" denotes product revision. Add an "R" at the end of the device to denote tape and reel option; 2500 quantity per reel.			

9. Package Outline: Si4210-GM

Figure 19 illustrates the package details for the Si4210-GM. Table 11 lists the values for the dimensions shown in the illustration.The package is lead-free and RoHS-compliant.

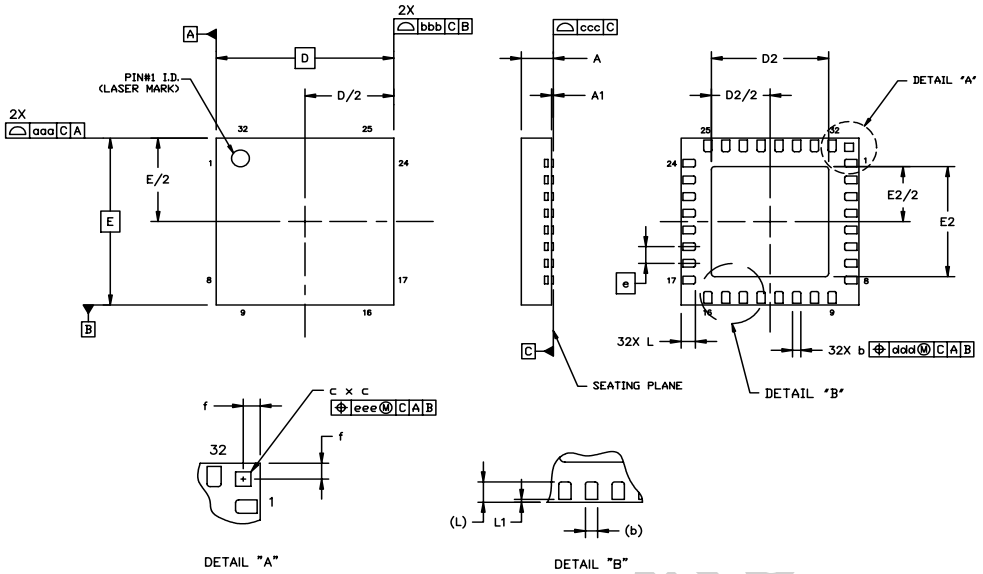


Figure 19. 32-Pin Quad Flat No-lead (QFN)

Table 11. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
c	0.20	0.25	0.30
D		5.00 BSC.	
D2	3.20	3.30	3.40
e		0.50 BSC.	
f		0.28 BSC.	
E		5.00 BSC.	
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.03	0.05	0.08
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHD-2.
3. The pin 1 ID marker (bottom) is for component orientation only and is not to be soldered to the PCB.
4. Package weight is approximately 0.067 g.
5. The mold compound for the package has a flammability rating of UL94-VO.
6. The recommended reflow profile for this package is defined by the JEDEC J-STD-020B Small Body Specification.
7. Lead-free/RoHS-compliant.

10. PCB Land Pattern: Si4210-GM

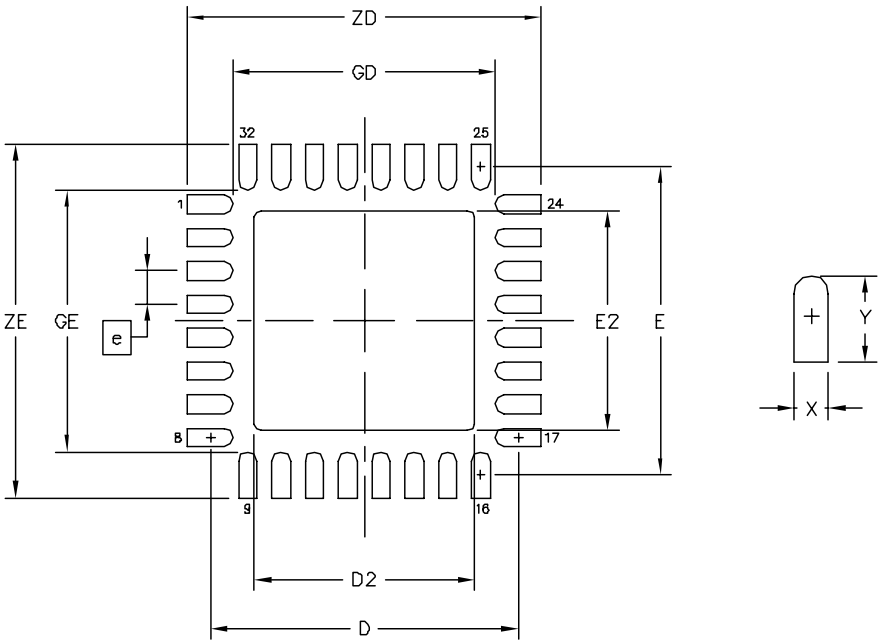


Figure 20. PCB Land Pattern for 32-Pin QFN

Table 12. Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
e	0.50 BSC.	
E	4.62 REF.	
D	4.62 REF.	
E2	3.20	3.40
D2	3.20	3.40
GE	3.93	—
GD	3.93	—
X	—	0.28
Y	0.69 REF.	
ZE	—	5.31
ZD	—	5.31

Notes:

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC). Least material condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum around the pad.

Document Change List

Revision 0.8 to Revision 1.0

- Updated Table 3, “DC Characteristics,” on page 5.
  - Added VDD Supply Current max specifications.
  - Added VIO Supply Current max specifications.
  - Updated I_{VDD}.
  - Updated I_{VIO_PDN}.
- Updated Table 5, “Receiver Characteristics,” on page 8.
  - Added Noise Figure at 25 ºC max specifications.
  - Added Noise Figure at 85 ºC max specifications.
  - Updated Maximum Voltage Gain.
  - Updated Differential Output Offset Voltage
    – Added Note 10.
- Updated Table 6, “Transmitter Characteristics,” on page 11.
  - Updated Phase Error
  - Updated TXVCO Pulling.
  - Updated Powerup Settling Time.
  - Updated note 9.
- Updated Table 7, “Transmitter Carrier Wave Characteristics (CW Mode) for 8-PSK EGPRS[1],” on page 13.
  - Updated note 7.
- Updated Table 8, “Reference Oscillator Characteristics: Digitally-Controlled Crystal Oscillator (DCXO) Mode,” on page 14.
  - Updated Powerup Settling Time.
- Updated "3. Bill of Materials" on page 16.
  - Added additional crystal vendors.
- Updated "6. Register Descriptions" on page 24.
  - Added XOUT Drive Level.
- Updated "9. Package Outline: Si4210-GM" on page 29.
  - Updated Figure 19, “32-Pin Quad Flat No-lead (QFN),” and Table 11, “Package Dimensions,” on page 29 to include pin 1 ID marker dimensions.

Table 13. Aero II Revision History

Data Sheet Revision	Part Revision
0.1	A
0.2	
0.3	
0.4	
0.5	
0.6	B
0.7	C
0.8	
1.0	

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