HERCROM400G2c035

Functional modifications

F751619 versus F741979

CAL022C

V1.0

CALYPSO

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Signature	

HISTORY

Version	Date	Author	Approval manager	Approval date	Notes
1.0	9 – Dec - 2001	Rodolphe Servato	Michel Gac	10-Dec-2001	1

Notes:

1. Creation of the document.

SUMMARY

1. REFERENCE DOCUMENTS

Teamtrack database: H/W bug entry / Calypso

2. INTRODUCTION

This document describes the functional modifications introduced in the HERCROM400G2 device processed in C035 technology versus the HERCROM400G2 device processed in c05 technology. These modifications are corresponding to both design bug corrections and functional improvements.

3. MODULE

3.1 RTC (32K oscillator default gain resistance)

Description:
Change default value of the 32KHz oscillator gain resistor due to techno change from C05 to C035.

Original default value (c05): QUARTZ_REG = 100111 (57K)
New default value (c035): QUARTZ_REG = 101011 (119K)

3.2 MPU

Description:
For MPU Reset all MPU regsiters (Status, Protection Mode, Control, base, start and end-address) are initialized upon any reset (power-on & watchdog/software)

CALYPSO c05 Remember: A reset (watchdog/software) does affect neither the MPU Protection Mode register nor the base, start and end-address registers. Only the MPU Status register is cleared to 0x00 after watchdog/software reset.

3.3 CLKM

3.3.1 Arm clock division

Bug report: BUG01340 / CALYPSO F741979

Description:
the ARM_MCLK clock is no more divisible (it is always at the same frequency as BRIDGE/DMA clock). the CNTL_ARM_DIV register (0xFFFFFD08) become a read-only register (always read "001" that is the current reset value)

the CNTL_ARM_DIV Bits 2-0 definition become:
bits 2-0 Reading these bits always return "001". Writing to them has no effect

3.3.2 Chip dead lock

Bug report: BUG01554 / CALYPSO F741979

Description:
When the deep sleep mode is set (bit set in CLKM) and not executed by the ULPD, then CLKM state_machine locked in SLEEP mode. Only Clear_Deep_Sleep from ULPD or Reset can unlock this state.

CLKM SM switches from SLEEP to WAKE when an interrupt is pending and Deep_Sleep is cleared. Since Deep Sleep mode is not send/executed due to PLL not entering idle mode, the Clear_Deep_Sleep signal is never generated hence locking the CLKM SM.

Solution: hardware fix in Sleep state machine.

3.3.3 Watchdog reset

Bug report: BUG01493 / CALYPSO F741979

Description: The WATCHDOG_RESET bit (bit 3) in the CNT_RST CLKM register is not updated when a watchdog timer interrupt occurs.

Solution: hardware fix

3.4 cDSP Emulator

Bug report: BUG01794 / CALYPSO F741979

Description: When using cDSP emulator, we can't read the data from ROM at page0. It's clock generation problem for ROM module. We can read 1st data from ROM. But we can't read 2nd, 3rd.. data. The clock isn't provided to ROM correctly.

Solution: hardware fix in cDSP subchip

4. CHIP LEVEL

4.1 Identification codes

Description:
New part number for the JTAG identification code: Device-ID is now B496.
Device-Ver = 000

Notes: new JTAG Id generated automatically by Hawkeye .

VHDL model: config_rtl.vhdl

4.2 nCS4 chip select added on spare ball

Description: enhancement consisting in having 5 chip select up to 8 Mbytes :

Add new signal on previously spare PIN :

Ball	Pad	Functional
C11	140	nCS4

To benefit of 8Mbytes address range remember that bit 3 to in register ARM_CONF_REG (FFFE:F006) must be set to 1.

Here below ARM_CONF_REG register table :

(Bit	Description	Reset
0	*Unused*	0
1	0 = Keyboard interface (KBC(0)) 1 = ARM fast interrupt (NFIQ)	0
2	0 = keyboard interface (KBC(1)) 1 = ARM normal interrupt (NIRQ)	0
3	**0 = CS4** **1 = ADD(22)**	**0**
4	0 = Serial clock (BCLKR) 1 = ARMCLK	0
5	0 = TSPACT6 1 = Internal memory chip select nCS6	0
6	0 = I/O(2) 1 = IRQ4	0
7	0 = TSPACT4 1 = nRDYMEM ready signal for external slow device.	0
15:8	*Unused*	0

NOTE: nCS4 MUST BE used with I/O MIF supply voltage 2.7 -> 3.3 V

4.3 Boot ROM

Description:

New MCU BOOT ROM COFF file version 3.0.0 has been implemented.

This ROM code contains the following corrections :

Bug report: BUG01493 / MCU BOOT ROM
BOOT ROM application switches from Supervisor to User mode, which can be a problem for FLASH application or FLASH programmer requiring to have an entry point in Supervisor mode.

Bug report: BUG01712 / MCU BOOT ROM
Interrupt vector in BOOT ROM does not run (configuration 0 at the address 0000:2000). In this configuration, the stack application seems to be corrupted.

4.4 PIN TSP_EN in OFF Mode

Bug report: BUG01795 / CALYPSO F741979

Description: In OFF mode the TSP_EN pins are reset in default configuration which is not in agreement with the register. Now TSP registers with the exception of REG_TSP_SET1, REG_TSP_SET2, REG_TSP_SET3 are frozen as long as TSP reset signal (see TPU register REG_TPU_CTRL) is active (level 1). TSP reset must be released to authorize access to registers.

Solution: hardware fix: Modification on the reset management apply on TSP_EN pins when the IC is in OFF mode.

4.5 Speed working

Description: ARM speed access improvement from 39MHz to 52Mhz and cDSP speed improvement from 91MHz to 104MHz

Solution: Technology C035 and tunning modifications in C28L128 for cDSP speed and all peripheral modules for ARM speed access.