HERCROM400G2c05

Functional modifications

F741979B versus F741979A

CAL021c

V1.0

CALYPSO

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HISTORY

Version	Date	Author	Approval manager	Approval date	Notes
1.0	29-July-02	Rodolphe Servato	Michel Gac	29-July-02	1

Notes:

1. Creation of the document.

SUMMARY

1. REFERENCE DOCUMENTS

Teamtrack database: H/W bug entry / Calypso

2. INTRODUCTION

This document describes the functional modifications introduced in the HERCROM400G2 device processed in C05 Version B technology versus the HERCROM400G2 device processed in c05 technology Version A.
The modifications listed hereafter are only related to the hardware implementation and doesn' t include changes in the DSP ROM code.
These modifications are corresponding to both design bug corrections and functional improvements.

3. MODULE

3.1 GEA

3.1.1 GEA – Bad synchronization

Bug report: BUG00678 / CALYPSO F741979

Description:
The start command generates, internally to the GEA module, an enable-clock signal which is asynchrounous compare to the free-running-clock used as module clock, so a spike is generated and GEA start a bad ciphering process. The CNTL_ARM_DIV Bits 2-0 definition become:
bits 2-0 Reading these bits always return "001". Writing to them has no effect

Solution: Hardware Fix in GEA module

3.1.2 GEA – speed limitation

Bug report: BUG01796 / CALYPSO F741979

Description: To have a right access on GEA the maximum speed access on it by the MCU must be 36.4Mhz.

Solution: Hardware Fix in GEA module

3.2 DMA

Bug report: PRB00716 / CALYPSO F741979

Description: The DMA cannot work with the RIF at a naximum frequency of 34 MHz. This implies the rhea strobe 0 access cannot exceed 34 MHz.

Solution: Hardware Fix

3.3 SPI

Bug report: BUG01606 / CALYPSO F741979

Description: Wrong CLKX_SPI clock duty cycle for baud-rate equal or lower to 6.5MHz For all baud-rates (prescalar value PTV=2,4,8 or 16) except the default (prescalar value PTV=1), the bit clock CLKX_SPI duty-cycle is not 50/50. The clock period is correct versus the PTV value but the duration of the active pulse is always equal to a 13MHz pulse (~76ns). Consequently, the selection of any divider ratio other than 1 doesn't offer any additional time for the external device to sample the transmit data.

Solution: Hardware Fix: Modification of the clock generator to provide a true 50/50 bit clock whatever the divider ratio instead of a gated clock based on the reference 13MHz. This 50/50 clock is used for both the internal transmit and receive logic and as the source for the external clock.

3.4 UART

Bug report: BUG01607 / CALYPSO F741979

Description: Due to internal synchronization problem (nstrobe versus fclk), the generation of the RX_FIFO_LAST_BYTE interrupt can be postponed until the next access to the FIFO. If problem occurs, IIR[2] will be set only when reading the next character which will be not the true last byte (2nd CRC).

Solution: Hardware Fix: RX_LAST_BYTE interrupt and status bit are now resynchronized to get reliable status and interrupt.

3.5 cDSP speed limitation

Description: Due to SPI limitation speed (speed max = 78MHz), speed of cDSP is limited to 78MHz

Solution: Increase speed of SPI up to 78MHz. In consequence speed of cDSP is now 91MHz

3.6 ULPD iT WAKE/UP / IOTA

Bug report: BUG01797 / CALYPSO F741979

Description: The ULPD activate a GSM IT timer on IOTA when he Enables the 13 MHz clock, which is to late, because at this moment IOTA is not ready to deleliver the necessary power.

Solution: Hardware Fix: Generation of the GSM IT timer earlier (IT generation during the ULPD wake up stage).

4. CHIP LEVEL

4.1 Identification codes

Description:
New part number for the JTAG identification code: Device ID = B396.
Device ver = 2
CDSP-ID = 0128

Notes: Device ID generated automatically by Hawkeye.

VHDL model: config_rtl.vhdl

4.2 Floating BUS

Bug report: BUG01402 / CALYPSO F741979

Description: In sleep mode the Data bus should be driven, but on the G2 RevA the bus is floating, indeed he is in entrance.This can bring about a high current consumption, in sleep mode.

Solution: Hardware Fix: On the G2 Rev B a hardware modification is done, which insure the fact that in sleep mode the bus should be driven.

4.3 SPI limitation

Report: detailed SPI interface is reported in technical memo EWTCBU TR005

Description: SPI Interface is limitated at 78MHz due to the SPI Audio system on HERCROM400G2 revA connected to TWL3011 serial bus that has not enough timing margin between VFSRK and VCLKRX signal for frequency up to 78MHz.

Solution: Hardware Fix: add delay on signal VCLKRX

4.4 cDSP Pins

4.4.1 Debug mode (IACKn, TOUT, XF)

Bug report: BUG01060 / CALYPSO F741979

Description: DSP nIACK signal is not available in functional debug mode. This signal should be multiplexed with Flash deep low power (FDP) signal and configured thanks to register FFFE:F004 (DSP configuration).
Moreover the following signals are tied low due to a misconnection during PMT gating modification. The problem is different of HZDO even if this is the same cause.(following signals are not used inside Calypso). Then all of theses are available in PMT mode, but not in functional debug mode:

iackn	(pad : 14	FDP)
tout	(pad : 153	RTS_MODEM)
xf	(pad : 149	CTS_MODEM)

Solution: Hardware Fix

4.4.2 Debug Mode (CLKOUT)

Bug report: BUG01015 / CALYPSO F741979

Description: DSP clock out cannot be checked thanks to the multiplexed pin (with SD_IRDA) when bit 10 of DSP configuration register is set to '1'. In fact, pad SD_IRDA is tied-low when you want to access 'clkout_dsp' in debug mode.

Solution: Hardware Fix: Restore the connection

4.5 BIST

Description: Bist controller was not functional, it means that we can' t test Internal RAM with BIST and we can' t do ram repair using datalogger (part of the BIST)

Solution: Hardware Fix : Generate new BIST with new tool (v3.3) and follow last guidelines concerning CTS balancing. Furthermore, Logic of the bist was scanned.

4.6 PMT Entry Flag

Description: When using test mode like PMT LEAD, PMT ARM… there was no pin reflecting that we are in test mode.

Solution: Hardware modification: When entering in Following test mode:

PMT_LEAD
PMT_ARM
PMT_SCAN

Pin TSPACT_12_5(7) (pin 102) indicate achieving of test mode and goes high

4.7 PAD MAPPING

Description: On silicon two PAD have been swapped, so Ball to PAD bonding was modified:

PAD 177=VSS not connected
PAD 178=D(15) bonded to ball B3

Solution: Hardware Fix: reverse PAD 177 with PAD 178 on device and restore the Ball to PAD bounding:

PAD 177=D(15) bonded to ball B3
PAD 178=VSS bonded to Ball A2

4.8 OSC32K

Bug report: BUG01798 / CALYPSO F741979

Description: When an internal commutation synchronized to 32KHz clock occurs in same time as OSC32Kout is falling, noise added to the signal may generate wrong commutation on the following shaper stage. Glitch may occur on CLK32K_OUT.due to the additional noise.

Solution: Add delay (around 50nS) to the commutation of the logic 32K out cell to move potential switching noise out of the threshold time.