Preliminary ABRIDGED APPROVAL FORM
- Hercrom400G2C035 -

Originator: **Michel Gac**

	Approval	Approval	Approval	Approval	Approval
Name	Michel Gac	Marc Couvrat	Gilles Mouze	Jose Lopez	Jean-Jacques Moureaud
Function	WW Wireless design manager	C.T.O WTCBU	Product engineer	QRA manager	Custom library manager
Date					
Signature					

HISTORY

Version	Date	Author	Approval managers	Approval date	Notes
Ver: 0.1	06/24/02	Rodolphe Servato	Michel Gac	06/24/02	1
Ver 0.2	07/24/02	Rodolphe Servato	Michel Gac	07/24/02	2
Ver 0.3	08/28/02	Rodolphe Servato	Michel Gac	08/28/02	3
Ver 0.4	10/15/02	Rodolphe Servato	Michel Gac	10/15/02	4
Ver 0.5	11/05/02	Cathy Kehon	Michel Gac	11/05/02	5
Ver 0.6	11/19/02	Rodolphe Servato	Michel Gac	11/19/02	6
Ver 0.7	01/20/03	Rodolphe Servato	Michel Gac	01/20/03	7
Ver 0.8	04/14/03	Rodolphe Servato	Eric Balard	04/14/03	8

NOTES :

1. Document creation from CAL000_A C035 v0.9.
2. Remove Memory interface timing table (I/O MIF supply voltage 1.90 -> 2.1 V).
3. Update DC parameters table (VDD min = 1.42V instead of 1.35V)
4. remove reference to F# (F751xxx instead), update general information (packaging)
5. Notification on conditional TMS release.
6. Update CLKTCXO input frequency min (10MHz)
7. Add DSP Rom code version V3606.
8. Update MEMIF timing (tda), remove external memory access time table, update SPI timing.

a) General information:

Parameter	Description		
Technology	1533C035		
Library	GS40		
F number	F751xxx		
Baseset	BF751xxx		
Package (*U*BGA)*	**Qualified**	**Package id**	**Application**
Package (*U*BGA)*	*Yes*	*GHH179*	*Production*
Package (*U*BGA)*	*No (Jan03)*	*GPH205*	*Production*
DSP ROM code	V3416, V3606		
BOOT ROM code	V0300		
ROM protection	Y		

ESD FEATURES

Following our reliability testing performed during HERCROM400G2 C035 qualification, all tests met Texas Instruments (TI) specification.

The following tables detail the ESD performance measured on HERCROM400G2 C035.

Table 1: HERCROM400G2 C035 ESD performance relative to TI requirements

ESD Method	Standard Reference	**HERCROM400G2 C035 Performance**	TI Standard Requirements
Human Body Model	EIA/JEDEC22-A114-A	**2000V**	2000V
Machine Model	EIA/JEDEC22-A115-A	**100V**	None
Charge Device Model	EIA/JEDEC22-C101-A	**750V**	500V

Table 2: Overall summary of the HERCROM400G2 C035 ESD results per voltages

ESD Method	**Voltage**	**Sample Size**	**Results** (failures)
Human Body Model	**±2000 Volts**	**126**	**0**
Machine Model	**±100 Volts**	**126**	**0**
Charge Device Model	**±750 Volts**	**15**	**0**

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b) DC Parameters:

Parameter	Description	Note	Min	Typ	Max	Unit
T_A	Operating temperature	Free air	-40	-	85	°C
VDDS-1	I/O Supply Voltage	Level_shifter	2.5	2.8	3	V
VDDS-2	I/O Supply Voltage	Level_shifter	2.5	2.8	3	V
VDDS-MIF	I/O MIF Supply Voltage	Level_shifter	1.65	2.8	3	V
VDDS-RTC	I/O RTC Supply Voltage	Level_shifter	1.42	2.8	3	V
VDDANG	Analog Supply Voltage		2.5	2.8	3	V
VDDPLL	DPLL Supply Voltage		1.42	1.5	1.65	V
VDD	Core logic Supply Voltage		1.42	1.5	1.65	V
VDD-RTC	RTC logic Supply Voltage		1.42	1.5	1.65	V
Vih	High-level input voltage	Level_shifter	0.7*VDDS[1]	-	VDDS+0.5	V
Vil	Low-level input voltage	Level_shifter	-0.5	-	0.3*VDDS	V
Voh	High-level output voltage	rated current	0.8*VDDS	-		V
Vol	Low-level output voltage	rated current			0.22*VDDS	V
Iol/Ioh	Rated output current	Level_shifter		-		
	Type1	$Voh=VCC_{Min}$ [1]		-	1	mA
		$Vol=VCC_{Max}$ [1]			1	mA
	Type2	$Voh=VCC_{Min}$ [1]		-	2	mA
		$Vol=VCC_{Max}$ [1]			2	mA
	Type3	$Voh=VCC_{Min}$ [1]		-	4	mA
		$Vol=VCC_{Max}$ [1]			4	mA
Iil/Iih	Input leakage current		-1	-	1	uA
Iozl/Iozh	High-Z Output leakage current		-20	-	20	uA

[1] See list of Type1, Type2 and Type3 pins in annex.

c) AC Parameters:

Core Parameters

Parameter	Description	Note	Min	Typ	Max	Unit
ARM7 F_{cyc}	cycle frequency		0	-	52	MHz
C28L128 F_{cycl}	cycle frequency		0	-	104	MHz

Oscillator parameters

Parameter	Description	Note	Min	Typ	Max	Unit
OSC32K	Oscillator input frequency	Sinus inp. [4] [5]		32.768		KHz

[4] http://www.asic.sc.ti.com/~adocs/gs40_aug01/docs/mls/oscillator/os11h1.htm
[5] nominal value according to crystal manufacturer with recommended value for external components

VTCXO general parameters

Parameter	Description	Note	Min	Typ	Max	Unit
CLKTCXO	Input frequency	[4]	10		26	MHz
	Input precision		-12		+12	ppm
	Input amplitude (AC)	[4]	0.5	1	2	V
	Input Impedance	Rin	20	30	65	KOhm
		Cin	6.45	5.85	5	pF

[4] http://www.asic.sc.ti.com/~adocs/gs40_aug01/docs/mls/analog/ck321.htm

VTCXO @13Mhz paramters

Parameter	Description	Note	Min	Typ	Max	Unit
CLKTCXO	Duty cycle		45	50	55	%
	Jitter	1V amplitude			300	Ps

[4] http://www.asic.sc.ti.com/~adocs/gs40_aug01/docs/mls/analog/ck321.htm

VTCXO @26Mhz paramters

Parameter	Description	Note	Min	Typ	Max	Unit
CLKTCXO	Duty cycle		40	50	60	%
	Jitter	1V amplitude			300	Ps

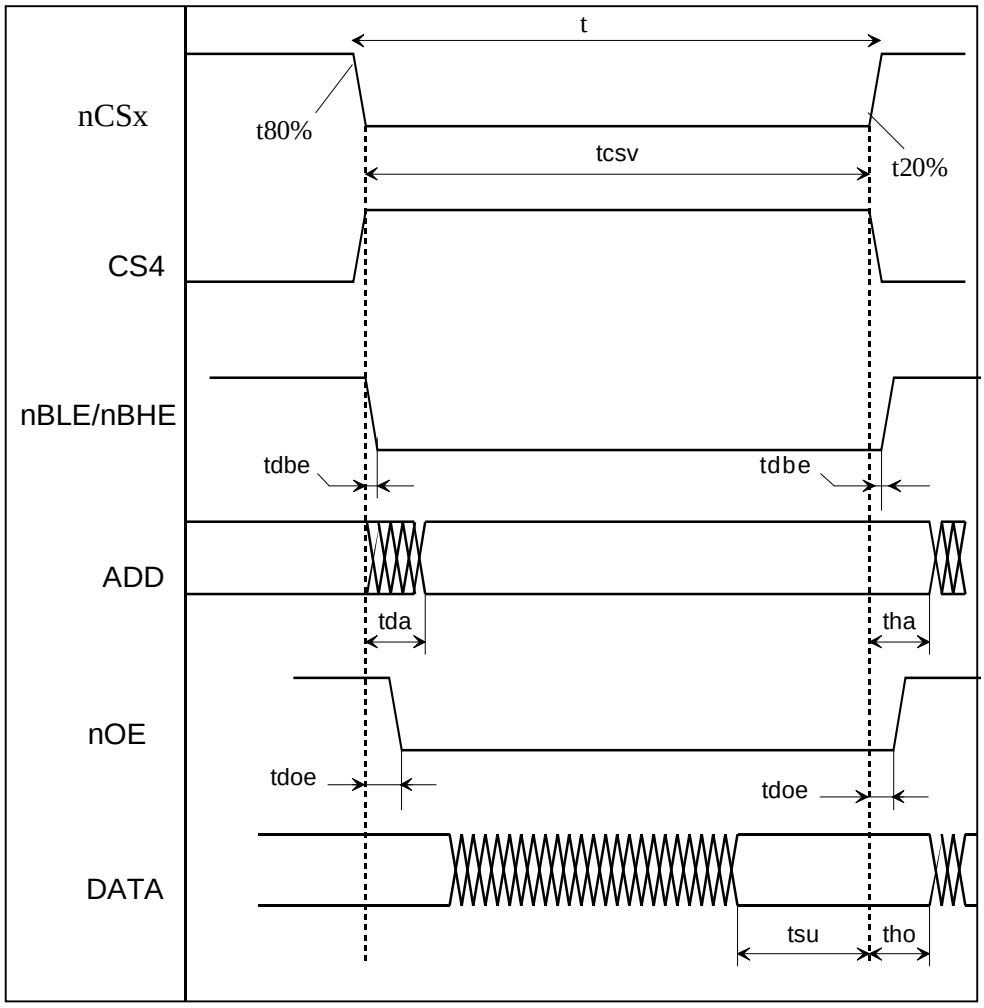
[4] http://www.asic.sc.ti.com/~adocs/gs40_aug01/docs/mls/analog/ck321.htm

32KHz quartz connection

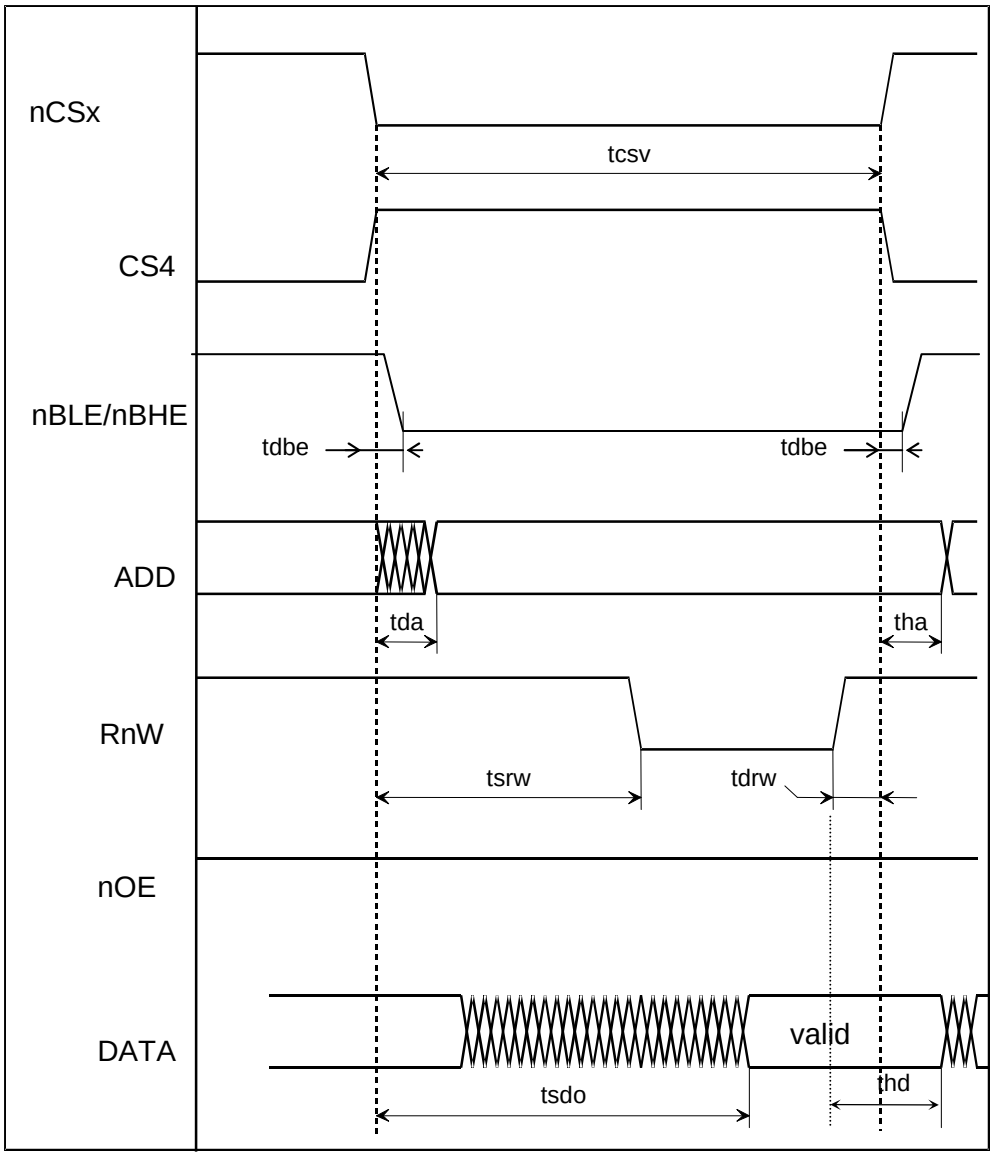
For Details refers to Document:

- **32KHz oscillator PCB recommendation and layout guidelines.**
- **APN0 (Calypso/Iota/Clara System Application Note)**

Read access timing



Write access timing



Memory interface timing table (I/O MIF supply voltage 2.5 -> 3 V)

Name	Function	Min	Max
tcyc	MCU input frequency	-	19.23 ns (52.0 Mhz)
N	Number of wait state	0	31

Name	Function	Min (ns)	Max (ns)
tcsv	Chip Select valid	$tcyc$	$(N+1)\times tcyc$
tda	nCS \ to Address valid	-	3.4
tha	Address hold from nCS /	0	-
tdbe	NBHE, nBLE \ to nCS \	-	0.2
tdoe	nOE \ to nCS \	-	0.5
tsu	Input data setup to nCS /	4.6	-
tho	Input data hold from nCS /	0	-
tsrw	nCS \ to RnW \	$\frac{tcyc}{2} - tdrw$	-
tdrw	RnW / to nCS /	0.9	2.1
tdso	nCS \ to output data valid	-	$(tsrw+7)$
thd	Output data hold from RnW /	0.7	-

***Note**: all timings computed for an external capacitance load of 20pF.*
For larger load capacitance CL then compute timings from table,

$T_{CL} = T_{20pF} + 0.08nS/pF * (CL - 20pF\ )$ *with CL Max= 50pF*

Memory interface timing table (I/O MIF supply voltage 1.65 -> 1.95 V)*:

Name	Function	Min	Max
tcyc	MCU input frequency	-	19.23 ns (52.0 Mhz)
tclk	Internal Mclk \ to nCS /	-	11
N	Number of wait state	0	31

Name	Function	Min (ns)	Max (ns)
tcsv	Chip Select valid	$tcyc$	$(N+1)\times tcyc$
tda	nCS \ to Address valid	-	5.9
tha	Address hold from nCS /	0.5	-
tdbe	nBHE, nBLE \ to nCS \	-	0.2
tdoe	nOE \ to nCS \	-	0.3
tsu	Input data setup to nCS /	4.5	-
tho	Input data hold from nCS /	0	-
tsrw	nCS \ to RnW \	$\frac{tcyc}{2} - tdrw$	-
tdrw	RnW / to nCS /	0.9	2.3
tdso	nCS \ to output data valid	-	$(tsrw+7)$
thd	Output data hold from RnW /	0.2	-

***Note**: all timings computed for an external capacitance load of 20pF.*
For larger load capacitance CL then compute timings from table,

$$T_{CL} = T_{20pF} + 0.08nS/pF * (CL - 20pF) \text{ with CL Max= 30pF}$$

*For using 1.65V external memory on CALYPSO with IOTA ABB see CAL000.doc for connection with IOTA

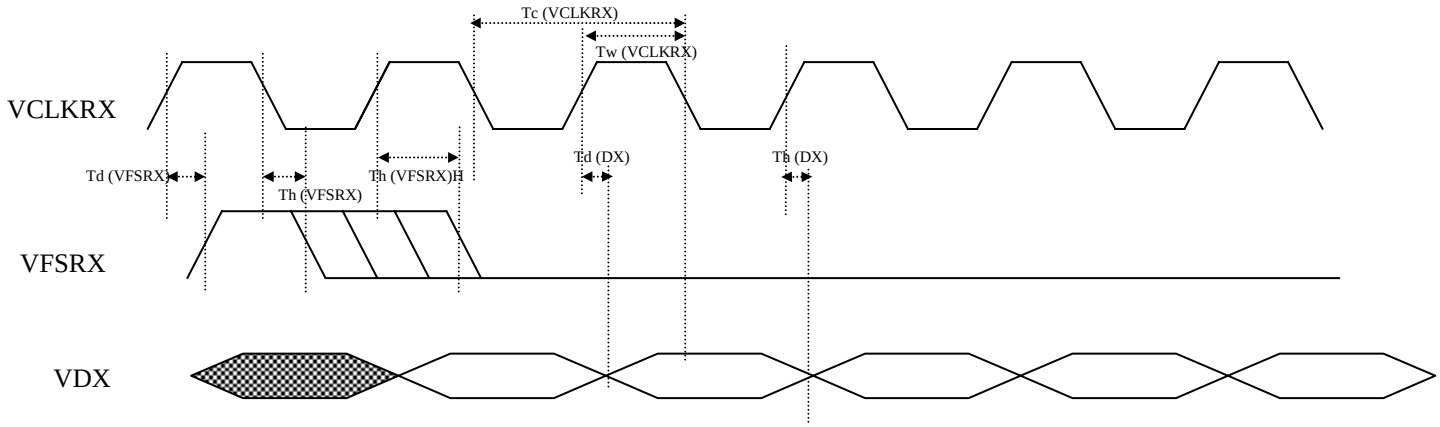
NOTE: nCS4 can't be use with this supply voltage

External memory access time vs MCU clock (examples)

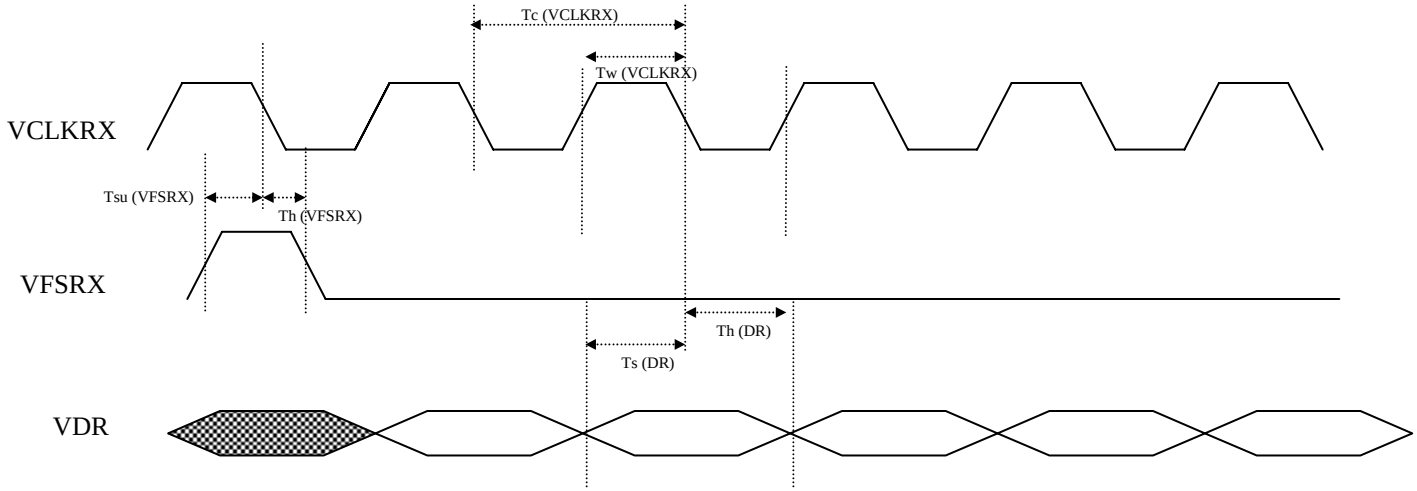
The formula for to calculate access time is in our case:

$$(tcsv - tsu - tda) = Tacc \quad (N+1) \times tcyc - tsu - tda = Tacc$$

Serial port transmit timing



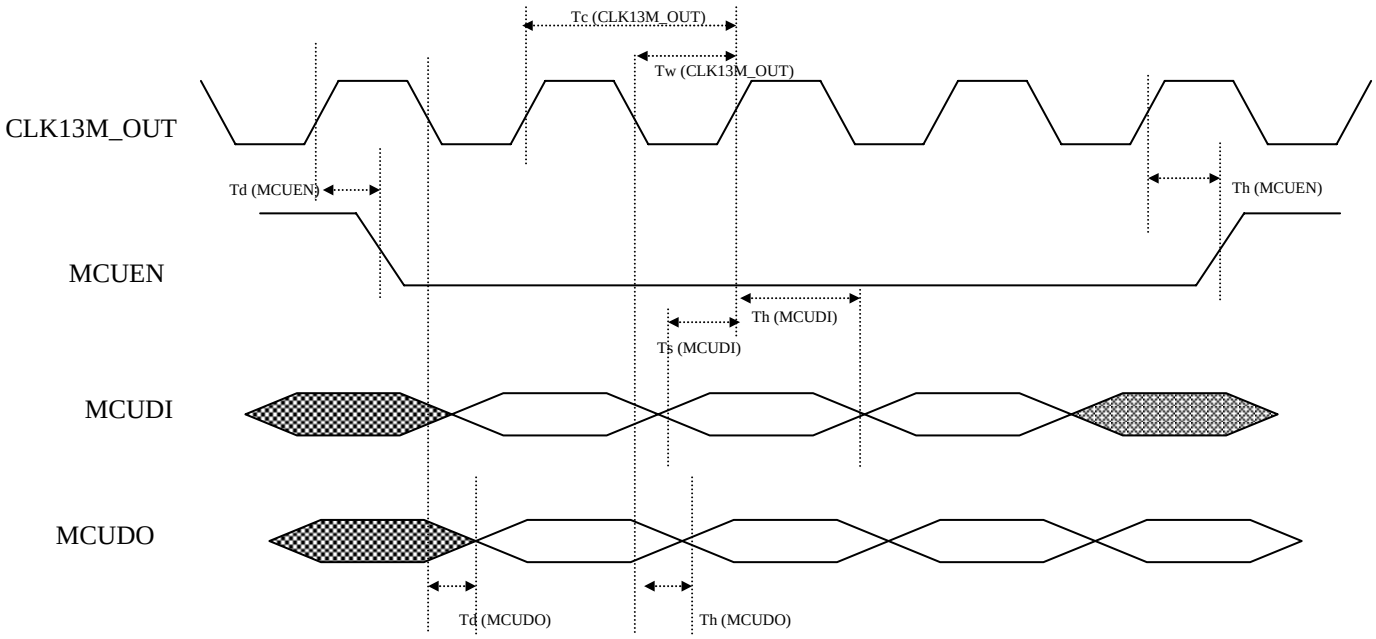
Serial port receive timing



SPI timing table

Parameter	Min	Max	Unit
T : cDSP clock period	9.6		Ns
Tw(VCLKRX) Pulse duration, serial port clock	3T		Ns
Tc(VCLKRX) Cycle time, serial port clock	6T		Ns
Td (DX) Delay time, Data valid after VCLKRX rising		25	Ns
Th(DX) Hold time, Data valid after VCLKRX rising	-5		Ns
Td(VFSRX) Delay time, VFSRX after VCLKRX rising edge		T+2.5	Ns
Th(VFSRX) Hold time, VFSRX after VCLKRX falling edge	10		Ns
Th(VFSRX)H hold time, VFSRX after VCLKRX rising edge		T+2.5	ns
Ts (DR) Setup, Data valid after VCLKRX rising	15		ns
Th(DR) Hold time, Data valid after VCLKRX rising	10		Ns
Tsu(VFSRX) Setup time, VFSRX before VCLKRX falling edge	15		Ns

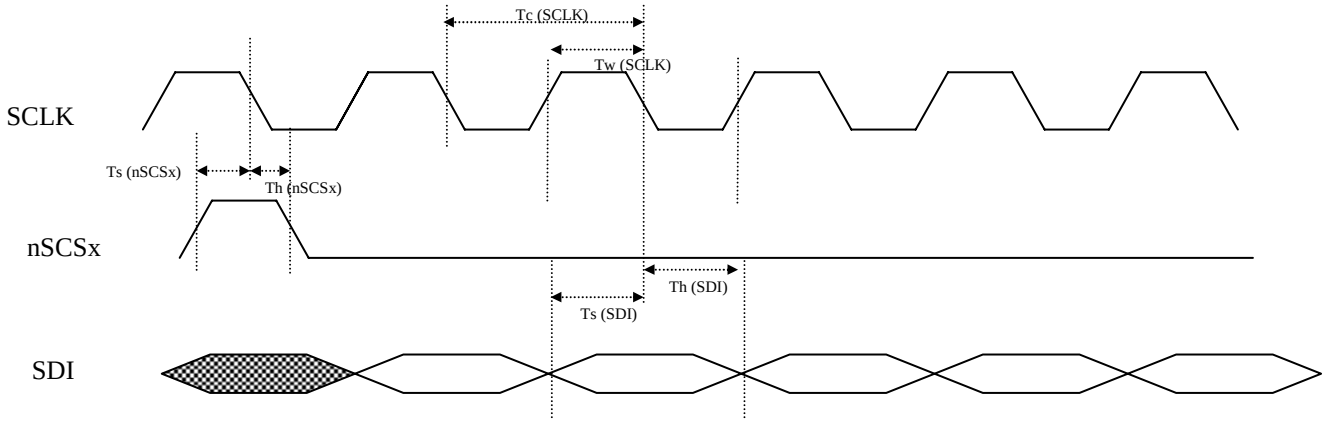
ARM Serial port



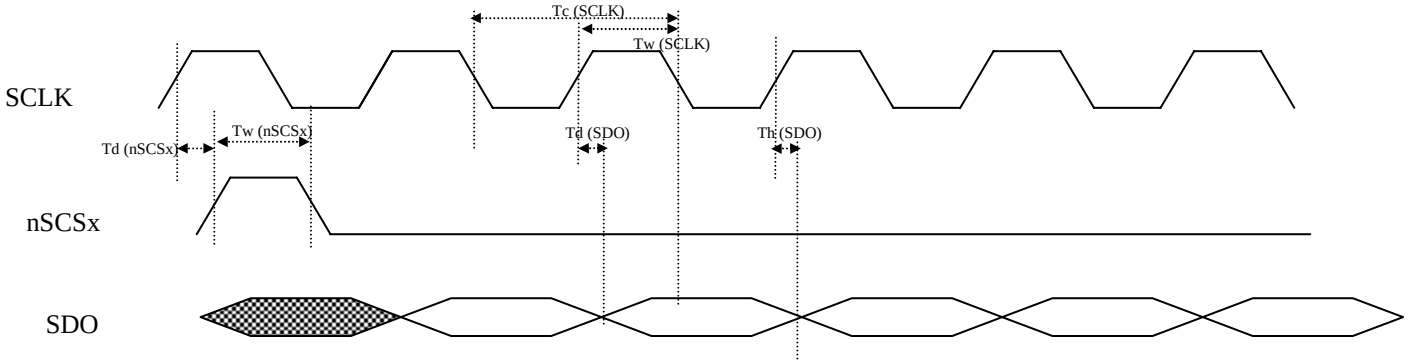
ARM Serial port timing table

Parameter	Min	Max	Unit
Tw(CLK13M_OUT) Pulse duration, serial port clock	38		Ns
Tc(CLK13M_OUT) Cycle time, serial port clock	77		Ns
Td(MCUDO) Delay time, Data valid after CLK falling		8.2	Ns
Th(MCUDO) Hold time, Data valid after CLK falling	0		Ns
Td(MCUEN) Delay time, EN after CLK rising edge		7.5	Ns
Th(MCUEN) Hold time, EN after CLK rising edge	0		Ns
Ts(MCUDI) Setup, Data valid before CLK rising	7.5		Ns
Th(MCUDI) Hold time, Data valid after CLK rising	2.5		Ns

MICROWIRE port receive timing



MICROWIRE port transmit timing

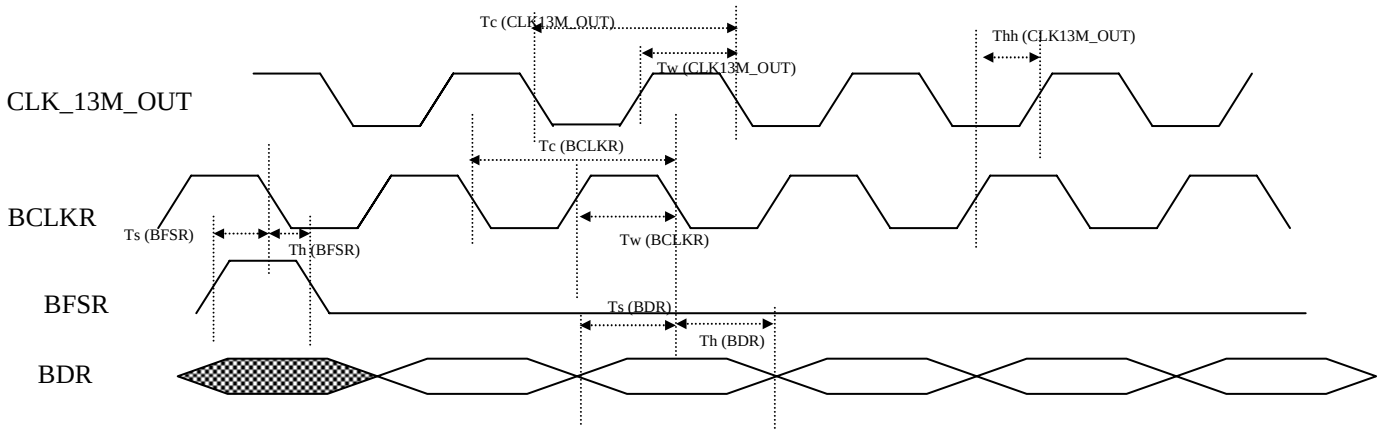


MICROWIRE port timing table

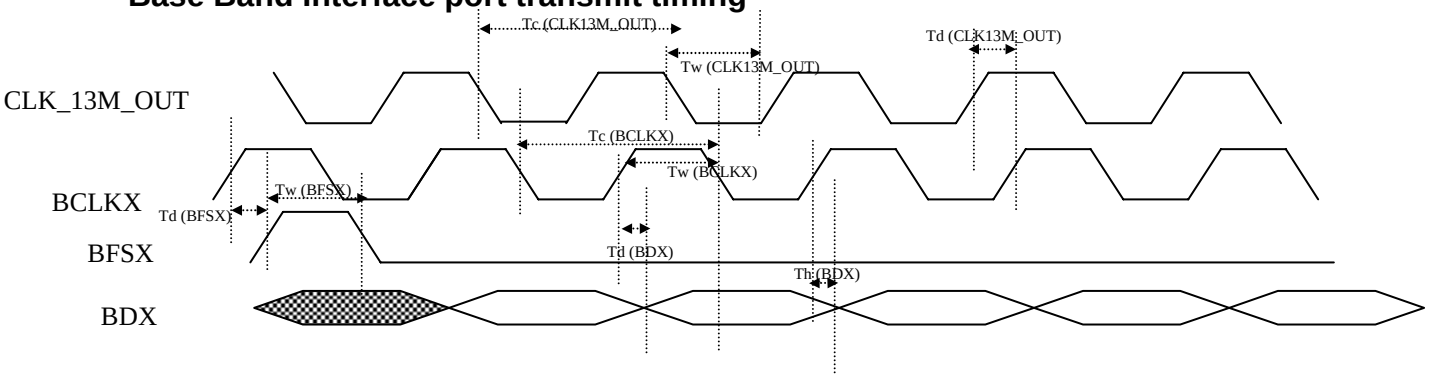
Parameter	Min	Max	Unit
Tw(SCLK) Pulse duration, serial port clock	154	*	Ns
Tc(SCLK) Cycle time, serial port clock	308	*	Ns
Td(SDO) Delay time, Data valid after CLK rising		10	Ns
Th(SDO) Hold time, Data valid after CLK rising	0		Ns
Tw(nSCSx) Pulse duration, EN port	154		Ns
Td(nSCSx) Delay time, EN after CLK rising edge		10	Ns
Ts(SDI) Setup, Data valid before CLK falling	15		Ns
Th(SDI) Hold time, Data valid after CLK falling	15		Ns
Ts(nSCSx) setup time, EN before CLK falling edge	10		Ns
Th(nSCSx) Hold time, EN after CLK falling edge	10		Ns

*depending on peripheral Register programmation

Base Band Interface port receive timing



Base Band Interface port transmit timing

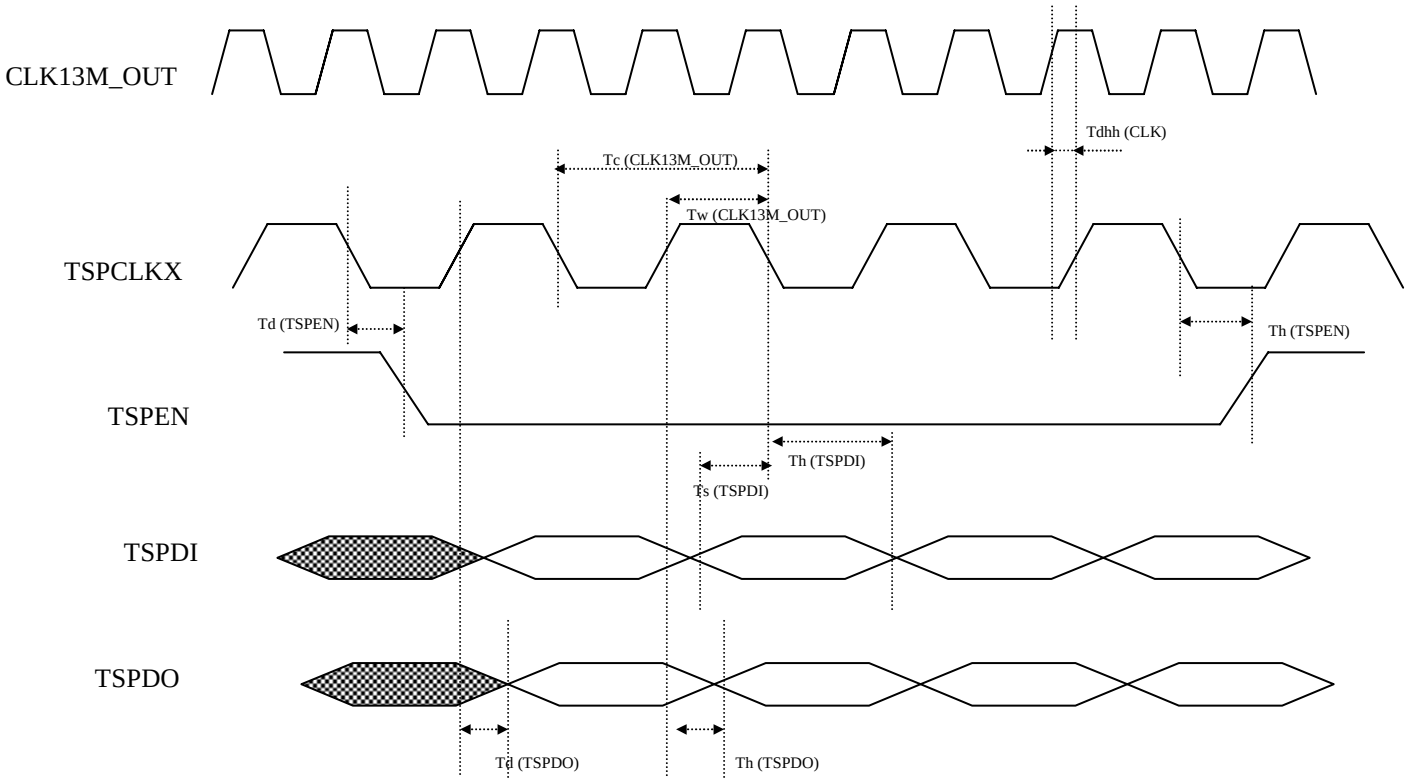


Base Band Interface port timing table

Parameter	Min	Max	Unit
Tw(BCLKR) Pulse duration, serial port clock	38	*	Ns
Tc(BCLKR) Cycle time, serial port clock	77	*	Ns
Tc(CLK_13M_OUT) Cycle time	77		Ns
Td(CLK_13M_OUT) Delay time		5.0	Ns
Thh(CLK_13M_OUT) Delay time**		3.2	Ns
** CLK_13M_OUT after BCLKR_INT			
Ts(BDR) Setup, Data valid before CLK falling	15		Ns
Th(BDR) Hold time, Data valid after CLK falling	8		Ns
Ts(BFSR) setup time, EN before CLK falling edge	10		Ns
Th(BFSR) Hold time, EN after CLK falling edge	8		Ns
Tw(BCLKX) Pulse duration, serial port clock	38	*	Ns
Tc(BCLKX) Cycle time, serial port clock	77	*	Ns
Td (BDX) Delay time, Data valid after CLK rising		12	Ns
Th(BDX) Hold time, Data valid after CLK rising	0		Ns
Td(BFSX) Delay time, EN after CLK rising edge		10	Ns
Tw(BFSX) Pulse duration, EN port	38		Ns

*depending on peripheral Register programmation

TPU serial port

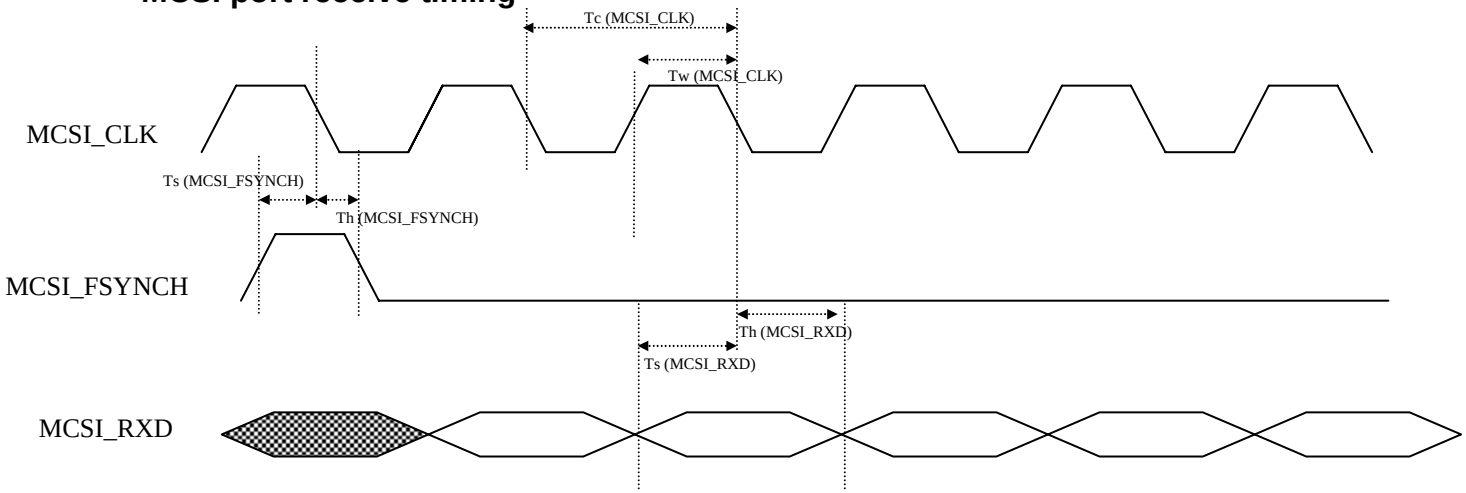


TPU serial port timing table

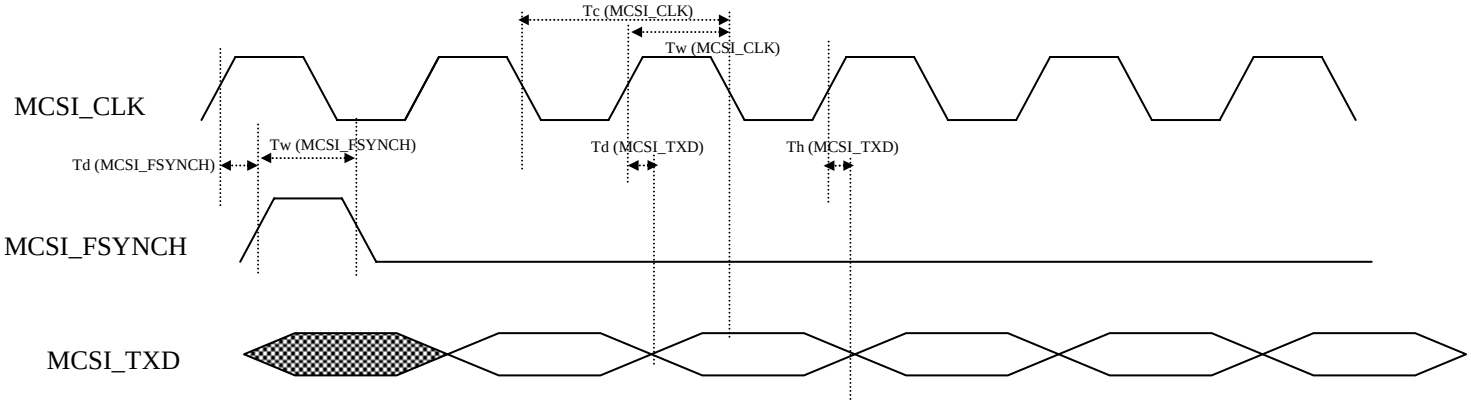
Parameter	Min	Max	Unit
Tw(TSPCLKX) Pulse duration, serial port clock	77	*	Ns
Tc(TSPCLKX) Cycle time, serial port clock	154	*	Ns
Tdhh(CLK) Delay time,TSPCLKX rising after CLK_13M_OUT rising		0.9	Ns
Td (TSPDO) Delay time, Data valid after CLK rising		10	Ns
Th(TSPDO) Hold time, Data valid after CLK rising	0		Ns
Ts (TSPDI) Setup, Data valid before CLK falling	15		Ns
Th(TSPDI) Hold time, Data valid after CLK falling	15		Ns
Td(TSPEN) Delay time, EN after CLK falling edge		10	Ns
Th(TSPEN) Hold time, EN after CLK falling edge	0		Ns

*depending on peripheral Register programmation

MCSI port receive timing



MCSI port transmit timing

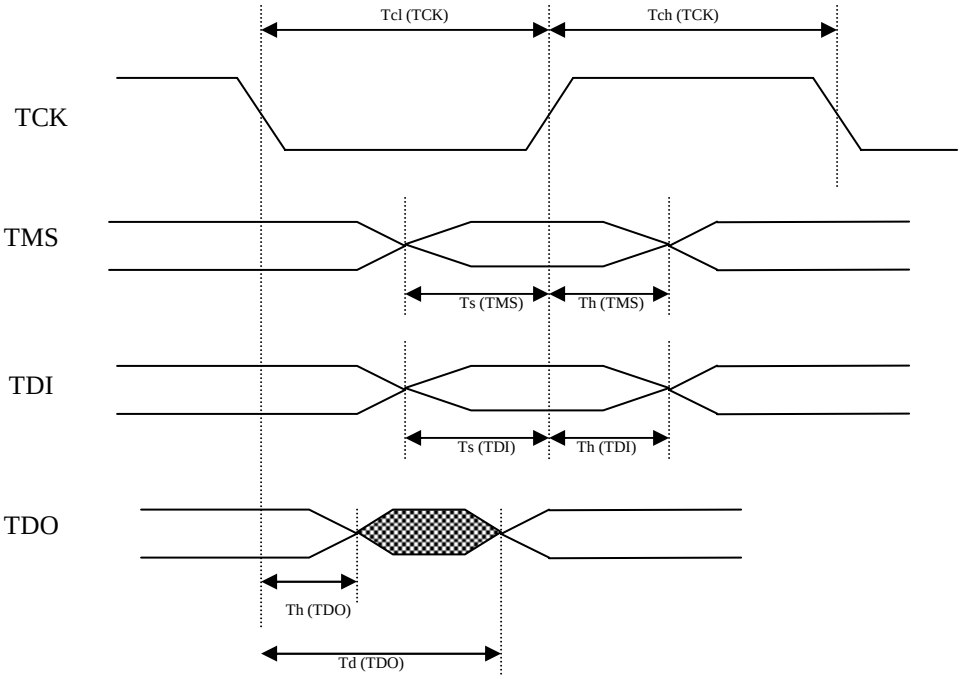


MCSI port timing table

Parameter	Min	Max	Unit
Tw(MCSI_CLK) Pulse duration, serial port clock	77	*	Ns
Tc(MCSI_CLK) Cycle time, serial port clock	154	*	Ns
Td (MCSI_TXD) Delay time, Data valid after CLK rising		10	Ns
Th(MCSI_TXD) Hold time, Data valid after CLK rising	0		Ns
Td(MCSI_FSYNCH) Delay time, EN after CLK rising edge		10	Ns
Tw(MCSI_FSYNCH) Pulse duration, EN port	77		Ns
Ts (MCSI_RXD) Setup, Data valid before CLK falling	15		Ns
Th(MCSI_RXD) Hold time, Data valid after CLK falling	15		Ns
Ts(MCSI_FSYNCH) setup time, EN before CLK falling edge	10		Ns
Th(MCSI_FSYNCH) Hold time, EN after CLK falling edge	10		Ns

*depending on peripheral Register programmation

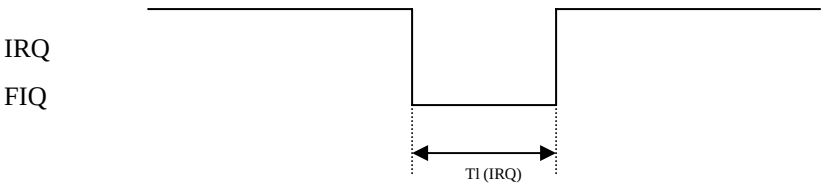
JTAG interface



Parameter	Min	Max	Unit
Tcl(TCK) TCK low period	50		Ns
Tch(TCK) TCK high period	50		Ns

Ts(TMS) Setup time TMS	15		Ns
Th(TMS) Hold time TMS	15		Ns
Ts(TDI) Setup time TMS	15		Ns
Th(TDI) Hold time TMS	15		Ns
Td(TDO) Delay time valid TDO		25	Ns
Th(TDO) Hold time TDO	0		Ns

Interrupt



Parameter	Min	Max	Unit
Tl(IRQ) Pulse duration in functional mode	77		Ns

ANNEXE 1

Level shifter Type 1 : OUO231
Level shifter Type 2 : OUI431, OUK 431, OUO431
Level shifter Type 3 : OUI831, OUK831