TWL3014

Specification

PRELIMINARY

Ver 2.0

Department: MSLP Design / Wireless Communication Systems

	Originator	Originator	Approval	Approval	Quality
Name	Jean-Christophe JIGUET	Lorenzo INDIANI	Philippe PERNEY	Marc COUVRAT	Deborah ROUCHOUSE
Date	7-mar-2001				
Signature					

HISTORY

Version	Date	Author	Notes
Ver: 1.0	23-June-2000	Jean-Christophe JIGUET	1
Ver: 1.2	07 -mar-2001	Jean-Christophe JIGUET	2,3,4
Ver: 2.0	14 -sep-2001	Jean-Christophe JIGUET	5, - ,17

Notes :

(1) Original draft
(2) Update VRPC state machine , state and timing
(3) Add quiescent consumption in BACKUP, OFF, SLEEP, ACTIV mode
(4) Update according to PG1.0 functionnality
(5) Change VRDBB , VRRTC output value (1.8-1.5-1.3 V)
(6) Change max ESR for external regulator output
(7) Update MAX current consumption in ACTIV & SLEEP mode
(8) Change BaseBand downlink TSNR (downto -82 db)
(9) Change LDO max voltage output value in sleep mode
(10) Update Min & Max values for BUL I&Q common mode voltage VVMID
(11) Update ADIN1 & ADIN2 Min & Max output current values
(12) Remove RSU check in VRPC
(13) Add POP cancelation function in VOICE output
(14) Add Sleep mode on VRABB
(15) Update digital input and output electrical characteristics
(16) Add TAP private instructions
(17) Modify bit orders BCCTL1 , BCIONF, BBCTL in register cross-reference

TABLE OF CONTENTS

1. REFERENCE DOCUMENTS

2. GLOSSARY

ABB	**A**nalog **B**ase**B**and chip, part of the TI solution
ACD	**A**uxiliary **D**rivers.
ADAC	**A**uxiliary **DAC**.
AFC	**A**utomatic **F**requency **C**ontrol.
APC	**A**utomatic **P**ower **C**ontrol.
BBC	**B**ase Band **C**odec.
BBS	**B**ackup **B**attery **S**witch
BCC	**B**attery **C**harger **C**ontrol.
BDL	**B**ase band **D**own**L**ink.
BSP	**B**ase Band **S**erial **P**ort.
BUL	**B**ase band **U**p**L**ink.
CKG	**C**lock **G**enerator.
DBB	**D**igital **B**ase**B**and chip , part of the TI solution
IBC	**I**nterna l **B**us **C**ontroller.
JTAG	**J**oined **T**est **A**ction **G**roup.
LDO	**L**ow **D**rop **O**ut regulator.
MADC	**M**onitoring **A**nalog to **D**igital **C**onverter.
SIM	**S**ubscriber **I**dentity **M**odule
TAP	**T**est **A**ccess **P**ort.
TPU	**T**ime **P**rocessing **U**nit.
TSP	**T**ime **S**erial **P**ort.
USP	■ controller **S**erial **P**ort.
VBC	**V**oice **B**and **C**odec.
VREG	**V**oltage **Reg**ulation.
VRPC	**V**oltage **R**eference / **P**ower **C**ontrol.
VSP	**V**oice **S**erial **P**ort

3. FUNCTIONAL DESCRIPTION

3.1 General description

TWL3014 is an analog baseband device (ABB) which, together with a digital baseband device (DBB), is part of a TI DSP solution intended for digital cellular telephone applications including GSM 900, DCS 1800 and PCS 1900 standards (dual band capability).

The TWL3014 device along with TWL3015 also forms the analog baseband solution for dual-mode (GSM / WCDMA) applications.

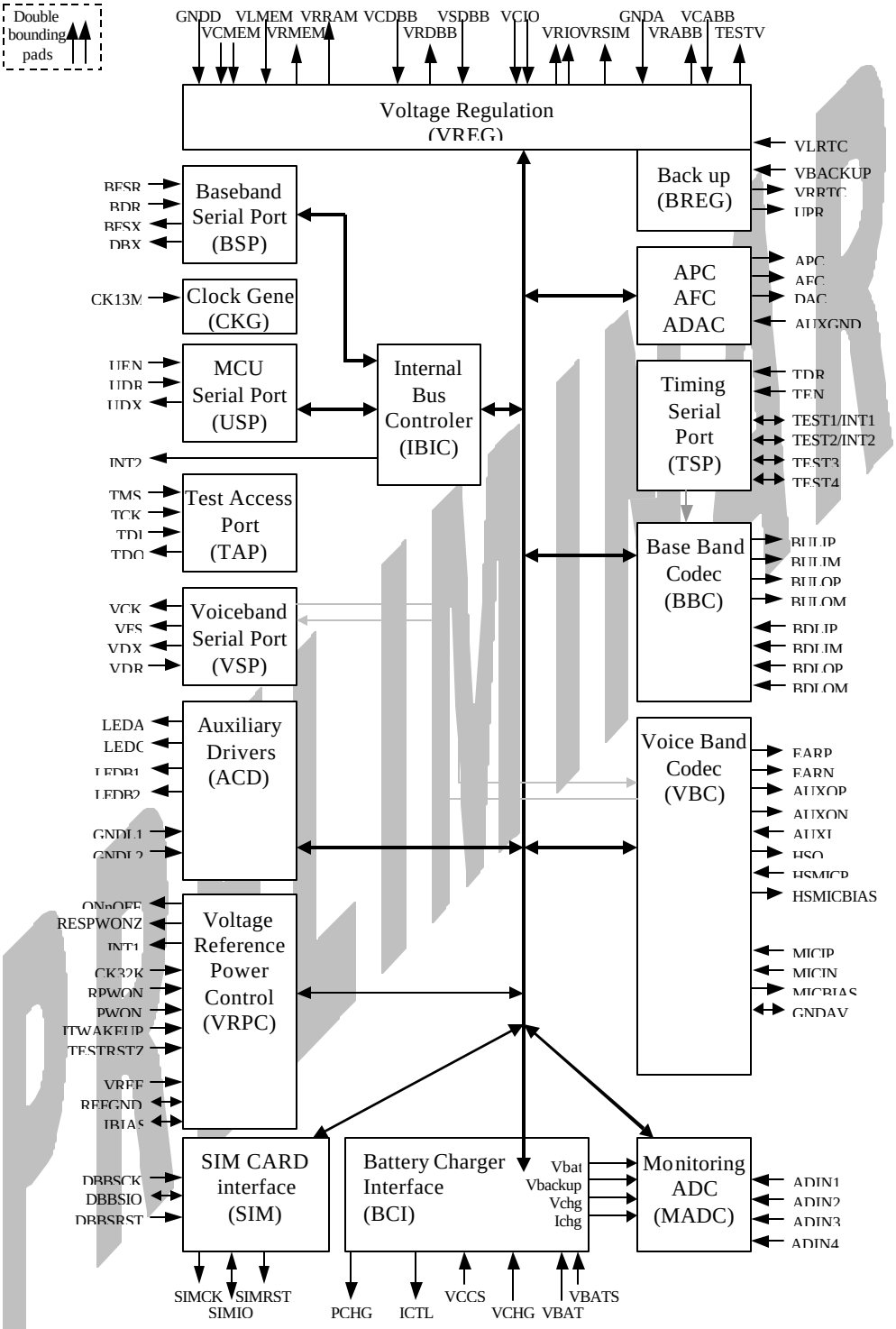
It includes a complete set of baseband functions to perform the interface and processing of voice signals, interface and processing of baseband in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis.

ABB interfaces with the digital baseband device through a set of digital interfaces dedicated to the main functions of DBB, a baseband serial port (BSP) and a voiceband serial port (VSP) to communicate with the DSP core (LEAD), a micro-controller serial port to communicate with the micro-controller core and a time serial port (TSP) to communicate with the time processing unit (TPU) for real time control.

ABB meets JTAG testability standard (IEEE Std 1131.1-1990) through a standard test access port (TAP) and boundary scan.

ABB includes also on chip voltage reference, under voltage detection and power-on reset circuits.

3.2 ABB block diagram



3.3 Caracteristics

3.3.1 Absolute maximum over operating free-air temperature range (Unless otherwise noted) ①

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage range VCHG	②	-0.3		6.8	V
Supply voltage range VBAT, VCx	②	-0.3		6.8	V
Voltage on input pins(par type)	②	-0.3		Vdd+0.3	V
Peak output current at pin VRDBB				240	mA
Peak output current at pin VRMEM				240	mA
Peak output current at pin VRIO				100	mA
Peak output current at pin VRA BB				150	mA
Peak output current at pin VRRTC				20	uA
Peak output current on all other pins		-5.0		5.0	mA
Maximum junction temperature Tj				150	°C
Storage temperature range Tstg		-65		150	°C

① Stresses beyond those listed under "absolute maximum ratings" may cause permanent damages to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

② Voltage specified with respect to VSS (pins GNDD, GNDA, REFGND, GNDAV, GNDL)

Dissipation rating table

Package	TA < 25°C POWER RATING	DERATING FACTOR ABOVE TA=25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING
GGM	2083 mW	16.7 mW/°C	1333 mW	1083 mW

Recommended operating conditions

Parameter	Conditions	Min	Typ	Max	Units
Main battery supply voltage, VCx		3.0	3.6	5.5	V
Backup Battery supply voltage VBACKUP		2.2①	3.0	3.2	V
Charger supply voltage VCHG		4.8		6.8	V
Supply voltage on GNDD, GNDA, GNDAV, REFGND, GNDL (**VSS**)			0		V
Operating temperature range TA		-25		85	°C

① Min level to keep device above POR level

3.3.2 Electrical characteristics digital inputs and outputs

Over recommended operating free-air temperature range (unless otherwise noted)

Digital inputs and outputs (except SIMIO, SIMRST, SIMCK)

Parameter	Pins	Conditions	Min	Typ	Max	Units
Low level output voltage, VOL	ONNOFF,RESPWONZ	Iol = 10ua			0.2 * VRRTC	V
	Other outputs	Iol = 1ma			0.2 * VRIO	
High level output voltage, VOH	ONNOFF,RESPWONZ	Ioh = -10ua	0.8 * VRRTC			V
	Other outputs	Ioh = -1ma	0.8 * VRIO			
Low level in put voltage, VIL	PWON, RPWON				0.3 * VBAT	V
	TESTRSTZ				0.3 * UPR	
	ITWAKEUP, CK32K				0.3 * VRRTC	
	Other inputs				0.3 * VRIO	
High level input voltage, VIH	PWON, RPWON		0.7 * VBAT			V
	TESTRESETZ		0.7 * UPR			
	ITWAKEUP, CK32K		0.7 * VRRTC			
	Other inputs		0.7*VRIO			
Low level input current , IIL	Standard and pull-down inputs	Vi = 0V	-1			uA
	Pull-up inputs		-20			
High level input current , IIH	Standard and pull-up inputs				1	uA
	Pull-down inputs				20	
Capacitor output load	All outputs				25	pF

Digital inputs and outputs (only SIMIO, SIMRST, SIMCK)

Pin	Parameters	Conditions	Min	Typ	Max	Units
SIMCK	VOH	SIMLEN=1, VRIO & VRSIM are set , Ioh = 20ua	0.7 * VRSIM			V
	VOL	SIMLEN=1 VRIO & VRSIM are set , Iol = -20ua			0.2 * VRSIM	
	VOL	SIMLEN=0 VRIO & VRSIM are not set , Iol = -1ma			0.2 * VRSIM	
SIMRST	VOH	SIMLEN=1, VRIO & VRSIM are set , Ioh = 200ua	0.8 * VRSIM			V
	VOL	SIMLEN=1 VRIO & VRSIM are set , Iol = -200ua			0.2 * VRSIM	
	VOL	SIMLEN=0 VRIO & VRSIM are not set , Iol = -1ma			0.2 * VRSIM	
SIMIO	VOH	SIMLEN=1, DBBIO=VRIO VRIO & VRSIM are set , Ioh = 20ua	0.7 * VRSIM			V

	VOL	SIMLEN=1 , DBBIO= GNDD VRIO & VRSIM are set , Iol = -1ma			0.3	
Capacitor load	All outputs				30	pF

3.4 Blocks description

3.4.1 Voiceband Codec (VBC)

The voice coder/decoder (codec) circuit processes analog audio components in the uplink path and transmits this signal to DSP speech coder through the voice serial port (VSP). In the downlink path the codec converts the digital samples of speech data received form the DSP via the voice serial port into analog audio signal.

Additional functions such as programmable gain, volume control and side-tone are performed into the voice band codec.

UPLINK PATH

Global characteristics

Parameter	Conditions	Min	Typ	Max	Units
Maximum Input Range (MICIP-MICIN)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0dB)		32.5		mVrms
Nominal Ref.level (MICIP-MICIN)			-10		dBm0
Differential Input Resistance (MICIP-MICIN)			36		KΩ
Micro amplifier gain (MIC)			25.6		dB
Parameter	Conditions	Min	Typ	Max	Units
Maximum Input Range (HSMIC)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0dB)		78		mVrms
Nominal Ref. level (HSMIC)			-10		dBm0
Micro amplifier gain (HSMIC)			18		dB
Parameter	Conditions	Min	Typ	Max	Units
Maximum Input Range (AUXI)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0dB)		365		mVrms
Nominal Reference level at AUXI			-10		dBm0
Auxiliary gain amplifier	VBDFAUXG = 0		4.6		dB
	VBDFAUXG = 1		28.2		dB
Input Resistance at AUXI	VBDFAUXG = 0	100	170	245	KΩ
Parameter	Conditions	Min	Typ	Max	Units
DC level at MICBIAS	MICBIAS=0		2.0		Volt
	MICBIAS=1		2.5		Volt
DC level at HSMICBIAS	MICBIAS=0		2.0		Volt
	MICBIAS=1		2.5		Volt
Current capability at MICBIAS		0		2	mA
Current capability at HSMICBIAS		0		2	mA

The MICBIAS and HSMICBIAS outputs are multipexed, only one is avalaible at the same time.
The AUXI and HSMIC inputs are multiplexed.

Parameter	Conditions	Min	Typ	Max	Units
PGA absolute gain	VULPGA code 10000 -12dB	-12.5	-12	-11.5	dB
	VULPGA code 10111 -11dB	-11.5	-11	-10.5	dB
	VULPGA code 11000 -10dB	-10.5	-10	-9.5	dB
	VULPGA code 11001 -9dB	-9.5	-9	-8.5	dB
	VULPGA code 11010 -8dB	-8.5	-8	-7.5	dB
	VULPGA code 11011 -7dB	-7.5	-7	-6.5	dB
	VULPGA code 00000 -6dB	-6.5	-6	-5.5	dB
	VULPGA code 00001 -5dB	-5.5	-5	-4.5	dB
	VULPGA code 00010 -4dB	-4.5	-4	-3.5	dB
	VULPGA code 00011 -3dB	-3.5	-3	-2.5	dB
	VULPGA code 00100 -2dB	-2.5	-2	-1.5	dB
	VULPGA code 00101 -1dB	-1.5	-1	-.5	dB
	VULPGA code 00110 0dB	-0.5	0	0.5	dB
	VULPGA code 00111 1dB	0.5	1	1.5	dB
	VULPGA code 01000 2dB	1.5	2	2.5	dB
	VULPGA code 01001 3dB	2.5	3	3.5	dB
	VULPGA code 01010 4dB	3.5	4	4.5	dB
	VULPGA code 01011 5dB	4.5	5	5.5	dB
	VULPGA code 01100 6dB	5.5	6	6.5	dB
	VULPGA code 10001 7dB	6.5	7	7.5	dB
	VULPGA code 10010 8dB	7.5	8	8.5	dB
	VULPGA code 10011 9dB	8.5	9	9.5	dB
	VULPGA code 10100 10dB	9.5	10	10.5	dB
	VULPGA code 10101 11dB	10.5	11	11.5	dB
	VULPGA code 10110 12dB	11.5	12	12.5	dB
	RESET value and others cases	-6.5	-6	-5.5	dB
Power supply rejection	0Hz—100kHz		40		dB

Frequency response

Parameter	Conditions	Min	Typ	Max	Units
Frequency Response Relative to reference gain at 1kHz	<= 100 Hz			-20	dB
	100 Hz to 200 Hz			-10	dB
	300 Hz to 400 Hz	-2	0	+1	dB
	400 Hz to 3300 Hz	-1	0	+1	dB
	3300 Hz to 3400 Hz	-2	0	+1	dB
	4000 Hz to 4600 Hz			-17	dB
	4600 Hz to 6000 Hz			-40	dB
	>= 6000 Hz			-45	dB

Psophometric SNR

Parameter	Conditions	Min	Typ	Max	Units
Psophometric SNR	3 dBm0	35			dB
	0 dBm0	40			dB
	-5dBm0	42			dB
	-10dBm0	45			dB
	-20dBm0	42			dB
	-30dBm0	40			dB
	-40dBm0	30			dB
	-45dBm0	25			dBm0
Maximum idle channel noise				-72	dB
Crosstalk with the downlink path	Downlink path loaded at 33 Ohms			-66	

Gain characteristics

Parameter	Conditions	Min	Typ	Max	Units
Absolute gain error	at 0 dBm0 and 1kHhz	-1		1	dB
	at -10dBm0 and 1kHz	-11		-9	
Gain Tracking Error Relative to –10dBm0 reference level	3dBm0	-0.25		0.25	dB
	0dBm0	-0.25		0.25	dB
	-5dBm0	-0.25		0.25	dB
	-20dBm0	-0.25		0.25	dB
	-30dBm0	-0.25		0.25	dB
	-40dBm0	-0.35		0.35	dB
	-45dBm0	-0.50		0.50	dB
Number of meaningful output bits	PGA set to 0 dB		13		Bit

DOWNLINK PATH

Output load conditions

Parameter	Conditions	Min	Typ	Max	Units
Differential Minimum resistive load at (EARP-EARN) : R//	Output swing 3.9 Vpp Output swing 1.5 Vpp		120 33		Ohms Ohms
Differential Maximum capacitor load at (EARP-EARN): C//				100	pF
Common Mode Minimum resistive load at EARP or EARN			200 K		Ω
Common Mode Maximum capacitor load at EARP or EARN				10	pF
Parameter	Conditions	Min	Typ	Max	Units
Minimum output resistive load at (HSO) : R//			32		Ohms
Maximum capacitor load at (HSO): C//				100	pF
Coupling capacitor load at (HSO): C			22		uF
Parameter	Conditions	Min	Typ	Max	Units
Differential Minimum output resistive load at (AUXOP-AUXON) : R//		1	1.2		kOhms
Differential Maximum capacitor load at (AUXOP-AUXON): C//				100	pF
Common Mode Minimum resistive load at AUXOP or AUXON			200		kOhms
Common Mode Maximum capacitor load at AUXOP or AUXON				10	pF

Global characteristics

Parameter	Conditions	Min	Typ	Max	Units
Maximum Output swing (EARP-EARN)	5% distortion and 120 Ohms 5% distortion and 33 Ohms	3.1 1.2	3.92 1.5		Vpp Vpp
Earphone amplifier gain			1		dB
Earphone amplifier state in power down			Hi-Z		
Parameter	Conditions	Min	Typ	Max	Units
Maximum output swing at (AUXOP-AUXON)	5%distortion maximum, Load = 1Kohms	1.6	1.96		Vpp
Auxiliary amplifier gain (AUXO)			-5		dB
AUXO amplifier state in power down			Hi-Z		
Parameter	Conditions	Min	Typ	Max	Units
Maximum output swing at (HSO)	5%distortion maximum, Load = 32 ohms	1.6	1.96		Vpp
Auxiliary amplifier gain (HSO)			-5		dB
HSO amplifier state in power down			Hi-Z		
Parameter	Conditions	Min	Typ	Max	Units
Power supply rejection			40		dB

Volume Control Gain
(Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
	VOCTL code 010	-1	0	1	dB
	VOCTL code 110	-7	-6	-5	dB
Default and reference	VOCTL code 000	-13	-12	-11	dB
	VOCTL code 100	-19	-18	-17	dB
	VOCTL code 011	-25	-24	-23	dB
Mute	VOCTL code 101,001,111			-40	dB

PGA Gain Step
(Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
Default	VDLPGA code 0000 -6dB	-6.5	-6	-5.5	dB
	VDLPGA code 0001 -5dB	-5.5	-5	-4.5	dB
	VDLPGA code 0010 -4dB	-4.5	-4	-3.5	dB
	VDLPGA code 0011 -3dB	-3.5	-3	-2.5	dB
	VDLPGA code 0100 -2dB	-2.5	-2	-1.5	dB
	VDLPGA code 0101 -1dB	-1.5	-1	-0.5	dB
Reference	VDLPGA code 0110 0dB	-0.5	0	0.5	dB
	VDLPGA code 0111 1dB	0.5	1	1.5	dB
	VDLPGA code 1000 2dB	1.5	2	2.5	dB
	VDLPGA code 1001 3dB	2.5	3	3.5	dB
	VDLPGA code 1010 4dB	3.5	4	4.5	dB
	VDLPGA code 1011 5dB	4.5	5	5.5	dB
	VDLPGA code 1100 6dB	5.5	6	6.5	dB
	other cases	-6.5	-6	-5.5	dB

Sidetone Gain Step
(Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
	VDLST code 1101 -23dB	-24	-23	-22	dB
	VDLST code 1100 -20dB	-21	-20	-19	dB
	VDLST code 0110 -17dB	-18	-17	-16	dB
	VDLST code 0010 -14dB	-15	-14	-13	dB
	VDLST code 0111 -11dB	-12	-11	-10	dB
	VDLST code 0011 -8dB	-9	-8	-7	dB
Reference	VDLST code 0000 -5dB	-6	-5	-4	dB
	VDLST code 0100 -2dB	-3	-2	-1	dB
	VDLST code 0001 1dB	0	1	2	dB
	VDLST code 0101 1dB	0	1	2	dB
	VDLST code 1000 MUTE			-66	dB
	other cases MUTE			-66	dB

Frequency response (Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Response relative to reference gain at 1kHz	<= 50 Hz			-10	dB
	50 Hz to 160 Hz			-3	dB
	300 Hz to 400 Hz	-2	0	+1	dB
	400 Hz to 3300 Hz	-1	0	+1	dB
	3300 Hz to 3400 Hz	-2	0	+1	dB
	4000 Hz to 4600 Hz			-17	dB
	4600 Hz to 6000 Hz			-40	dB
	>= 6000 Hz			-45	dB

These values are given without the external coupling capacitor.

Psophometric SNR (Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
Psophometric SNR	3 dBm0	35			dB
	0 dBm0	45			dB
	-5dBm0	52			dB
	-10dBm0	57			dB
	-20dBm0	54			dB
	-30dBm0	52			dB
	-40dBm0	42			dB
	-45dBm0	37			dB
Maximum idle channel noise				-86	dBm0
Crosstalk with the uplink path				-66	dB

Gain characteristics (Rload = 120 ohms)

Parameter	Conditions	Min	Typ	Max	Units
Absolute gain error	at 0 dBm0 and 1kHhz	-1	0	1	dB
	at -10dBm0 and 1kHz	-11	-10	-9	dB
Gain Tracking Error	3dBm0	-0.25		0.25	dB
	0dBm0	-0.25		0.25	dB
	-5dBm0	-0.25		0.25	dB
	-10dBm0(reference)		0		dB
	-20dBm0	-0.25		0.25	dB
	-30dBm0	-0.25		0.25	dB
	-40dBm0	-0.35		0.35	dB
	-45dBm0	-0.50		0.50	dB
Number of meaningful output bits	PGA and VOCTL set to 0 dB		14		Bit

3.4.2 Baseband Codec (BBC)

The baseband codec is composed of a baseband uplink path (BUL), which modulates the bursts of data coming from the DSP via the baseband serial port (BSP) and to be transmitted at the antenna. A GMSK modulator according to GSM specification 5.04 performs modulation. The GMSK modulator implemented in digital technique generates In-phase (I) and Quadrature (Q) components which are converted into analog baseband by two 10 bits DACs and then filtered by third order low-pass filters. The baseband uplink path includes secondary functions such as DC offset calibration and I/Q gain unbalance.

Second part of baseband codec is the baseband downlink path (BDL) which converts the baseband analog I & Q components coming from the RF receiver into digital samples and filters these resulting signals through a digital FIR to isolate the desired data from the adjacent channels. During reception of burst I & Q digital data are sent to the DSP via the baseband serial port (BSP) at a rate of 270.833 kHz. The baseband downlink includes a DC offset calibration.

Timing windows of the BUL and BDL are controlled through the Time Serial Port (TSP) by the TPU of DBB and [BULON, BULENA, BDLON, BDLENA] are accessible through the pins TEST[1..4] programmed by a specific test mode.

Implementation of baseband codec allows full-duplex operation. Multislot is supported in uplink and downlink.

UPLINK PATH

DC characteristics

(Output differential load 10KÙ // 47pF for BULIP-BULIN and BULQP-BULQN

)

Parameter	Conditions	Min	Typ	Max	Units
I and Q DAC resolution			10		bit
Voltage reference BBVREF ①			1.75		V
Dynamic range on each output	Centered on VVMID		BBVREF		Vpp
Output common mode voltage VVMID	SELMID[2,1,0]=000	VRABB / 2 -5%	VRABB / 2	VRABB / 2 +5%	V
	SELMID[2,1,0]=001	1.30	1.35	1.40	V
	SELMID[2,1,0]=010	1.40	1.45	1.50	V
	SELMID[2,1,0]=011	VREF -5%	VREF	VREF +5%	V
	SELMID[2,1,0]=1xx	1.20	1.25	1.30	V
Offset error after calibration		-9		9	mV
I and Q output state in power down			HiZ		

① internal reference

AC characteristics

Parameter	Conditions	Min	Typ	Max	Units
Differential output dynamic range BULIP -BULIM or BULQP -BULQM	OUTLEV[2,1,0]=000		2x BBVREF		Vpp
	OUTLEV[2,1,0]=010		2.56		
	OUTLEV[2,1,0]=001		1.86		
	OUTLEV[2,1,0]=011		0.93		
	OUTLEV[2,1,0]=100		2.1		
	OUTLEV[2,1,0]=101		2.1		
	OUTLEV[2,1,0]=110		2.33		
	OUTLEV[2,1,0]=111		2.33		

Parameter	Conditions	Min	Typ	Max	Units
Absolute gain error relative to V_{VREF}	Measured on 67.7kHz sine wave	-1.5		1.5	DB
Gain matching between channels I and Q	Measured on 67.7kHz	-0.5	0.0	0.5	DB
Phase matching between channels I and Q	Sine wave	-0.5	0.0	0.5	Deg
Modulation spectrum mask. Measured by average of FFT's On random modulated bursts using a Blackman-Harris window with 30 kHz bandwidth	100 kHz			0.5	DBc
	200 kHz			-34	DBc
	250 kHz			-37	DBc
	400 kHz			-65	DBc
	600 kHz			-72	DBc
	800 kHz			-72	DBc

Timing characteristics

Parameter	Conditions	Min	Typ	Max	Units
Setup time , BULON ↑ to BULCAL ↑		15			µS
Pulse duration BULCAL high		132			µS
Setup time , BULCAL ↓ to BULENA ↑		2			¼bit
Pulse duration BULENA high	N effective duration of burst		N - 32		¼bit ①
Modulation hold time after BULENA ↓			32		¼bit ①
Hold time BULON after BULENA ↓		32			¼bit ①
Modulator input to output delay	From BULENA ↑ to mid of 1st bit		2.5		¼bit ①

Values in above table are given for system information only.

① Bit is relative to GSM bit = 1/270.833 kHz.

DOWNLINK PATH

General characteristics

Parameter	Conditions	Min	Typ	Max	Units
Dynamic range on each input			BBVREF		Vpp
Differential input dynamic range	BDLIP-BDLIM or BDLQP-BDLQM		2x BBVREF		Vpp
Differential input resistance	BDLIP-BDLIM or BDLQP-BDLQM	130	200	270	KΩ
Differential input capacitance	BDLIP-BDLIM or BDLQP-BDLQM		4		PF
Single ended input resistance to ground	BDLIP or BDLIM or BDLQP or BDLQM	70	110	150	KΩ
Single ended input capacitance to ground			8		pF
External input common mode voltage ①		0.8	VRABB/2	VRABB -0.8	V
Range of digital ouput data samples		-32768		+32767	
I and Q input state in power down			HiZ		

① Min and Max value will limited the Dynamic range on each input (see Analog IO electrical characteristics)

DC characteristics

Parameter	Conditions	Min	Typ	Max	Units
Offset error after calibration		-25		25	LSB ①
		-7.5		7.5	mV ②

① The LSB corresponds to the one of the ADC that is specified as 82dB dynamic range (± 5792), which means 13.3 bits, but the output data bits are transmitted through the BSP in a 16 bit word format. The maximum/minimum code on a 16 bits word is ±32767.
Therefore, one LSB of the ADC corresponds to a value of 32768/5792=5.65 on the 16 bit output serial words on Q & I.
The maximum digital output code is 32767 for an input of −3 dbm0 without clipping. For an input signal from −3 dbm0 to 0 dbm0, the output of digital filter is clipped to 32767 code.

② Analog value of the LSB is 1.75V/5792 = 0.3 mV.

AC characteristics

Parameter	Conditions	Min	Typ	Max	Units
Gain matching between channels	Measured on 18 kHz	-0.5	0.0	0.5	dB
Delay matching between channels	Sine wave	-16	0.0	16	ns
Frequency response of the total downlink path with values related to 18 kHz	800 Hz	0.0		0.35	dB
	18 kHz (ref)		0		
	35 kHz	-0.4		0.25	
	59 kHz	-0.4		0.30	
	68 kHz	-0.7		0.30	
	81 kHz	-3		0.0	
	97 kHz	-6		-3	
	110 kHz			-8	
	120 kHz			-15	
	135 kHz			-35	
	200 kHz			-45	
	> 200 kHz			-45	
Signal to noise ratio on 200 kHz bandwidth	-45 dBm0	37			dB
	-40 dBm0	42			
	-30 dBm0	52			
	-20 dBm0	62			
	-10 dBm0	72			
	-6 dBm0	72			
Idle channel noise 0-200 kHz				-82	dBm0 ①
Gain tracking error at 18 kHz with reference at -10dBm	-6 dBm0	-0.25		0.25	dB
	-10 dBm0	-0.25		0.25	
	-20 dBm0	-0.25		0.25	
	-30 dBm0	-0.25		0.25	
	-40 dBm0	-0.25		0.25	
	-50 dBm0	-0.50		0.50	
Group delay	0 Hz to 100kHz		28		µS

① 0 dBm0 is defined as a differential input signal of 2xBBVREF

Timing characteristics

Parameter	Conditions	Min	Typ	Max	Units
Setup time , BDLON ↑ to BDLCAL ↑		5			µS
Pulse duration BDLCAL high		60			µS
Setup time , BDLCAL ↓ to BDLENA ↑		>0			1/4-bit
Pulse duration BDLENA high	N effective duration of burst		N		1/4-bit ①
Setup time after BDLENA↑ before DATA valid				32.7	µS
Hold time DATA valid after BDLENA↓				3.7	µS
Hold time BDLON high after BDLENA ↓		3.7			µS

Values in the above table are given for system information only

① Bit is relative to GSM bit = 1/270.833 kHz .

3.4.3 Voltage Regulation (VREG)

Several low-dropout (LDO) regulators perform linear regulation to supply analog and digital baseband circuits.

The LDO (VRDBB) generates programmable supply voltage (1.8V, 1.5V, and 1.3V, programmable by register bits) for the digital core of DBB. The battery supplies it.

The LDO (VRABB) generates the supply voltage (2.8V) for the analog functions of ABB. The battery supplies it.

The LDO (VRIO) generates, from the battery, the supply voltage (2.8V) for the digital core of ABB and the digital I/O's of DBB and ABB. The battery supplies it.

The LDO (VRMEM) generates, from the battery, the supply voltages (1.8V, 2.8V, programmable by VLMEM pin) for DBB memory interfaces I/O's. The battery supplies it.

The LDO (VRRAM) generates, from the battery, the supply voltages (1.8V, 2.8V, programmable by VLMEM pin) for DBB memory interfaces I/O's. The battery supplies it. The output blocks reverse current when the regulator is OFF.

The LDO (VRRTC) generates programmable supply voltage (1.8V, 1.5V or 1.3V, programmable by register bits and by an external pin) for the following blocks of DBB (real time clock and 32khz oscillator). It is supplied by UPR and is always ON.

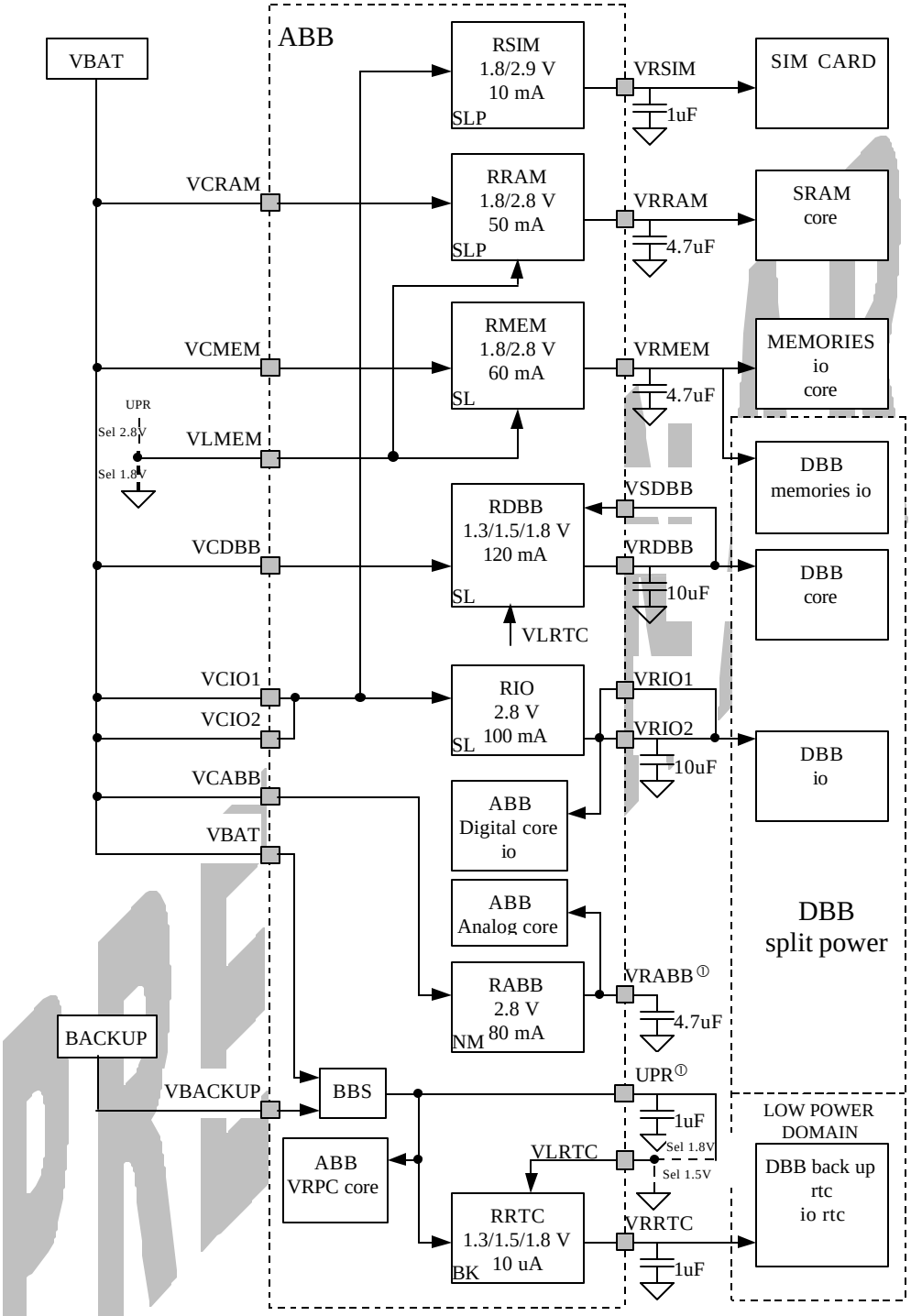
The LDO (VRSIM) generates, from the battery, the supply voltages (1.8V, 2.9V, programmable by register bit) for SIMCARD interfaces I/O's. The battery supplies it.

The backup battery switch (BBS) generates at its output an uninterrupted power rail (UPR) of which purpose is to supply continuously the minimum necessary circuitry of the power-control functions either from the main battery or from the backup battery. This uninterrupted power rail is connected to the external pin UPR for decoupling purpose.

VRABB, VRDBB, VRIO, VRMEM, VRRAM are enable by the VRPC switch on/off sequences. VRDBB, VRIO, VRMEM, VRRAM, VRSIM have 3 functional modes ON, SLEEP and OFF. VRABB has 2 functional modes ON and OFF. VRSIM is enabled/disabled by a register bit.

The outputs VRABB, VRDBB, VRIO, VRMEM, VRSIM are not blocking the reverse current when the regulators are OFF.

The default value for all the programmable LDO are the value set by a VRPC register after a PORZ (see VRPC block description and VRPC register).



BK : regulators ON in BACKUP/ SLEEP / NORMAL mode
SL : regulators ON in SLEEP / NORMAL mode
SLP : idem SL + reverse current protection
NM : regulators ON in NORMAL mode
① : reserved for ABB private use only

REGULATOR RDBB

(With 10uF decoupling capacitor① connected between VRDBB and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCDBB		3.00	VBAT	5.5	V
Output Voltage VRDBB	VDBB1,VDBB0 = '10' (Default if VLRTC='1') ②	1.65	1.80	1.95	V
	VDBB1,VDBB0 = '00'(Default ②	1.35	1.50	1.65	
	VDBB1,VDBB0 = '01' ②	1.24	1.30	1.36	
Rated output current Iout	Activ mode			120	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 1.55V to 5.5V @ Iout = max VDBB1,VDBB0 = '00'			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRDBB = final +/- 3%		10		µs
Turn-on time	from RDBBEN = 0 to 1 @ Iout = max, VRDBB=final +/-3%		.2		ms
Ripple rejection	f=100Hz @ Iout max		55		dB
	f=500kHz @Iout max		35		dB
Quiescent current	Activ mode		150		uA
	Sleep mode		20		
	Disable		1		

① 0.01 Ù <ESR < 0.3 Ù. ② With input sense pins VSDBB connected externally to VRDBB output.

REGULATOR RRAM

(With 4.7uF decoupling capacitor① connected between VRRAM and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCRAM ②		3.0	VBAT	5.5	V
Output Voltage VRRAM	Activ mode , VLMEM = VCMEM	2.7	2.8	2.9	V
	Activ mode , VLMEM = VSS	1.65	1.8	1.95	
	Sleep mode , VLMEM = VCMEM	2.7	2.85	3.0	
	Sleep mode , VLMEM = VSS	1.65	1.85	2.0	
Rated output current Iout	Activ mode			50	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRMEM = final +/- 3%		10		µs
Turn-on time	from RMEMEN = 0 to 1 @ Iout = max, VRMEM =final +/-3%		.2		ms
Ripple rejection	f=100Hz @ Iout max		55		dB
	f=500kHz @Iout max		35		
Quiescent current	Activ mode		150		uA
	Sleep mode		20		
	Disable		1		

① 0.01 Ù <ESR < 0.3 Ù. ② Two input pins to reduce input dropout

REGULATOR RMEM

(With 4.7uF decoupling capacitor① connected between VRMEM and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCMEM1, VCMEM2 ②		3.0	VBAT	5.5	V
Output Voltage VRMEM	Activ mode , VLMEM = VCMEM	2.7	2.8	2.9	V
	Activ mode , VLMEM = VSS	1.65	1.8	1.95	
	Sleep mode , VLMEM = VCMEM	2.7	2.85	3.0	
	Sleep mode , VLMEM = VSS	1.65	1.85	2.0	
Rated output current Iout	Activ mode			60	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRMEM = final +/- 3%		10		µs
Turn-on time	from RMEMEN = 0 to 1 @ Iout = max, VR2OUT =final +/-3%		.2		ms
Ripple rejection	f=100Hz @ Iout max		55		dB
	f=500kHz @Iout max		35		
Quiescent current	Activ mode		150		uA
	Sleep mode		20		
	Disable		1		

① 0.01 Ù <ESR < 0.3 Ù.

② Two input pins to reduce input dropout

REGULATOR RABB

(With 4.7uF decoupling capacitor① connected between VRABB and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCABB		3.0	VBAT	5.5	V
Output voltage VRABB	Activ mode	2.7	2.8	2.9	V
	Sleep mode	2.7	2.85	3.0	
Rated output current Iout	Activ mode			80	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRABB = final +/- 3%		10		µs
Turn-on time	from RABBEN = 0 to 1 @ Iout = max, Vout = final +/-3%		.2		ms
Ripple rejection	f=100Hz @ Iout max		55		dB
	f=500kHz @Iout max		35		
Quiescent current	Enable		150		uA
	Disable		1		

① 0.01 Ù <ESR < 1 Ù.

REGULATOR RIO

(With 10uF decoupling capacitor① connected between VRIO and VSS)
CAUTION: VRIO supplies ABB digital IO and ABB digital core.

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCIO1, VCIO2 ②		3.0	VBAT	5.5	V
Output Voltage VRIO1, VRIO2 ③	Activ mode	2.7	2.8	2.9	V
	Sleep mode	2.7	2.85	3.0	
Rated output current Iout	Activ mode			100	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRIO = final +/- 3%		10		µs
Turn-on time	from RIOEN = 0 to 1 @ Iout = max, VRIO=final +/-3%		.5		ms
Ripple rejection	f=100Hz @ Iout max f=500kHz @Iout max		55 35		dB
Quiescent current	Enable		150		uA
	Sleep		20		
	Disable		1		

① 0.01 Ù <ESR < 1.0 Ù.
② Two input pins to reduce input dropout
③ Two output pins to reduce output dropout

RSIM

(With 1uF decoupling capacitor① connected between VRSIM and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCIO1, VCIO2 ②		3.0	VBAT	5.5	V
Output Voltage VRSIM	SIMSEL = '1'	2.7	2.85	3.0	V
	SIMSEL = '0'	1.65	1.8	1.95	
Rated output current Iout	Activ mode			10	mA
	Sleep mode			1	
Load regulation	Iout = max to 0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRSIM = final +/- 3%		10		µs
Turn-on time	from RSIMEN = 0 to 1 @ Iout = max, VRSIM =final +/-3%		.2		ms
Ripple rejection	f=100Hz @ Iout max		55		dB
	f=500kHz @Iout max		35		
Quiescent current	Activ mode		150		uA
	Sleep mode		20		
	Disable		1		

① 0.01 Ù <ESR < 0.3 Ù.
② Two input pins to reduce input dropout

UPR

(With 1.0uF decoupling capacitor① connected between UPR and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VBAT			VBAT		V
Input voltage VBACKUP			VBCK		V
Output Voltage UPR	VBAT > 2.8		VBAT		V
	VBAT < 2.8 & VBAT > VBACKUP		VBAT		
	VBAT < 2.8 & VBAT < VBACKUP		VBCK		

① 0.1 Ù <ESR < 0.5 Ù.

REGULATOR RRTC

(With 1.0uF decoupling capacitor① connected between VRRTC and VSS)

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCRTC			UPR		V
Output Voltage VRRTC	VRTC1,VRTC0 = '10' (Default if VLRTC= '1')	1.65	1.80	1.95	V
	VRTC1,VRTC0 = '00' (Default if VLRTC= '0')	1.35	1.50	1.65	
	VRTC1,VRTC0 = '01'	1.24	1.30	1.36	
Rated output current Iout				10	uA
Load regulation	from Iout =max to Iout=0			100	mV
Line regulation	Input voltage = 3.0V to 5.5V @ Iout = max			50	mV
Response time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRRTC = final +/- 3%		100		us
Turn-on time	Iout step from 0 to Iout max Iout step from Iout max to 0 @ VRRTC = final +/- 3%		0.5		ms
Ripple rejection	f=100Hz @ Iout max f=500kHz @Iout max		55 35		dB
Quiescent current	Enable		2		uA

① 0.1 Ù <ESR < 0.5 Ù.

Parameter	Conditions	Min	Typ	Max	Units
Input voltage VCRTC			UPR		V
PORZ high threshold		2.5	2.65	2.8	V
PORZ low threshold		1.9	2.1	2.3	V

① RRTC as 2 exclusive modes: REGULATOR or POWER ON RESET generator.

3.4.4 Reference Voltage / Power on Control (VRPC)

Band gap reference

An integrated band-gap generates a reference voltage. This reference is available on an external pin for external filtering purpose only. This filtered reference is internally used for analog functions.

The external resistor connected between pin IBIAS and REFGND sets, from the band-gap voltage, the value of the bias currents of the analog functions.

(with 0.1uF decoupling capacitor connected between VREF and REFGND)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage on VREF	VBAT = 3.6V	1.16	1.185	1.20	V
Output Voltage on IBIAS	VBAT = 3.6V R(IBIAS)=100 kÙ 1%		VREF		V

DAC and ADC in ABB are references towards VREF value.

Power on Control

The VRPC block is in charge to control the Power ON, Power OFF, Switch On, and Switch OFF sequences.

Even in Switch OFF state some blocks functions are performed. These “permanent” functions are functions, which insure the wake-up of the mobile such as ON/OFF button detection or charger detection.

Interrupt INT1 are generated at power-down detection when abnormal voltage conditions are detected.

Interrupt INT2 are generated on some PWON, RPWON, Charger plug, ITWAKEUP events.

Mode Definition

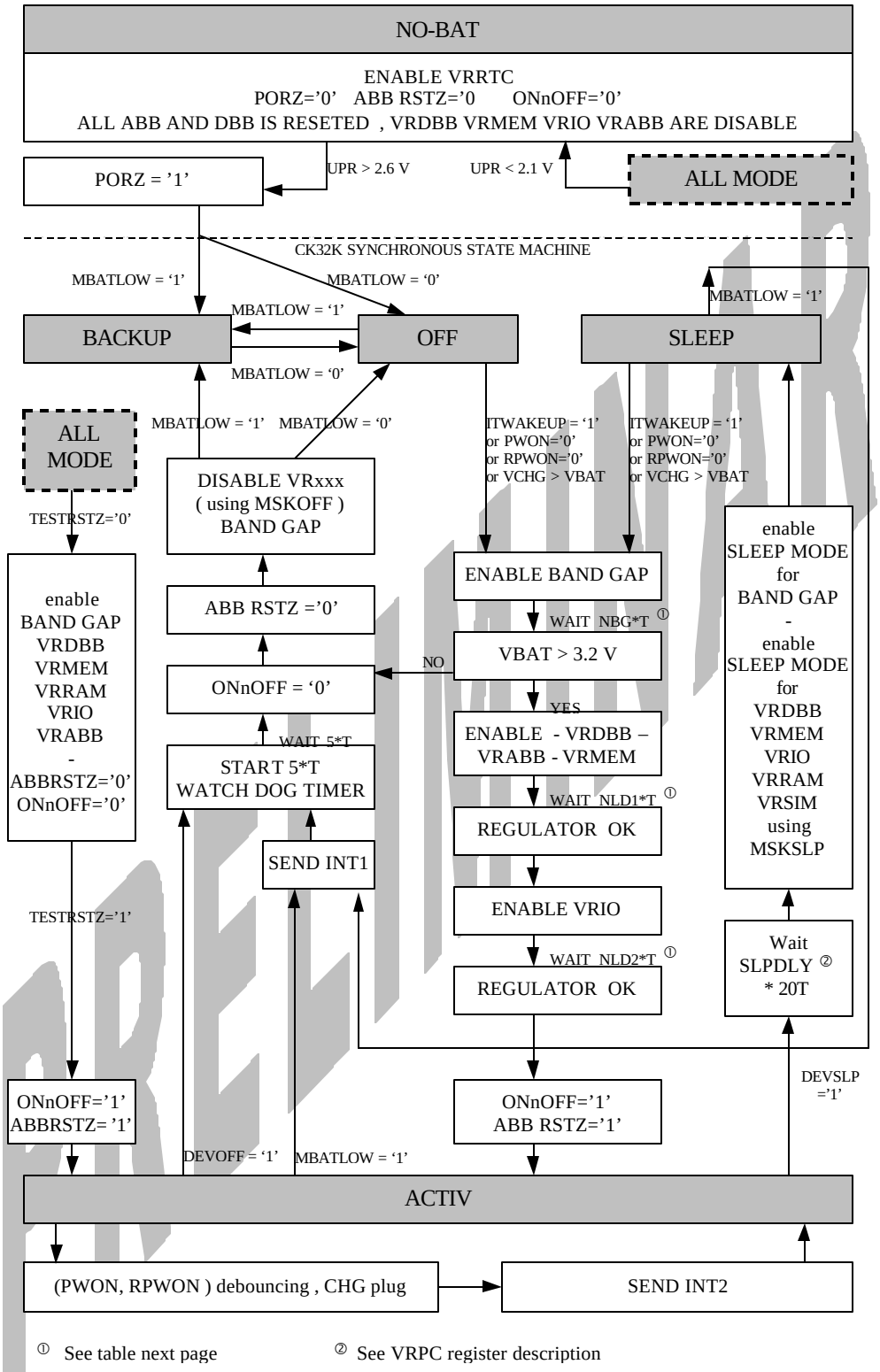
NOBAT : Batteries (MAIN or BACK UP) are not efficient to supply ABB or DBB. PORZ is maintained low, All ABB registers are reseted, DBB is reseted.

BACKUP : BACKUP battery is used to supply UPR, only VRRTC is enable supplied by UPR, 32KHZ is available, all switch on conditions are masked. Part of ABB is reseted (see register bits definition) , DBB is reseted.

OFF : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRSIM supplied by MAIN battery can be in sleep mode (using MSKOFF register) or are disable. VRABB is disable. Part of ABB is reseted (see register bits definition), DBB is reseted.

SLEEP : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRSIM supplied by MAIN battery can be in sleep mode (using MSKSLP register) or are disable. VRABB is disable. All ABB blocks are forced in power down mode, but power on block configuration is kept when ABB return in ACTIV mode.

ACTIV : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRABB are enable and under DBB control, VRSIM is under DBB control.



① See table next page ② See VRPC register description

Note

CK32K : Provided by DBB, is available sometimes after that VRTC is regulated. VRPC state machine is clock by CK32K and as its asynchronous reset PORZ.

T : CK32K period

PORZ : ABB internal signal, Power On Reset , activ low, reset VRPC.

ABBRSTZ : ABB internal signal, Analog Baseband Reset, activ low, reset all ABB blocks (except VRPC)

RESPWONZ : DBB RTC reset , is equal to the boolean function : PORZ and TESTRSTZ.

MBATLOW : State of VBAT>2.8 comparator (describe in UPR specification part)

Debouncing

PWON and RPWON are debounce in the VRPC hardware. The counter used is the same that count all others VRPC timing events, the debouncing has the lowest VRPC priority and can be done only on one signal at a time.

Parameter	Conditions		Value		Units
NDEB	Debouncing on PWON and RPWON		1022		T

Switch On Timing Table

The state machine waiting times are variable depending on the switch on configuration:

Parameter	Conditions		Value		Units
NBG	Switch on from OFF		1010		T
	Switch on from SLEEP		130		T
NLD1	Switch on from OFF		21		T
	Switch on from SLEEP		7		T
NLD2	Switch on from OFF		11		T
	Switch on from SLEEP		7		T

Consumption in dedicated mode

Parameter	Conditions	Min	Typ	Max	Units
BACKUP	From Backup battery 3.2V **@ 25C** CK32 on	1.65	2.35	3.25	uA
	From Backup battery 3.2V **@ 85C** CK32 on	1.75	2.5	3.5	uA
OFF	From Main battery 5.5V **@ 25C** CK32 on, LDO off	10	25	55	uA
	From Main battery 5.5V **@ 85C** CK32 on , LDO off	10	30	75	uA
SLEEP	From Main battery 5.5V **@ 25C** CK32 on, CK13M off, all block off.		100	150	uA
	From Main battery 5.5V **@ 85C** CK32 on, CK13M off, all block off.		130	200	uA
ACTIV (no external load on LDO)	From Main battery 5.5V CK32 on, **CK13M off**, all block off.		800	1500	uA

	From Main battery 5.5V CK32 on, **CK13M on**, all block off.		1500	3000	uA

Backup battery charge is disable and Main battery precharge is disable

3.4.5 Battery charger Interface (BCI)

The main function of the ABB Charger interface is the charging control of either a 1-cell Li-ion Battery or 3-serie Ni-MH/Ni-Cd cell batteries with the support of the micro controller (DBB).

The battery monitoring uses the 10 bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage.

The magnitude of the charging current is set by the 10 bits of a programming register converted by an 10 bit Digital to Analog Converter, whose output sets the reference input of the charging current control loop.

The battery charger interface performs also some auxiliary functions. They are battery precharge and back-up battery charge if it is rechargeable.

The battery charger interface is under registers control. These registers can be programmed either through the BSP or through the USP.

BCI (Battery Charger Interface)

VBAT = 3.6V unless otherwise specified

Parameter (main battery charge)	Conditions	Min	Typ	Max	Units
VCHG input voltage range		4.8 ①		6.8	V
ICTL output voltage swing	CHEN='0', VCHG=6.8V, I(ICTL) = -10uA	VCHG-0.3			V
	CHEN='1', VCHG=6.8V, MESBAT=0 I(ICTL) = +10uA			0.8	V
	CHEN='1', VCHG=6.8V, MESBAT=1 I(ICTL) = +10uA	VCHG-0.3			V
Current to voltage conversion slope ②	Rs=0.2 Ù (VRABB-VBAT) from 0.1V to 0.17V		2		mV / mA
Current to voltage conversion offset ④	Rs=0.2 Ù		0.2		V
Current to voltage conversion offset calibration step: OFFSTEP ④	Rs=0.2 Ù		12.6		mV
Parameter (main battery precharge)	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Precharge charging current ③	VBAT = 0.5V			100	mA
	VBAT = 3.6V				
Battery voltage at precharge end	VBAT open	3.4	3.6	3.9	V
Parameter (MADC)	**Conditions**	**Min**	**Typ**	**Max**	**Units**
VCHG to MADC input attenuation	VCHG from 4.0V to 6.8V	0.15	0.20	0.30	V/V
VBACKUP to MADC input attenuation	VBACKUP from 2.2V to 5.5V	0.2	0.25	0.35	V/V
VBAT to MADC input attenuation	VBAT from 3.0V to 5.5V	0.2	0.25	0.35	V/V
ADIN2 DC current source for temperature measurement	R(IBIAS)=100k Ù , ADIN2= 1V 8 possibles ranges (Register BCICTL1, bits THSENS2-0)				
	Code = 0	8		14	uA
	Code = 1	15		24	
	Code = 2	25		34	
	Code = 3	35		43	
	Code = 4	44		52	
	Code = 5	53		62	
	Code = 6	62		72	
	Code = 7	72		82	
ADIN1 DC current source for battery identification	R(IBIAS)= 100k Ù , ADIN1= 1V	8		12	µA
Parameter (backup battery charge)	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Back-up battery charging current	VBACKUP=2.8V , BBCHEN = 1	250	500	800	uA
End back-up battery charging voltage	VBACKUP open	3.0		3.6	V

① The max voltage value of the charging device is 7V (process limitation). The min voltage value of the charging device is: **VBATMAX + diode drop + 0.2ohm resistor drop + VDC drop.** When VBATMAX is the max voltage value of the battery (4.2V for Li-ion battery). For example to charge Li-ion battery with 1A fast current charge, the min voltage value of the charging device must be 5.1V.

② MADC output code = (VCCS-VBATS) * 10 + offset

③ The current is programmable by an external resistor.

④ Calibration can be made through BCICONF register, to the natural offset can be added a positive offset from 0 to 15*OFFSTEP.

3.4.6 Monitoring ADC (MADC)

The monitoring ADC consists in a 10-bit analog to digital converter combined with a nine inputs analog multiplexer. Out of the 8 inputs 4 are available externally, the 4 remaining being dedicated to main battery voltage, back up battery voltage, charger voltage and charger current monitoring. On the tree available as standard inputs intended for battery temperature, batteries type measurements. Conversion requests, input/output channels and results reading can be done either through the BSP or through the USP. The STARTADC bit through the TSP interface can also control the start of conversion.

General characteristics

Parameter	Conditions	Min	Typ	Max	Units
Resolution			10		Bit
MADC Voltage reference			1.75		V
Input leakage current ADINx				1	uA
Differential non linearity		-2		+2	LSB
Integral non linearity	Best fitting	-2		+2	LSB
Input Range		0		1.75	V

AC characteristics

Parameter	Conditions	Min	Typ	Max	Units
Running frequency F			1		MHz
Clock period T=1/F			1		us
Conversion time (16*T = delay before the sampling of the analog input)			16*T + 8.5*T		us

3.4.7 Clock generator (CKG)

The clock generator generates the system clocks needed by the internal functions. They are derived from the CK13M master clock provided by DBB to ABB.

In low power mode some functions such as VRPC are maintained alive by using the low power clock, CK32K, generated by the RTC of the DBB.

3.4.8 Automatic Frequency control (AFC)

The automatic frequency control function (AFC) consists of a DAC optimized for high-resolution DC conversion. The AFC digital interface includes two registers that can be written or read using either the BSP or the USP under the arbitration of IBC. The content of these registers controls a 13-bit DAC, operating at a sampling frequency of 2.165 MHz (or 1.08 MHz, 541 kHz, 270 kHz setting correctly the AFCCTLADD register), whose purpose is to correct frequency shifts of the voltage-controlled oscillator to maintain the GSM 13 MHz master clock frequency in a 0.1 PPM range.
The AFC value is programmed with registers AUXAFC1 (which contains the 10 LSB) and AUXAFC2 (which contains the 3 MSB). The three MSB are fed to the DAC through AUXAFC2 whose content is updated with the content of a shadow register when LSBs are written in AUXAFC1, so proper operation of the AFC is ensured by writing the MSB first and then the LSBs.
The monotonicity is ensured by the structure of the DAC made with Σ-Δ digital modulators followed by an analog FIR which performs one bit digital to analog conversion and low pass filtering. Further low pass filtering is provided by the RC formed by the internal output resistor (25 kΩ) and an external capacitor (33 nF). However most of the filtering is ensured by the voltage-controlled oscillator of which high quality factor provide a very low frequency low pass filtering.
Power on of the AFC is controlled by bit AFCON of PWDNRG register
The automatic frequency control provides a 13-bit accuracy and a 2.0 V dynamic range.

DAC 13 characteristics

Parameter	Conditions	Min	Typ	Max	Units
DAC resolution			13		Bit
Sampling frequency	AFCCTLADD reg ='00'		2.165		MHz
	AFCCTLADD reg ='01'		1.08		MHz
	AFCCTLADD reg ='10'		541		kHz
	AFCCTLADD reg ='11'		270		kHz
LSB value		250		340	uV
Integral non linearity	(0 to 75% range)	-1		+1	LSB
Differential non linearity	(0 to 75% range)	-1		+1	LSB
Settling time			100		us

Output characteristics ①

Parameter	Conditions	Min	Typ	Max	Units
Output voltage at code min				45	mV
Output voltage at code max		2.0	2.4	2.8	V
Output voltage in power-down			0		V
Output resistance		15.6	22.5	29	Kohms

① Recommended load on pin AFC: 33nF

3.4.9 Automatic Power Control (APC)

Purpose of the Automatic Power Control (APC) is to generate an envelope signal to control the power ramping up, ramping down and power level of the radio burst. The APC structure is intended to support single slot and multislot transmission with smooth power transition when consecutive bursts are transmitted at different power level.

It includes a DAC and a RAM in which the shape of the edges (ramp-up and ramp-down) of the envelope signals are stored digitally. This envelope signal is converted to analog by a 10 bits digital to analog converter.

Timing of the APC is generated internally and depends of the real time signals coming from the TSP and the content of two registers which control the relative position of the envelope signal versus the modulated I & Q.

DAC 10 characteristics

Parameter	Conditions	Min	Typ	Max	Units
DAC resolution			10		Bit
Integral nonlinearity	Best fitting line	-1		+1	lsb
Differential non-linearity		-1		+1	lsb
Settling time			5		µs

Output stage characteristics ①

Parameter	Conditions	Min	Typ	Max	Units
Output voltage with code max		2	2.2	2.4	V
Offset voltage floor	AUXAPC=0 APCOFF=0		120	200	mV
Offset voltage adjustment			128	150	mV
Offset voltage adjustment step			2	2.3	mV
Output impedance in power down				150	Ω
Output voltage in power down				50	mV

① Recommended load on pin APC : 50pF max // 10 kΩ min

Timings

Parameter	Conditions	Min	Typ	Max	Units
delay BULENA ↑ to ramp-up start		2		1025	1/4-bit
delay BULENA ↓ to ramp-down start		2		1025	1/4-bit
ramp-up duration		0		16	1/2-bit
ramp-down duration		0		16	1/2-bit
modulation after BULENA ↓			32		1/4-bit

3.4.10 Auxiliary DAC (ADAC)

The auxiliary DAC is a general-purpose 10 bits digital to analog converter.

Output stage characteristics ①

Parameter	Conditions	Min	Typ	Max	Units
DAC resolution			10		Bit
Integral non linearity	Best fitting line	-1		+1	LSB
Differential non linearity		-1		+1	LSB
Settling time			10		µs
Output voltage with code max		2.0	2.2	2.4	V
Output voltage with code min		0.18	0.24	0.3	V
Output impedance in power down			200		kΩ
DC power supply sensitivity			1		%

① Recommended load on pin DAC : 50pF max // 10 kΩ min

3.4.11 SIM card interface (SIM)

The Sim Card digital interface in ABB insures the translation of logic levels between DBB and Sim Card, for the transmission of 3 different signals: a clock derived from a clock elaborated in DBB, to the Sim-Card (DBBSCK ⇨ SIMCK), a reset signal from DBB to the Sim Card (DBBSRST ⇨ SIMRST), and serial data from DBB to the Sim Card (DBBSIO ⇔ SIMIO) and vice-versa.

The SIM card interface can be programmed to drive a 1.8V or 3V Sim Card.

3.4.12 Auxiliary Current Driver (ACD)

Auxiliary drivers are provided
LEDA is dedicated for paging indication.
LEDB is dedicated for LCD backlight and Keypad backlight.
LEDC is dedicated for charging indication with hardware switch on.

Parameter	Conditions	Min	Typ	Max	Units
LEDC drive current				10	mA
LEDA drive current	Current sink			10	mA
LEDB drive current	Current sink			150	mA
LEDC Output high level voltage				VCHG	V
LEDA, LEDB Output high level voltage				VBAT	V
LEDA, LEDC Output low level voltage	I = drive current max			0.4	V
LEDB Output low level voltage	I = drive current max			0.7	V

LEDC is controlled in BCI registers. When ABB is in OFF or SLEEP mode, the LEDC control follows the precharge state. When ABB is in ACTIV mode, the LEDC control is given by a register bit (in BCI register).

LEDA, LEDB is controlled in a dedicated register.
LEDA needs CK32K clock to be fully functional
LEDB needs CK13M clock to be fully functional

The 3 led drivers are connected internally to 2 ground pads, GNDL1 and GNDL2.
The LEDB driver has 2 input pads (LEDB1, LEDB2) due to high current sinked.

3.4.13 Internal bus and interrupt controller (IBIC)

Read and write access to all internal registers being possible via both the BSP and USP, purpose of the internal bus controller is to arbitrate the access on the internal bus and to direct the read data to the proper serial port. During reception of a burst the internal bus controller assign the transmit part of the BSP to the baseband downlink to transfer the I & Q samples to the DSP.

This block also handles the internal interrupts generated by the MADC, BCI and VRPC blocks and generates the micro-controller interrupt signal INT2.

3.4.14 Baseband Serial Port (BSP)

The baseband serial port is a bi-directional (transmit/receive) serial port. Both received and transmit operations are double buffered and permit a continuous communication stream. Format is 16 bit data packet with frame synchronization.

The CK13M master clock is used for as clock for both transmit and receive.

The baseband serial port allows read and writes access of all internal registers under the arbitration of the internal bus controller. But its transmit path is allocated to baseband downlink during burst reception for I & Q data transmission.

In the receive mode the frame signal, BFSR, is generated by DBB. In the transmit mode the frame signal, BFSX, is generated by ABB.

BSP access are not allowed when ACTIVMCLK='0'.

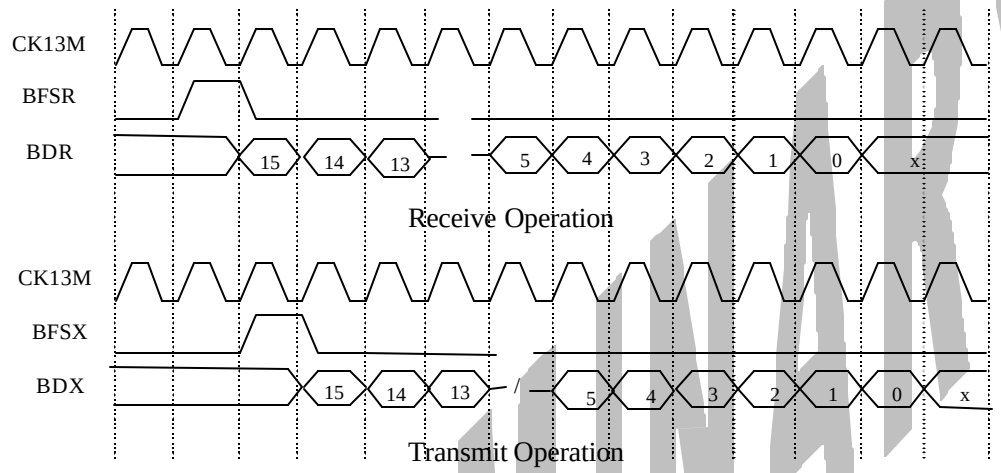
BSP interface timings requirements

Parameter	Conditions	Min	Typ	Max	Units
tsu3 BFSR setup time before CK13M↓			20		ns
th3 BFSR hold time after CK13M↓			20		ns
tsu4 BDR setup time before CK13M↓			20		ns
th4 BDR hold time after CK13M↓			20		ns
td2 BFSX delay from CK13M↓			20		ns
td3 BDX delay after CK13M↓			20		ns

Note : T = CK13M clock period = 77ns

Single Operation Mode

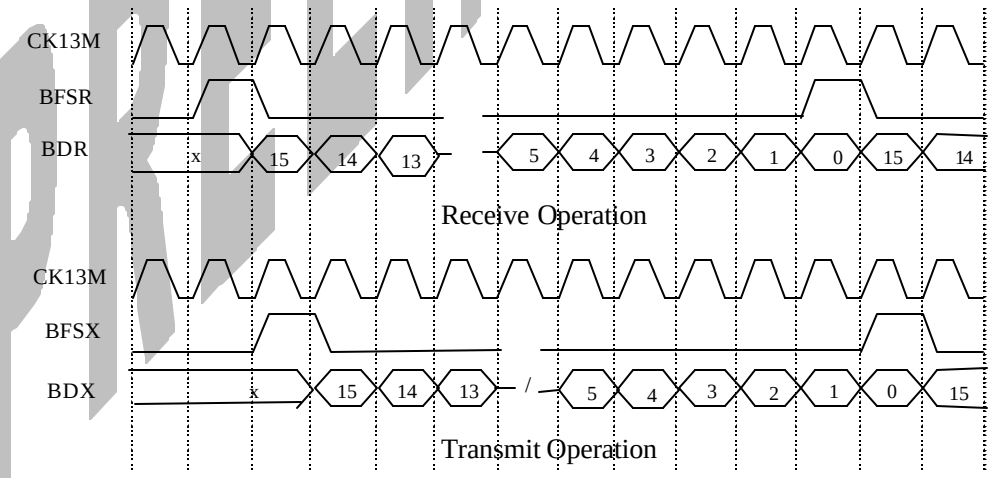
In the single mode operation the synchronization pulses, BFSR or BFSX, are generated one CK13M period before the first data bit (the MSB or bit15).



Single **BSP** Operations

Adjacent Operations Mode (GMSK burst)

In the adjacent operations mode the first transmission is same as in the single operation mode. But for the following words the synchronization pulse is synchronous with the last bit (the LSB or bit0) from the previous word.



Adjacent **BSP** Operations

3.4.15 Time serial port (TSP)

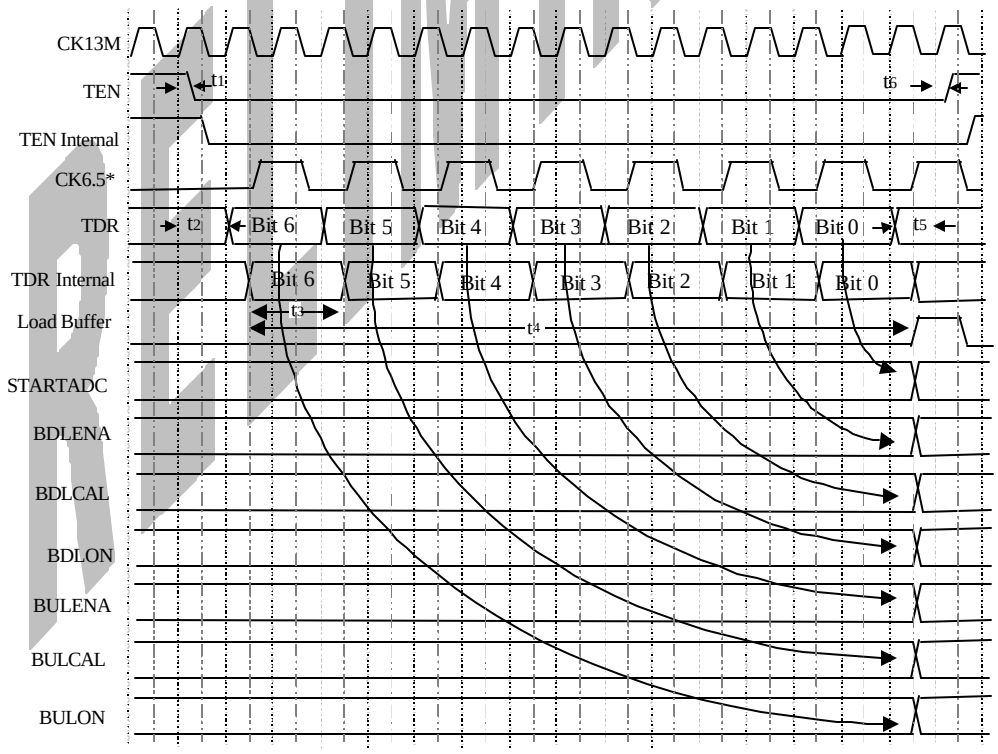
Purpose of the time serial port is to control in real time the radio activation windows of ABB which are BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration and BDL receive and the ADC conversion start.

These real time control signals are processed by the TPU of DBB and transmitted serially to ABB via the TSP, which consists in a very simple two pins serial port. One pin is an enable (TEN) the other one the data receive (TDR). The master clock CK13M divided by 2 is used as clock for this serial port.

TSP interface timings requirements

Parameter	Conditions	Min	Typ	Max	Units
t1 TEN↓ setup time before CK13M↑		0		T/2	ns
t2 TDR valid after TEN↓			T		ns
t3 Bit duration			2T		ns
t4 Data duration			14T		ns
t5 TEN low hold time after last bit			T		ns
t6 TEN setup time (low to high) before CK13M high				T/2	ns

Note : T = CK13M clock period = 77ns



3.4.16 Micro-controller serial port (USP)

The micro-controller serial port is a standard synchronous serial port. It consists in three terminals, data transmit (UDX), data receive (UDR) and port enable (UEN). The clock signal is the CK13M master clock.

Transfers are initiated by the external micro-controller which push data into the USP via UDR while synchronously data contained in the transmit buffer of the USP are pushed out via UDX.

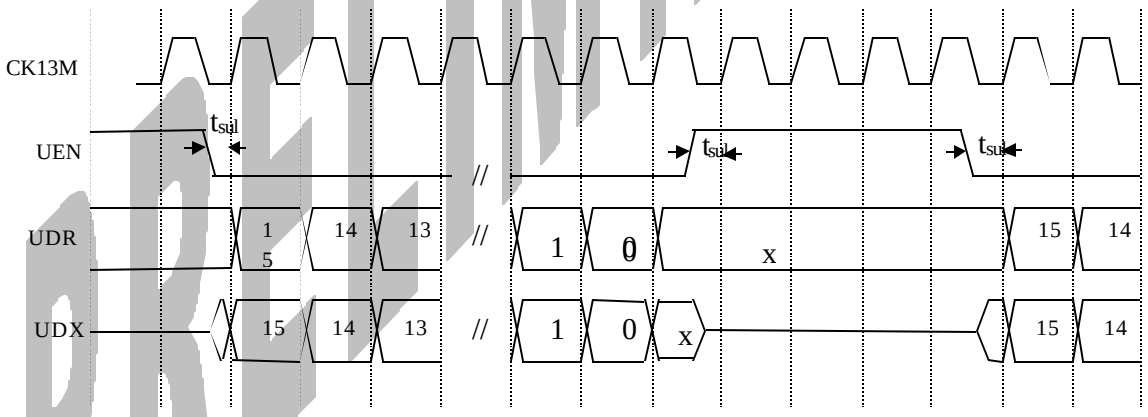
The micro-controller serial port allows read and write access of all internal registers under the arbitration of the internal bus controller.

Between to consecutive USP access, there must be a minimum of 8 CK13M or CK32K rising edge (depending of ACTIVMCLK status).

USP interface timings requirements

Parameter	Conditions	Min	Typ	Max	Units
tsu1 UEN setup delay before CK13M↑			20		ns
th1 UEN hold after CK13M↑ - (CK13M period - t1)			50		ns
tsu2 UDR setup delay before CK13M low			20		ns
th2 UDR hold after CK13M↓			20		ns
td1 UDX delay after CK13M↓			20		ns
Time between continuous words		8			T

Note : T = CK13M clock period = 77ns (ACTIVMCLK='1') or T = CK32K (ACTIVMCLK='0')



Receive and Transmit **USP** Operations

3.4.17 Test access port (TAP)

The test access port (TAP) meets JTAG testability standard (IEEE Std1131.1-1990). TAP allows public instructions set of JTAG standard and also private instructions to configure the device in special modes for test or debug purpose.

Four pins are dedicated to the TAP (TCK, TMS, TDI, TDO).

JTAG Interface timings requirements

Parameter	Conditions	Min	Typ	Max	Units
Setup time TMS to TCK ↑		20			ns
Setup time TDI to TCK ↑		20			ns
Delay time TDO from TCK ↑				20	ns

JTAG ID Code

Variant	Part Number	Manufacturer	LSB
0000	0000 0000 0110 0110	0000 0010 111	1

3.4.18 Public instructions

As defined in IEEE Std1149.1 the public instructions are:

NAME	OPCODE	DESCRIPTION
BYPASS	111111 (63)	Connects the by-pass register between TDI and TDO
EXTEST	000000 (00)	Connects the boundary scan register between TDI & TDO. This mode allows to capture the state of the inputs pins and to force the state of the output pins. (For example it can be used for printed circuit board connections test)
IDCODE	000001 (01)	Connects the identification register between TDI and TDO. This is the default configuration at reset.
SAMPLE/ PRELOAD	000010 (02)	Connects the boundary scan register between TDI & TDO. This mode allows to capture a snapshot of the state of the I/O's of the device.
INTEST	001001 (09)	Connects the boundary scan register between TDI & TDO. This mode allows to force the internal system input signals via the parallel latches of the boundary register and to capture internal system outputs. (This mode can be used for device internal test independently of the state of its input pins). The internal master clock is derived from TCK and is active in the Run-Test-Idle state of the state machine to allow single step operation of the device.

3.4.19 Private instructions:

A private instructions set exists for the specific test features.

In addition to the *public* instruction set, ABB chip contains a set of *private* instructions, in order to put the device in the various test configurations.
The private instructions set connects specific internal signals to the four dedicated pins TEST1, TEST2, TEST3 and TEST4. These pins are I/O's, set to INPUTS by default, and have pull-up devices to insure a driven state to the internal bus in this case.

CONFIG NAME	OPCODE	DESCRIPTION			
BSPLOOP	000111 (07)	The data written to any register is automatically sent back (read) by the Bus Controller.			
VSPLOOP	001010 (10)	Connects the output of the Voice Serial Interface to its input. This is done in the Filter.			
AFCTEST	010000 (16)	AFCA test: connects the internal data bus (bit7 to bit0) directly to the input of the AFCA.			
MADCTEST	010010 (18)	Connects TEST pin on the MADC outputs			
		1-O	ADC_END_IT	3-I	Not used
		2-O	ADC_END_IT	4-I	Not used
TSPADC	010101 (21)	Connects Baseband window control signals on the test pins.			
		1-I	Not used	3-O	BULENA
		2-I	Not used	4-O	STARTADC
TSPUP	010111 (23)	Connects Baseband window control signals on the test pins			
		1-I	Not used	3-O	BULON
		2-I	Not used	4-O	BULENA
TSPDN	011000 (24)	Connects Baseband window control signals on the test pins			
		1-I	Not used	3-O	BDLON
		2-I	Not used	4-O	BDLENA
TSPENA	011010 (26)	Connects Baseband window control signals on the test pins.			
		1-I	Not used	3-O	BULENA
		2-I	Not used	4-O	BDLENA
TSPTEST1	011101 (29)	Connects Baseband window control signals on the test pins.			
		1-O	BULON	3-O	BDLON
		2-O	BULENA	4-O	BDLENA
TSPTEST2	011110 (30)	Connects Baseband window control signals and the ADC conversion start bit on the test pins.			
		1-O	BULCAL	3-O	STARTADC
		2-O	BDLCAL	4-I	Not used
APCRAMP	011111 (31)	Connects Ramp window control signals on the test pins.			
		1-I	External RAMP pulse	3-O	CKAPC
		2-I	Not used	4-O	BULDRAMP internal

4. DATA AND ADDRESS FORMAT

Writing or reading registers via a serial interface is done by transferring 16 bit words to the serial interface.

Internal Registers Operations

Each word is split in three fields.

Data										Address					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	1 / 0

Writing to internal registers:

Bit 0 : At **0** (zero) it indicates a write operation.
Bit 1 to 5 : This field shall contain the address of the register to be accessed.
Bit 6 to 15 : This field shall contain the data to be written into the internal register.

Reading from internal registers:

Bit 0 : At **1** (one) it indicates a read operation.
Bit 1 to 5 : This field shall contain the address of the register to be accessed.
Bit 6 to 15 : This filed don't care in a read request operation.

Baseband Burst Operations

During reception of a burst, transfer of radio data from the downlink baseband codec is done via the TX part of the BSP serial interface in the following 16 bit word format.

Data															I/Q
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

As the I/Q samples are coded with 16 bit words, the data rate is 8.66 Mbps (or 270833 * 16 * 2) . As the digital clock MCLK is 13 MHz, the transfer will done at 13 Mbps in burst mode: during burst reception the DSP serial interface will be idled about 33% of the time.

Address format

Because the number of registers is greater than 32, the ABB internal address bus will have **6** bits. But with each word only **5** address bits are transmitted by the Baseband Serial Port or by the Micro controller Serial Port. So a page register has been added. Through this register the **MSB** from the internal address can be set to 1 or to 0 **independently** for and by each serial port. The write access address to this 'page selection' register is **1** from **page 0** or **1**. It has no read access.

5. PIN DESCRIPTIONS

BSP : 4 Pins	Type	Description	Supplies	Comment	Pin #
BFSX	DIGOUT	Baseband serial port transmit data and frame synchronization	VRIO / GNDD		27
BDX	DIGOUT	Baseband serial port transmit data	VRIO / GNDD		26
BFSR	DIGIN	Baseband serial port receive frame synchronization	VRIO / GNDD		29
BDR	DIGIN	Baseband serial port receive data	VRIO / GNDD		28

TSP : 4 Pins	Type	Description	Supplies	Comment	Pin #
TDR	DIGIN	Time serial port input data	VRIO / GNDD		21
TEN	DIGIN	Time serial port enable	VRIO / GNDD		22
TEST1	DIGIO	Special Test I/O pin – Multiplex with INT1	VRIO / GNDD	INT1 pin	-
TEST2	DIGIO	Special Test I/O pin – Multiplex with INT2	VRIO / GNDD	INT2 pin	-
TEST3	DIGIO	Special Test I/O pin	VRIO / GNDD	Pull-up	40
TEST4	DIGIO	Special Test I/O pin	VRIO / GNDD	Pull-up	63

USP : 3 Pins	Type	Description	Supplies	Comment	Pin #
UDX	DIGOUT	Micro-controller serial port transmit data	VRIO / GNDD	Tristate	35
UDR	DIGIN	Micro-controller serial port receive data	VRIO / GNDD		34
UEN	DIGIN	Micro-controller serial port enable	VRIO / GNDD		39

CKG : 1 Pin	Type	Description	Supplies	Comment	Pin #
CK13M	DIGIN	13 MHz master clock input	VRIO / GNDD		12

TAP : 4 Pins	Type	Description	Supplies	Comment	Pin #
TCK	DIGIN	Scan test clock	VRIO / GNDD	Pull-down	71
TMS	DIGIN	JTAG test mode select	VRIO / GNDD	Pull-up	66
TDI	DIGIN	Scan path input	VRIO / GNDD	Pull-up	68
TDO	DIGOUT	Scan path output	VRIO / GNDD	Tristate	67

VSP : 4 Pins	Type	Description	Supplies	Comment	Pin #
VCK	DIGOUT	Voiceband serial port clock	VRIO / GNDD		30
VFS	DIGOUT	Voiceband serial port frame synchronization	VRIO / GNDD		37
VDR	DIGIN	Voiceband serial port receive data	VRIO / GNDD		38
VDX	DIGOUT	Voiceband serial port transmit data	VRIO / GNDD		36

AXD : 6 Pins	Type	Description	Supplies	Comment	Pin #
LEDA	ANIN	LED driver, paging	VBAT/ GNDL		78
LEDB1	ANIN	LED driver, backlight input 1	VBAT/ GNDL		74
LEDB2	ANIN	LED driver, backlight input 2	VBAT/ GNDL		75
LEDC	ANIN	LED driver, charging indicator	VCHG/VBAT/ GNDL		79
GNDL1	GND	Ground for LED driver	GNDL		76
GNDL2	GND	Ground for LED driver	GNDL		77

IBIC: 1 Pin	Type	Description	Supplies	Comment	Pin #
INT2	DIGIO	Micro-controller interrupt (INT2)	VRIO / GNDD		88

VRPC: 11 Pins	Type	Description	Supplies	Comment	Pin #
RPWON	DIGIN	Remote Power On (Other than button)	VBAT / GNDD	Pull-up	62
PWON	DIGIN	On button input	VBAT / GNDD	Pull-up	61
ITWAKEUP	DIGIN	Auxiliary power on input	VRRTC / GNDD		6
INT1	DIGIO	Fast interrupt (INT1)	VRIO / GNDD		41
RESPWONZ	DIGOUT	Digital BaseBand Reset (@ power on reset)	VRRTC / GNDD		8
ONNOFF	DIGOUT	Digital BaseBand Reset (@ each switch on)	VRRTC / GNDD		11
VREF	ANIO	Reference voltage (1.2V)	VCABB / REFGND		80
REFGND	ANIO	Reference voltage ground	REFGND		82
IBIAS	ANIO	Bias current reference resistor (100K)	VCABB / REFGND		81
TESTRESETZ	DIGIN	RESET input for test mode only	UPR / GNDD	Pull-up	54
CK32K	DIGIN	32Khz clock input	VRRTC / GNDD		10

VBC : 12 Pins	Type	Description	Supplies	Comment	Pin #
MICIP	ANIN	Microphone 1 amplifier input (+)	VRABB / GNDAV		45
MICIN	ANIN	Microphone 1 amplifier input (-)	VRABB / GNDAV		46
MICBIAS	ANOUT	Microphone bias supply	VRABB / GNDAV		48
HSO	ANOUT	Headset 32 ohm driver (single ended)	VRABB / GNDA		53
HSMICP	ANIN	Headset Microphone amplifier input (single ended)	VRABB / GNDAV		44
HSMICBIAS	ANOUT	Headset Microphone bias supply	VRABB / GNDAV		47
AUXOP	ANOUT	Auxiliary hands free amplifier output (+)	VRABB / GNDA		49
AUXON	ANOUT	Auxiliary hands free amplifier output (-)	VRABB / GNDA		50
AUXI	ANIN	Auxiliary hands free signal input	VRABB / GNDAV		43
GNDAV	ANIO	MICBIAS and AUXI ground	REFGRND		42
EARP	ANOUT	Earphone amplifier output (+)	VRABB / GNDA		51
EARN	ANOUT	Earphone amplifier output (-)	VRABB / GNDA		52

ADAC : 1 Pin	Type	Description	Supplies	Comment	Pin #
DAC	ANOUT	Auxiliary 10 bit DAC output	VRABB / REFGND		33

AFC : 1 Pin	Type	Description	Supplies	Comment	Pin #
AFC	ANOUT	Automatic frequency control DAC output	VRABB / GNDA		31

APC : 1 Pins	Type	Description	Supplies	Comment	Pin #
APC	ANOUT	Automatic power control DAC output	VRABB / GNDA		32

BBC : 8 Pins	Type	Description	Supplies	Comment	Pin #
BDLQM	ANIN	Quadrature input (Q-) baseband codec downlink	VRABB / GNDA		65
BDLQP	ANIN	Quadrature input (Q+) baseband codec downlink	VRABB / GNDA		64
BDLIM	ANIN	In-phase input (I-) baseband codec downlink	VRABB / GNDA		59
BDLIP	ANIN	In-phase input (I-) baseband codec downlink	VRABB / GNDA		60
BULQM	ANOUT	Quadrature output (Q-) baseband codec uplink	VRABB / GNDA		73
BULQP	ANOUT	Quadrature output (Q+) baseband codec uplink	VRABB / GNDA		72
BULIM	ANOUT	In-phase output (I-) baseband codec uplink	VRABB / GNDA		69
BULIP	ANOUT	In-phase output (I+) baseband codec uplink	VRABB / GNDA		70

MADC: 4 Pins	Type	Description	Supplies	Comment	Pin #
ADIN1	ANIN	Monitoring ADC input 1 (Battery temp)	VRABB / GNDA		85
ADIN2	ANIN	Monitoring ADC input 2 (Battery type)	VRABB / GNDA		84
ADIN3	ANIN	Monitoring ADC input 3 (Spare)	VRABB / GNDA		83
ADIN4	ANIN	Monitoring ADC input 4	VRABB / GNDA		86

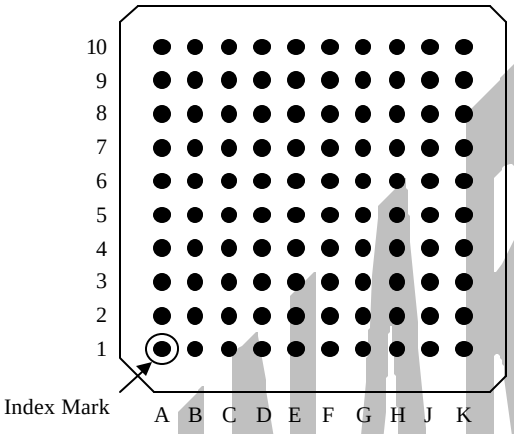
BCI: 6 Pins	Type	Description	Supplies	Comment	Pin #
VBAT	ANIN	Battery voltage input	VBAT / GNDA		94
VCHG	ANIN	Charger voltage sense input	VCHG / GNDA		89
ICTL	ANOUT	Charger current control	VCHG / GNDA		87
VBATS		Battery voltage sense input	VBAT / GNDA		91
VCCS		Charger transistor sense	VCHG / GNDA		92
PCHG		Battery Precharge Current	VCHG / GNDA		90

SIM: 6 Pins	Type	Description	Supplies	Comment	Pin #
DBBSCK	DIGIN	Sim card clock shifter input	VRIO / GNDD		17
DBBSIO	DIGIO	Sim card io shifter to/from DBB	VRIO / GNDD		13
DBBSRST	DIGIN	Sim card reset shifter input	VRIO / GNDD		18
SIMCK	DIGOUT	Sim card clock shifter output	VRSIM / GNDD		96
SIMIO	DIGIO	Sim card io shifter to/from SIMCARD	VRSIM / GNDD		98
SIMRST	DIGOUT	Sim card reset shifter output	VRSIM / GNDD		93

VREG: 23 Pins	Type	Description	Supplies	Comment	Pin #
GNDD	PWIO	Power ground return for VRDBB, VRTC, VRMEM, VRIO, VRRAM	GNDD		97
VCDBB	PWIN	Regulator DBB input	VBAT / GNDD		25
VRDBB	PWOUT	Regulator DBB output	VRDBB / GNDD		24
VSDBB	ANIN	Regulator DBB input feedback	VRDBB / GNDD		23
VCIO1	PWIN	Regulator IO input 1	VBAT / GNDD		99
VCIO2	PWIN	Regulator IO input 2	VBAT / GNDD		100
VRIO1	PWOUT	Regulator IO output 1	VRIO / GNDD		1
VRIO2	PWOUT	Regulator IO output 2	VRIO / GNDD		2
VRSIM	PWOUT	Regulator SIM output	VRSIM / GNDD		95
VCMEM	PWIN	Regulator MEM input	VBAT / GNDD		20
VCRAM	PWIN	Regulator RAM input	VBAT / GNDD		15
VLMEM	DIGIN	Regulator MEM output selection bit	VBAT / GNDD		16
VRMEM	PWOUT	Regulator MEM output	VRMEM / GNDD		19
VRRAM	PWOUT	Regulator RAM output	VRRAM / GNDD		14
GNDA	PWIO	Power ground return for VRABB	GNDA		57
VCABB	PWIN	Regulator ABB input	VBAT / GNDD		56
VRABB	PWOUT	Regulator ABB output	VRABB / GNDD		55
VBACKUP	PWIN	Backup battery input	VBACKUP / GNDD		9
UPR	PWOUT	Uninterrupted power rail output	VBAT / VBACKUP GNDD		3
VRRTC	PWOUT	Regulator RTC output	VRRTC / GNDD		7
VLRTC	DIGIN	Regulator RTC output selection bit	UPR / GNDD		4
VXRTC	ANIN	Regulator RTC auxiliary output	VRRTC / GNDD		5
TESTV	ANOUT	Regulator RDBB, RIO, RABB, RMEM, RRAM output sense (Reserved for test purpose)	VBAT / GNDD		58

Total Pins	100			

Package 100 GGM (TOP VIEW)



PIN#		GGM BALL#	PIN#		GGM BALL#	PIN#		GGM BALL#	PIN#		GGM BALL#
1	-	B2	26	-	J2	51	-	J9	76	-	B9
2	-	B1	27	-	K2	52	-	J10	77	-	A9
3	-	C2	28	-	J3	53	-	H9	78	-	B8
4	-	C3	29	-	H3	54	-	H8	79	-	C8
5	-	C1	30	-	K3	55	-	H10	80	-	A8
6	-	D2	31	-	J4	56	-	G9	81	-	B7
7	-	D1	32	-	K4	57	-	G10	82	-	A7
8	-	D3	33	-	H4	58	-	G8	83	-	C7
9	-	E1	34	-	K5	59	-	F10	84	-	A6
10	-	E2	35	-	J5	60	-	F9	85	-	B6
11	-	E3	36	-	H5	61	-	F8	86	-	C6
12	-	E4	37	-	G5	62	-	F7	87	-	D6
13	-	E5	38	-	F5	63	-	F6	88	-	E6
14	-	F1	39	-	K6	64	-	E10	89	-	A5
15	-	F2	40	-	J6	65	-	E9	90	-	B5
16	-	F3	41	-	H6	66	-	E8	91	-	C5
17	-	F4	42	-	G6	67	-	E7	92	-	D5
18	-	G4	43	-	G7	68	-	D7	93	-	D4
19	-	G1	44	-	K7	69	-	D10	94	-	A4
20	-	G2	45	-	J7	70	-	D9	95	-	B4
21	-	G3	46	-	H7	71	-	D8	96	-	C4
22	-	H1	47	-	K8	72	-	C10	97	-	A3
23	-	H2	48	-	J8	73	-	C9	98	-	B3
24	-	J1	49	-	K9	74	-	B10	99	-	A2
25	-	K1	50	-	K10	75	-	A10	100	-	A1

6. REGISTERS CROSS-REFERENCE

6.1 Page 0

Pg	Ad	Registers	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	-	-	-	-	-	-	-	-	-	-	-
0①	1	PAGEREG	-	-	-	-	-	-	BSPP1	BSPP0	UCP1	UCP0
0	2	APCDEL1	DELD4	DELD3	DELD2	DELD1	DELD0	DELU4	DELU3	DELU2	DELU1	DELU0
0	3	BULDATA1/2	BIT0	//	//	//	//	//	//	//	//	BIT159
0	4	TOGBR1	MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR
0	5	TOGBR2	-	-	-	IAPCTR	IBFPT2	IBFPT1	ACTS	ACTR	KEEPS	KEEPR
0	6	VBDR	-	-	-	VOLCTL2	VOLCTL1	VOLCTL0	VDLPG 3	VDLPG 2	VDLPG 1	VDLPG 0
0	7	AUXAFC1	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	8	AUXAFC2	-	-	-	-	-	-	-	BIT12	BIT11	BIT10
0	9	AUXAPC	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	10	APCRAM	DW0	to	DW15	//	//	//	//	UP-0	to	UP15
0	11	APCOFF	-	-	-	-	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	12	AUXDAC	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	13	MADCCTRL	-	-	-	ADIN3	ADIN2	ADIN1	VBKP	ICHG	VCHG	VBAT
0	14	-	-	-	-	-	-	-	-	-	-	-
0	15	VBATREG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	16	VCGHREG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	17	ICGHREG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	18	VBKPREG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	19	ADIN1REG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	20	ADIN2 REG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	21	ADIN3REG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	22	ADIN4REG	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	23	-	-	-	-	-	-	-	-	-	-	-
0	24	MADCSTATUS	-	-	-	-	-	-	-	-	-	ADCBUSY
0	25	CHGREG	CHG9	CHG8	CHG7	CHG6	CHG5	CHG4	CHG3	CHG2	CHG1	CHG0
0	26	ITMASKREG	-	-	-	-	ADCND	-	CHRGER	PUSHOF	REMOT	-
0①	27	ITSTATREG	-	-	-	-	ADCND	-	CHRGER	PUSHOF	REMOT	-
0	28	BCICTL1	-	RSV	TYPEN	THEN	THSENS2	THSENS1	THSENS0	-	DACNBUF	MESBAT
0	29	BCICTL2	RSV	RSV	PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHPASSPA	CHIV	CHEN
0	30	VRPCDEV	-	-	-	-	-	-	-	-	DEVSLP	DEVOFF
0	31	VRPCSTS	-	-	-	CHGPRE	ONMRFLT	ONREFLT	CHGSTS	ITWSTS	ONRSTS	ONBSTS

① This register as two addresses one in page 0 and the same in page 1.

6.2 Page 1

Pg	Ad	Registers	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	-	-	-	-	-	-	-	-	-	-	-
1①	1	PAGEREG	-	-	-	-	-	-	BSPP1	BSPP0	UCP1	UCP0
1	2	BULIOFF	-	ULIOFF8	ULIOFF7	ULIOFF6	ULIOFF5	ULIOFF4	ULIOFF3	ULIOFF2	ULIOFF1	ULIOFF0
1	3	BULQOFF	-	ULQOFF8	ULQOFF7	ULQOFF6	ULQOFF5	ULQOFF4	ULQOFF3	ULQOFF2	ULQOFF1	ULQOFF0
1	4	BULQDAC	ULQD9	ULQD8	ULQD7	ULQD6	ULQD5	ULQD4	ULQD3	ULQD2	ULQD1	ULQD0
1	5	BULIDAC	ULID9	ULID7	ULID7	ULID6	ULID5	ULID4	ULID3	ULID2	ULID1	ULID0
1	6	BBCTL	EXTCAL	OUTLV 2	OUTLV 1	OUTLV 0	MSLOT	BBMOD	BALOOP	SLVMI2	SLVMI1	SLVMI0
1	7	VBUR	DXEN	VDLST3	VDLST2	VDLST1	VDLST0	VULPG4	VULPG 3	VULPG2	VULPG 1	VULPG0
1	8	VBCR1	VFBYP	VBDFAUXG	VSYNC	VCLKM	VALOOP	MICBIA	VULSW 1	VBUZ	VDLEAR	VDLAUX
1	9	PWDNRG	-	-	-	ACTCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON
1	10	VBPOP	-	AUXAUTO	AUXCHG	AUXDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS
1	11	VBCR2	-	-	-	-	-	-	-	MICNAUX	VDLHSO	MICBIASEL
1	12	APCOUT	APC9	APC8	APC7	APC6	APC5	APC4	APC3	APC2	APC1	APC0
1	13	BCICONF	-	BBSEL1	BBSEL0	MESBB	BBCHGEN	OFFEN	OFFSN3	OFFSN2	OFFSN1	OFFSN0
1	14	BULGCAL	-	QAG3	QAG2	QAG1	QAG0	-	IAG3	IAG2	IAG1	IAG0
1	15	-	-	-	-	-	-	-	-	-	-	-
1	16	-	-	-	-	-	-	-	-	-	-	-
1	17	-	-	-	-	-	-	-	-	-	-	-
1	18	-	-	-	-	-	-	-	-	-	-	-
1	19	TAPCTL	-	-	-	-	-	-	-	-	-	TAPEN
1	20	TAPREG	HEAD3	HEAD2	HEAD1	HEAD0	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
1	21	AFCCTLADD	-	-	-	-	-	-	-	AFCBYP	AFCK1	AFCK0
1	22	AFCOUT	-	-	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0
1	23	VRPCSIM	-	-	-	-	-	-	SIMLEN	SIMRSU	SIMEN	SIMSEL
1	24	ACDLED	-	-	-	-	-	-	-	-	LEDB	LEDA
1	25	-	-	-	-	-	-	-	-	-	-	-
1	26	APCDEL2	DELD9	DELD8	DELD7	DELD6	DELD5	DELU9	DELU8	DELU7	DELU6	DELU5
1①	27	ITSTATREG	-	-	-	-	ADCND	-	CHRGER	PUSHOF	REMOT	-
1	28	-	-	-	-	-	-	-	-	-	-	-
1	29	VRPCMSK2	-	-	-	-	-	-	-	-	MSKOFF ABB	MSKSLP ABB
1	30	VRPCCFG	-	RRTC1	RRTC0	RDBB1	RDBB0	SLPDLY4	SLPDLY3	SLPDLY2	SLPDLY1	SLPDLY0
1	31	VRPCMSK1	MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO

① This register as two addresses one in page 0 and the same in page 1.

7. VOICE REGISTERS

7.1 Voice band Control Register : VBCR

Name : VBCR1	Description : Voice band control register 1									Address : 8		Page : 1			R/W
VFBYP	VBDFAUXG	VSYNC	VCLKMODE	VALOOP	MICBIAS	VULSWIT	VBUZ	VDLEAR	VDLAUX	0	1	0	0	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

VDLAUX : Enable the auxiliary output amplifier if the VDLON bit is 1

VDLEAR : Enable the Ear amplifier, if the VDLON bit is 1

VBUZ : When this bit is set, the Auxiliary and Ear stage are powered down even if VDLAUX or VDLEAR are 1.

VULSWITCH : Enables the auxiliary input if 0 enables MICIN if 1 (and bit VULON is 1).

MICBIAS : When MICBIAS=0, the analog bias for the electric microphone and external decoupling is driven to 2V; when the value is 1 the bias is to 2.5V.

VALOOP : When this bit is set to 1, the internal analog loop of the output samples is sent to the audio input terminal. To avoid saturation of the analog path in this mode you must set:
PGA downlink = -6 dB, PGA uplink = 0 dB, Volume = 0dB and Sidetone = MUTE

VCLKMODE : When cleared to 0, this bit allows selection of the VCK in burst mode. When set to 1, this bit allows selection of the VCK in continuous mode.

VSYNC : When the bit VSYNC is set to one, The Digital Modulator, the digital Voice Serial Port and the Digital Filter can be reseted externally using VDR input. At the reset using VDR, the Filter will set VSYNC to '0'.

VBDFAUXG : When the bit VBDFAUXG is set to '0', the gain of AUXIN amplifier is 4.6dB, when se gain of AUXIN amplifier is 28.2dB.

VFBYP : When the bit VFBYP is set at '0', the filter is not bypassed. If set at '1', the filter is bypassed.

Name : VBCR2	Description : Voice band control register 2										Address : 11		Page : 1			R/W
-	-	-	-	-	-	-	MICNAUX	VDLHSO	MICBIASEL	0	1	0	1	1	1 / 0
R	R	R	R	R	R	R	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

MICBIASEL : When bit is set at '1' the HSMICBIAS is active else the MICBIAS is active.

VDLHSO : Enable the head set output amplifier if the VDLON bit is '1'

MICNAUX : When bit is set at '1' the HSMIC input is used else it is the AUXI input (those inputs are multiplexed in ABB)

7.2 Voice band pop cancellation register : VPOP

Name : VPOP	Description : Voice band pop cancellation									Address : 10	Page : 1	R/W
-	AUXAUTO	AUXCHG	AUXDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS	0 1 0 1 0		1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE		
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET		

xx = AUX / EAR / HSO , one of the VDL outputs.

xxDIS : Enable the discharge of the external capacitor
This bit has NO effect when xxCHG is set to '1
or when VDLON is set to '0'
or when VDLxx is set to '1'

xxCHG : Enable the charge of the external capacitor (up to VRABB / 2)
This bit has NO effect when VDLON is set to '0'

Mode AUTO	Mode NORMAL
This bit is set automatically to '1' when VDLON rise	This bit has NO effect when the corresponding VDLxx is set to '1'
This bit is cleared automatically to '0' when the corresponding VDLxx is ON	Write access En able/Disable the charge.
Write access have NO effect.	

xxAUTO : '1' means that xxCHG functionality runs in AUTOMATIC mode
'0' in NORMAL mode

7.3 Voice band Control Register : VBUR

Name : VBUR	Description : Voice band uplink register									Address : 7	Page : 1				R/W
DXEN	VDLST3	VDLST2	VDLST1	VDLST0	VULPG4	VULPG3	VULPG2	VULPG1	VULPG0	0	0	1	1	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

DXEN : When bit DXEN is set at '1' the VDX signal is in Mute mode. If DXEN = '0' , the VDX is in normal mode.

VDSLT[3-0] : Side tone levels.

VULPG[4-0] : Gain of the voice uplink programmable gain amplifier (-12dB to +12dB in 1 dB step) see Table

VULPG 4	VULPG 3	VULPG 2	VULPG 1	VULPG 0	Relative Gain
1	0	0	0	0	-12dB
1	0	1	1	1	-11dB
1	1	0	0	0	-10dB
1	1	0	0	1	-9dB
1	1	0	1	0	-8dB
1	1	0	1	1	-7dB
0	0	0	0	0	-6dB
0	0	0	0	1	-5dB
0	0	0	1	0	-4dB
0	0	0	1	1	-3dB
0	0	1	0	0	-2dB
0	0	1	0	1	-1dB
0	0	1	1	0	0dB
0	0	1	1	1	1dB
0	1	0	0	0	2dB
0	1	0	0	1	3dB
0	1	0	1	0	4dB
0	1	0	1	1	5dB
0	1	1	0	0	6dB
1	0	0	0	1	7dB
1	0	0	1	0	8dB
1	0	0	1	1	9dB
1	0	1	0	0	10dB
1	0	1	0	1	11dB
1	0	1	1	0	12dB

VDLST 3	VDLST 2	VDLST 1	VDLST 0	Relative Gain
1	1	0	1	-23dB
1	1	0	0	-20dB
0	1	1	0	-17dB
0	0	1	0	-14dB
0	1	1	1	-11dB
0	0	1	1	-8dB
0	0	0	0	-5dB
0	1	0	0	-2dB
0	0	0	1	1 dB
0	1	0	1	1 dB
1	0	0	0	MUTE
1	0	0	1	MUTE
1	0	1	0	MUTE
1	0	1	1	MUTE
1	1	1	0	MUTE

1	1	1	1	MUTE

7.4 Voice Band Downlink Register: VBDR

Name : VBDR			Description : Voice band downlink register							Address : 6			Page : 0		R/W
-	-	-	VOLCTL2	VOLCTL1	VOLCTL0	VDLPG3	VDLPG2	VDLPG1	VDLPG0	0	0	1	1	0	1 / 0
R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

VDLPG[3-0] : Gain of the Voice downlink programmable gain amplifier (-6dB to +6dB in 1 dB steps).
VOCTL[2-0] : Volume control (0,-6,-12,-18,-14, Mute).

VDLPG 3	VDLPG 2	VDLPG 1	VDLPG 0	Relative Gain
0	0	0	0	-6dB
0	0	0	1	-5dB
0	0	1	0	-4dB
0	0	1	1	-3dB
0	1	0	0	-2dB
0	1	0	1	-1dB
0	1	1	0	0dB
0	1	1	1	1dB
1	0	0	0	2dB
1	0	0	1	3dB
1	0	1	0	4dB
1	0	1	1	5dB
1	1	0	0	6dB
1	1	0	1	-6dB
1	1	1	0	-6dB
1	1	1	1	-6dB

VOLCTL2	VOLCTL1	VOLCTL0	Relative Gain
0	1	0	0dB
1	1	0	-6dB
0	0	0	-12dB
1	0	0	-18dB
0	1	1	-24dB
1	0	1	Mute
0	0	1	Mute
1	1	1	Mute

8. BASEBAND REGISTERS

8.1 Baseband uplink registers

Name : BULIOFF Description : Baseband Uplink I Offset Register										Address : 2 Page : 1					R/W
-	ULIOFF8	ULIOFF7	ULIOFF6	ULIOFF5	ULIOFF4	ULIOFF3	ULIOFF2	ULIOFF1	ULIOFF0	0	0	0	1	0	1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	1	1	1	1	1	1	1	1	<--- VALUE AT RESET					

ULIOFF [8-0] : Value of the offset on I channel.
W access is disabled during offset calibration (BULCAL high).

Name : BULQOFF Description : Baseband Uplink Q Offset Register										Address : 3 Page : 1					R/W
-	ULQOFF8	ULQOFF7	ULQOFF6	ULQOFF5	ULQOFF4	ULQOFF3	ULQOFF2	ULQOFF1	ULQOFF0	0	0	0	1	1	1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	1	1	1	1	1	1	1	1	<--- VALUE AT RESET					

ULQOFF [8-0] : Value of the offset on Q channel.
W access is disabled during offset calibration (BULCAL high).

Name : BULIDAC Description : Baseband Uplink I DAC register										Address : 5 Page : 1					R/W
ULIDAC9	ULIDAC8	ULIDAC7	ULIDAC6	ULIDAC5	ULIDAC4	ULIDAC3	ULIDAC2	ULIDAC1	ULIDAC0	0	0	1	0	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	1	1	1	1	1	1	1	1	1	<--- VALUE AT RESET					

ULIDAC [9-0] : Data applied digital to analog converter of I channel.
Write is disabled during modulation.

Name : BULQDAC Description : Baseband Uplink Q DAC register										Address : 4 Page : 1					R/W
ULQDAC9	ULQDAC8	ULQDAC7	ULQDAC6	ULQDAC5	ULQDAC4	ULQDAC3	ULQDAC2	ULQDAC1	ULQDAC0	0	0	1	0	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

ULQDAC [9-0] : Data applied digital to analog converter of Q channel.
Write is disabled during modulation.

Name : BULGCAL Calibration Description : Baseband Uplink Absolute Gain										Address : 14 Page : 1					R/W
-	QAG3	QAG2	QAG1	QAG0	-	IAG3	IAG2	IAG1	IAG0	0	1	1	1	0	1 / 0
R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

IAG [3-0] : Absolute Gain calibration for I DAC
QAG [3-0] : Absolute Gain calibration for Q DAC

[I,Q]AG[3:0]	Relative Gain
0000	0dB
0001	+0.27dB
0010	+0.53dB
0011	+0.78dB

[I,Q]AG[3:0]	Relative Gain
0000	0dB
1111	-0.27dB
1110	-0.56dB
1101	-0.85dB

0100	+1.02dB
0101	+1.26dB
0110	+1.49dB

1100	-1.16dB
1011	-1.48dB
1010	-1.80dB

Name : BULDATA1 Description : Baseband Uplink Data Buffer 1										Address : 3 Page : 0 (16 words)					W
BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	BIT8	BIT9	0	0	0	1	1	0
BIT10	BIT11	BIT12	BIT13	BIT14	BIT15	BIT16	BIT17	BIT18	BIT19	0	0	0	1	1	0
BIT20	BIT21	BIT22	BIT23	BIT24	BIT25	BIT26	BIT27	BIT28	BIT29	0	0	0	1	1	0
BIT30	BIT31	BIT32	BIT33	BIT34	BIT35	BIT36	BIT37	BIT38	BIT39	0	0	0	1	1	0
BIT40	BIT41	BIT42	BIT43	BIT44	BIT45	BIT46	BIT47	BIT48	BIT49	0	0	0	1	1	0
BIT50	BIT51	BIT52	BIT53	BIT54	BIT55	BIT56	BIT57	BIT58	BIT59	0	0	0	1	1	0
BIT60	BIT61	BIT62	BIT63	BIT64	BIT65	BIT66	BIT67	BIT68	BIT69	0	0	0	1	1	0
BIT70	BIT71	BIT72	BIT73	BIT74	BIT75	BIT76	BIT77	BIT78	BIT79	0	0	0	1	1	0
BIT80	BIT81	BIT82	BIT83	BIT84	BIT85	BIT86	BIT87	BIT88	BIT89	0	0	0	1	1	0
BIT90	BIT91	BIT92	BIT93	BIT94	BIT95	BIT96	BIT97	BIT98	BIT99	0	0	0	1	1	0
BIT100	BIT101	BIT102	BIT103	BIT104	BIT105	BIT106	BIT107	BIT108	BIT109	0	0	0	1	1	0
BIT110	BIT111	BIT112	BIT113	BIT114	BIT115	BIT116	BIT117	BIT118	BIT119	0	0	0	1	1	0
BIT120	BIT121	BIT122	BIT123	BIT124	BIT125	BIT126	BIT127	BIT128	BIT129	0	0	0	1	1	0
BIT130	BIT131	BIT132	BIT133	BIT134	BIT135	BIT136	BIT137	BIT138	BIT139	0	0	0	1	1	0
BIT140	BIT141	BIT142	BIT143	BIT144	BIT145	BIT146	BIT147	BIT148	BIT149	0	0	0	1	1	0
BIT150	BIT151	BIT152	BIT153	BIT154	BIT155	BIT156	BIT157	BIT158	BIT159	0	0	0	1	1	0
W	W	W	W	W	W	W	W	W	W	<--- ACCESS TYPE					
1	1	1	1	1	1	1	1	1	1	<--- VALUE AT RESET					

BIT0 to BIT159 : Bits composing the sequence of the burst to be send. BIT 0 is transmitted first.
For a normal burst, burst buffer should be loaded as follows :

- Bit0 to Bit 3 : 4 guard bits .
- Bit4 to Bit 6 : 3 tail bits.
- Bit7 to Bit 64 : 58 data bits.
- Bit 65 to Bit 90 : 26 training sequence bits.
- Bit 91 to Bit 148 : 58 data bits.
- Bit 149 to bit 151 : 3 tail bits.
- Bit 152 to bit 159 : 8 guard bits.

At reset and after each transmission the burst buffer is re-initialized with guard bits (all bits at 1).

Name : BULDATA2 Description : Baseband Uplink Data Buffer 2										Address : 3 Page : 0 (16 words)					W
BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	BIT8	BIT9	0	0	0	1	1	0
BIT10	BIT11	BIT12	BIT13	BIT14	BIT15	BIT16	BIT17	BIT18	BIT19	0	0	0	1	1	0
BIT20	BIT21	BIT22	BIT23	BIT24	BIT25	BIT26	BIT27	BIT28	BIT29	0	0	0	1	1	0
BIT30	BIT31	BIT32	BIT33	BIT34	BIT35	BIT36	BIT37	BIT38	BIT39	0	0	0	1	1	0
BIT40	BIT41	BIT42	BIT43	BIT44	BIT45	BIT46	BIT47	BIT48	BIT49	0	0	0	1	1	0
BIT50	BIT51	BIT52	BIT53	BIT54	BIT55	BIT56	BIT57	BIT58	BIT59	0	0	0	1	1	0
BIT60	BIT61	BIT62	BIT63	BIT64	BIT65	BIT66	BIT67	BIT68	BIT69	0	0	0	1	1	0
BIT70	BIT71	BIT72	BIT73	BIT74	BIT75	BIT76	BIT77	BIT78	BIT79	0	0	0	1	1	0
BIT80	BIT81	BIT82	BIT83	BIT84	BIT85	BIT86	BIT87	BIT88	BIT89	0	0	0	1	1	0
BIT90	BIT91	BIT92	BIT93	BIT94	BIT95	BIT96	BIT97	BIT98	BIT99	0	0	0	1	1	0
BIT100	BIT101	BIT102	BIT103	BIT104	BIT105	BIT106	BIT107	BIT108	BIT109	0	0	0	1	1	0
BIT110	BIT111	BIT112	BIT113	BIT114	BIT115	BIT116	BIT117	BIT118	BIT119	0	0	0	1	1	0
BIT120	BIT121	BIT122	BIT123	BIT124	BIT125	BIT126	BIT127	BIT128	BIT129	0	0	0	1	1	0
BIT130	BIT131	BIT132	BIT133	BIT134	BIT135	BIT136	BIT137	BIT138	BIT139	0	0	0	1	1	0
BIT140	BIT141	BIT142	BIT143	BIT144	BIT145	BIT146	BIT147	BIT148	BIT149	0	0	0	1	1	0
BIT150	BIT151	BIT152	BIT153	BIT154	BIT155	BIT156	BIT157	BIT158	BIT159	0	0	0	1	1	0
W	W	W	W	W	W	W	W	W	W	<--- ACCESS TYPE					
1	1	1	1	1	1	1	1	1	1	<--- VALUE AT RESET					

The BULDATA2 register is use for multislots modulation, while data in BULDATA1 are modulated and transmit in a GSM slot, data are write in BULDATA2. At the following slot, data from BULDATA2 are transmit while data are write in BULDATA1.

8.2 Baseband control registers

Name : BBCTL Description : Baseband codec control register										Address : 6 Page : 1					R/W
EXTCAL	OUTLEV2	OUTLEV1	OUTLEV0	MSLOT	BBMOD	BALOOP	SELVMID2	SELVMID1	SELVMID0	0	0	1	1	0	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

EXTCAL : Downlink auto calibration mode. When 0 internal autocalibration (differential (IN,IP) are shorted , (QN,QP) are shorted) when 1 external calibration.

SELVMID [2-0] : Select the value of output common mode of baseband uplink.

SELVMID2	*SELVMID1*	*SELVMID0*	*Output common mode*
0	0	0	VRABB / 2
0	0	1	1.35 V
0	1	0	1.45 V
0	1	1	VREF
1	0	0	1.25
1	0	1	1.25
1	1	0	1.25
1	1	1	1.25

BALOOP : when 1, internal analog loop of I/Q uplink pins to the I/Q downlink pins. (internal calibration is also masked)

BBMOD : when 0, enable GMSK mode

MSLOT : when 1, modulator is in multislot mode

OUTLEV[2:0] : Select the value of the Baseband output level.

OUTLEV2	*OUTLEV1*	*OUTLEV0*	*Output level(Vpp)*
0	0	0	$2 \times V_{VREF}$
0	0	1	$(16/15) \times V_{VREF}$
0	1	0	$(22/15) \times V_{VREF}$
0	1	1	$(8/15) \times V_{VREF}$
1	0	0	$(18/15) \times V_{VREF}$
1	0	1	$(18/15) \times V_{VREF}$
1	1	0	$(20/15) \times V_{VREF}$
1	1	1	$(20/15) \times V_{VREF}$

9. VRPC REGISTERS

Name : VRPCMSK1	Description : VPRC MASK									Address : 31	Page : 1				R/W
MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO	1	1	1	1	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

MSKSLP[IO,MEM,DBB,RAM,SIM] : '0' the regulator is in low consumption mode in SLEEP mode
'1' the regulator is disable, in SLEEP mode no regulation is provided

MSKOFF[IO,MEM,DBB,RAM,SIM] : '1' the regulator is in low consumption mode in OFF mode
'0' the regulator is disable, in OFF mode no regulation is provided

Name : VRPCMSK2	Description : VPRC MASK ABB									Address : 29	Page : 1				R/W
-	-	-	-	-	-	-	-	MSKOFF ABB	MSKSLP ABB	1	1	1	0	1	1 / 0
R	R	R	R	R	R	R	R	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	1	<--- VALUE AT RESET					

MSKSLPABB : '0' the regulator is in low consumption mode in SLEEP mode
'1' the regulator is disable, in SLEEP mode no regulation is provided

MSKOFFABB : '1' the regulator is in low consumption mode in OFF mode
'0' the regulator is disable, in OFF mode no regulation is provided

Name : VRPCCFG	Description : VPRC CONFIG									Address : 30	Page : 1				R/W
-	RRTC1	RRTC0	RDBB1	RDBB0	SLPDLY4	SLPDLY3	SLPDLY2	SLPDLY1	SLPDLY0	1	1	1	1	0	1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	1	1	1	1	1	<--- VALUE AT RESET (AFTER EACH SWITCH ON)					
0	VLRTC	0	VLRTC	0	1	1	1	1	1	<--- VALUE AT RESET (AFTER FIRST RESET)					

SLPDLY[4:0] : Delay in SLPDLY*20*T32K before going in SLEEP mode
(Code 00000 is not allowed)

RDBB1, RDBB0 : Programs VRDBB voltage
'01' = 1.2 V '00'= 1.4 V '10'= 1.8

RRTC1, RRTC0 : Programs VRRTC voltage
'01' = 1.2 V '00'= 1.4 V '10'= 1.8

Name : VRPCDEV	Description : VPRC switch off register									Address : 30	Page : 0				R/W
-	-	-	-	-	-	-	-	DEVSLP	DEVOFF	1	1	1	1	0	1 / 0
R	R	R	R	R	R	R	R	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

DEVOFF : Start the WDT to switch OFF the regulators.

DEVSLP : Start the SLPDLY and switch the ABB in SLEEP mode

Name : VRPCSTS	Description : VPRC STATUS									Address : 31	Page : 0				R
-	-	-	CHGPRES	ONMRFLT	ONREFLT	CHGSTS	ITWSTS	ONRSTS	ONBSTS	1	1	1	1	1	0
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	<--- VALUE AT RESET					

ONBSTS : Switch on Condition on ON BUTTON Push

ONRSTS : Switch on Condition on ON REM transition 0->1

ITWSTS	:	Switch on Condition on ITWAKEUP
CHGSTS	:	Switch on Condition on CHARGER PLUG
ONREFLT	:	Reflect the state of PWON pin after de bouncing
ONMRFLT	:	Reflect the state of ON_REM pin after debouncing
CHGPRES	:	Mention that the Battery Charger is plugged

10. BCI REGISTERS

Controlling the operation of the BCI requires the exchange of 2 types of programming signals between the BCI itself and the rest of the system, i.e., the Power Control state machine contained in the VRPCD of ABB , and the uC contained in Hercules

-1- some programming signals will be sent or received by the uC exclusively, when it is fully awake; the path for these signals includes the uC interface registers only.

-2- other programming signals will be also sent or received by the Power Control state machine located in VRPCD block, before the uC gets awakened; the path for these signals includes a multiplexing operation between the uC interface registers (VRIO supply domain) and the Power Control state machine. A signal driving the direction of the multiplex, will decide which device, the Power Control state machine or the uC, will send or receive programming data to or from the BCI .

10.1 Battery charger current/voltage dac register:

Name : CHGREG					Description :						Address : 25 Page : 0					R/W
CHG9	CHG8	CHG7	CHG6	CHG5	CHG4	CHG3	CHG2	CHG1	CHG0	1	1	0	0	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

CHG [9..0] : 10 Bit DAC register for setting a voltage or a current for Main Battery charging.

10.2 Battery charging Control registers

Name : BCICTL1					Description :					Address : 28 Page : 0					R/W
-	RSV	TYPEN	THEN	THSENS2	THSENS1	THSENS0	-	DACNBUF	MESBAT	1	1	1	0	0	1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

MESBAT : connects resistive divider to Main battery
DACNBUF : bypass DAC buffer
THSENS [2..0] : Set eight possible values for thermal sensor bias current
THEN : enables bias current for main battery temperature sensing
TYPEN : enables bias current for main battery type reading
RSV : reserved bit (write only '0')

Name BCICTL2					Description :					Address : 29 Page : 0					R/W
RSV	RSV	PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHPASSPA	CHIV	CHEN	1	1	1	0	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET (CHG PRESENT)					
1	1	1	1	1	1	1	1	1	1	<--- VALUE AT RESET (CHG NOT PRESENT)					

CHEN : enables the charger
CHIV : selects constant current or constant voltage charging
CHPASSPA : controls fully charge of Main Battery
CLIB : allows a zero calibration routine of the I to V converter
CHDISPA : controls charge or no charge of Main Battery
LEDC : enable the LEDC to indicate a charge
CGAIN4 : reduce the gain of the current to voltage converter from 10 to 4
PREOFF : disable the precharge
RSV : reserved bit (write only '0')

This register is supplied by VCHG.
When charger is not present, '1' value are read on each bit.

10.3 Battery charging configuration registers

Name : BCICONF					Description :					Address : 13 Page : 1					R/W
-	BBSEL1	BBSEL0	MESBB	BBCHGEN	OFFEN	OFFSN3	OFFSN2	OFFSN1	OFFSN0	1	1	1	0	0	1 / 0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	KEEP VALUE	KEEP VALUE	0	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	<--- VALUE AT RESET (AFTER EACH SWITCH ON)					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET (AFTER FIRST RESET)					

OFFSN [3..0] : Set 16 possible values for current to voltage conversion offset.
0 => +0mv N => +N*12.5mV 15 => +187.5 mV
(typical values)
OFFEN : Enable offset settings for current to voltage conversion.
BBCHGEN : Enable Back Up Battery Charger
MESBB : connects resistive divider to Back-up Battery
BBSEL[1:0] : End charging backup battery voltage offset
00 => 0mV, 01 => -100mV, 10 => -200mV, 11 => -200 mV
(typical values)

11. MADC REGISTERS

11.1 Monitoring ADC Control

Name :ADCCTRL						Description :				Address : 13 Page : 0					W
-	-	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV	0	1	1	0	1	1/0
R	R	W	W	W	W	W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

Name :ADCCTRL SHADOW						Description :				Address : 13 Page : 0					R
-	-	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV	0	1	1	0	1	1/0
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

VBATCV : This bit selects a conversion of the battery voltage. When it is high, a conversion of this input is expected during the next conversion sequence.

VCHGCV : This bit selects a conversion of the charger battery voltage. When it is high, a conversion of this input is expected during the next conversion sequence.

ICHGCV : This bit selects a conversion of the charger battery current. When it is high, a conversion of this input is expected during the next conversion sequence.

VBKPCV : This bit selects a conversion of the backup battery voltage. When it is high, a conversion of this input is expected during the next conversion sequence.

ADIN1CV : This bit selects a conversion of the ADIN1 input. When it is high, a conversion of this input is expected during the next conversion sequence.

ADIN2CV : : This bit selects a conversion of the ADIN2 input. When it is high, a conversion of this input is expected during the next conversion sequence.

ADIN3CV : This bit selects a conversion of the ADIN3 input. When it is high, a conversion of this input is expected during the next conversion sequence.

ADIN4CV : This bit selects a conversion of the ADIN4 input. When it is high, a conversion of this input is expected during the next conversion sequence.

A **shadow** register, which corresponds to ADCCTRL Register is used during a conversions sequence: the running sequence performs conversions depending on bits of the shadow register. If the micro-controller modifies the value of ADCCTRL data during a conversions sequence, the new data will be loaded in the shadow register at the beginning of the next sequence.

Access:

ADCCTRL : Write access at any time, even if MADC powered down.

ADCCTRL shadow : Updated with ADCCTRL contents at the beginning of a sequence of conversions (when receiving START_CONV signal);

: Read access at any time:

If a read signal occurs when ADCBUSY = 1 (sequence is running), selection bits, which correspond to current running sequence, are read;

If a read signal occurs when ADCBUSY = 0 (no runnin g sequence), last written selection bits, which correspond to last performed sequence, are read.

11.2 Monitoring ADC output register

For each register from Address 15 to 22 perform a ,
Read access : Only when ADCEOC bit is 0 and MADC module is powered on.
Write access : Start a conversion (bits contents not affected) like STARTADC in TSP interface.

11.2.1 ADC_STATUS

Name :ADC_STATUS					Description :						Address : 24 Page : 0					R
-	-	-	-	-	-	-	-	-	ADCBUSY	1	1	0	0	0	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

ADCBUSY : This bit is high during a conversion.

11.2.2 Battery voltage register: VBATREG (MADC RAM)

Name :VBATREG					Description :						Address : 15 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	1	1	1	1	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the voltage of the battery.

11.2.3 Charger battery voltage register: VCHGREG (MADC RAM)

Name :VCGHREG					Description :						Address : 16 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	0	0	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the voltage of the battery charger.

11.2.4 Charger battery current register: ICHGREG (MADC RAM)

Name :ICGHREG					Description :						Address : 17 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	0	1	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the current of the battery charger.

11.2.5 Backup battery voltage register: VBKPREG (MADC RAM)

Name :VBKPREG					Description :						Address : 18 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	0	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the voltage of the backup battery.

11.2.6 Battery type register: ADIN1REG (MADC RAM)

Name :ADIN1REG					Description :					Address : 19 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	0	1	1	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the ADIN1 pin.

11.2.7 Battery temperature register: ADIN2REG (MADC RAM)

Name :ADIN2REG					Description :					Address : 20 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	0	0	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the ADIN2 pin.

11.2.8 ADIN3REG (MADC RAM)

Name :ADIN3REG					Description :					Address : 21 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	0	1	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the ADIN3 pin.

11.2.9 ADIN4REG (MADC RAM)

Name :ADIN4REG					Description :					Address : 22 Page : 0					R
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	1	0	1
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Output of the 10 bits monitoring ADC for the ADIN4 pin.

12. CKG REGISTERS

12.1 Block power up / down selection

These bits are not memories cells, they generate only set or reset of internal latches. Writing “0” into any of these bit has no action.
If both xxxR and xxxS are writen to “1” at the same time it is interpreted as xxxR
(e.g set xxON to zero).

Name : TOGBR 1						Description : Toggle bits register1				Address : 4		Page : 0			W
MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR	0	0	1	0	0	0
W	W	W	W	W	W	W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

VULR : Writing “1” sets the bit VULON to zero
VULS : Writing “1” sets the bit VULON to one
VDLR : Writing “1” sets the bit VDLON to zero
VDLS : Writing “1” sets the bit VDLON to one
ADACR : Writing “1” sets the bit ADACON to zero
ADACS : Writing “1” sets the bit ADACON to one
AFCR : Writing “1” sets the bit AFCON to zero
AFCS : Writing “1” sets the bit AFCON to one
MADCR : Writing “1” sets the bit MADCON to zero
MADCS : Writing “1” sets the bit MADCON to one

Name : TOGBR 2					Description : Toggle bits register2					Address : 5		Page : 0			W
-	-	-	IAPCTR	IBUFPTR2	IBUFPTR1	ACTS	ACTR	KEEPS	KEEPR	0	0	1	0	1	0
-	-	-	W	W	W	W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

KEEPR : Writing “1” sets the bit KEEPON to zero
KEEPS : Writing “1” sets the bit KEEPON to one
ACTR : Writing “1” sets the bit ACTIVMCLK to z ero
ACTS : Writing “1” sets the bit ACTIVMCLK to one
IBUFPTR1 : Writing “1” initializes pointer of burst buffer 1
IBUFPTR2 : Writing “1” initializes pointer of burst buffer 2
IAPCTR : Writing “1” initializes pointer of APC ram

12.2 Power up / down status

Name : PWDNRG			Description : Register For Powering Down							Address : 9 Page : 1					R
-	-	-	ACTIVMCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON	0	1	0	0	1	1/0
R	R	R	R	R	R	R	R	R	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

VULON : When this bit is set to 0, the voice band uplink path is in power down mode. This bit is set by VULS and reset by VULR.

VDLON : When this bit is set to 0, the voice band downlink path is in power down mode. This bit is set by VDLS and reset by VDLR.

ADACON : When this bit is set to 0, the auxiliary DAC is in power down mode. This bit is set by ADACS and reset by ADACR

AFCON : When this bit is set to 0, the AFC is in power down mode. This bit is set by AFCS and reset by AFCR.

MADCON : When this bit is set to 0, the MADC is in power down mode. This bit is set by MADCS and reset by MADCR.

KEEPON : When this bit is set to 1, the ADC of MADC block is always ON even after a conversion. When this bit is set to 0, the ADC of MADC block sets itself automatically OFF after a conversion. This bit is set by KEEPS and reset by KEEPR.

ACTIVMCLK : When this bit is set to 0, the MADC, IBIC are in low power mode, using CK32K clock. This bit is set by ACTS and reset by ACTR.

13. AFC REGISTERS

Name : AUXAFC1 Description : Automatic Frequency Control Reg1										Address : 7 Page 0					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	0	1	1	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9-0] : LSB Input of the 13 bit AFC DAC in two's complement.

Name : AUXAFC2 Description : Automatic Frequency Control Reg2										Address : 8 Page 0					R/W
-	-	-	-	-	-	-	BIT12	BIT11	BIT10	0	1	0	0	0	1 / 0
R	R	R	R	R	R	R	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[12-10] : MSB Input of the 13 bit AFC DAC in two's complement.
The AFC value is loaded after successive write of AFC-MSB and AFC-LSB.

Name : AFCCTLADD Description : Work frequency of AFC										Address : 21 Page 1					R/W
-	-	-	-	-	-	-	AFCBYP	AFCCK1	AFCCK0	1	0	1	0	1	1 / 0
R	R	R	R	R	R	R	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

AFCCK[1:0] : '00' → CKAFC = CKIN
'01' → CKAFC = CKIN/2
'10' → CKAFC = CKIN/4
'11' → CKAFC = CKIN/8
(CKIN = CK13M/3 = 4.3 MHz)

AFCBYP : Disable write in AFCOUT by delta sigma modulator
Enable write by USP or BSP access in AFCOUT register

Name : AFCOUT Description : AFC Digital output register										Address : 22 Page 1					R/W
-	-	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0	1	0	1	1	0	1 / 0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

DOUT[7:0] : Output of the AFC delta sigma modulator
(for write access , see AFCBYP bit description)
AFCON must be set to enable the write

14. APC REGISTERS

Name : APCDEL1 Description : APC Ramp Delay Reg.										Address : 2 Page : 0					R/W
DELD5	DELD4	DELD2	DELD1	DELD0	DELU4	DELU3	DELU2	DELU1	DELU0	0	0	0	1	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

DELU[4:0] : LSB for the value of the delay of ramp-up start versus the rising edge of BENA.
DELD[4:0] : LSB for the value of the delay of ramp-down start versus the falling edge of BENA.

Name : APCDEL2 Description : APC Ramp Delay Reg.										Address : 26 Page : 1					R/W
DELD9	DELD8	DELD7	DELD6	DELD5	DELU9	DELU8	DELU7	DELU6	DELU5	1	1	0	1	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

DELU[9:5] : MSB of the value of the delay of ramp-up start versus the rising edge of BENA.
DELD[9:5] : MSB of the value of the delay of ramp-down start versus the falling edge of BENA.

Name :AUXAPC Description : Automatic Power Control Register										Address : 9 Page : 0					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	1	0	0	1	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : 10 bit APC power level.

Name : APCRAM Description : Automatic Power Control RAM										Address : 10 Page : 0 (16 words)					W
DW-0 (5BIT)					UP-0 (5 BIT)					0	1	0	1	0	0
DW-1 (5 BIT)					UP-1 (5BIT)					0	1	0	1	0	0
//////////					//////					//////	//////	//////	//////	//////	//////
//////////					//////					//////	//////	//////	//////	//////	//////
DW-14 (5 BIT)					UP-14 (5BIT)					0	1	0	1	0	0
DW-15 (5 BIT)					UP-15 (5BIT)					0	1	0	1	0	0
W	W	W	W	W	W	W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

Content of the APC ram is the coefficients of the rampup and rampdown shaping filters.

Name :APCOFF Description : Offset DAC Input Register										Address : 11 Page : 0					R/W
-	-	-	RSV	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	1	0	1	1	1 / 0
R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[5:0] : Input of the 6 bit Offset DAC.
RSV : Reserved bits.

Name : APCOUT Description : APC output register										Address : 12 Page : 1					R/W
APC9	APC8	APC7	APC6	APC5	APC4	APC3	APC2	APC1	APC0	0	1	1	0	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

APC[9:0] : Value of data applied to APC DAC 10.

15. AUXDAC REGISTERS

Name :AUXDAC Description : Auxiliary DAC Control Register										Address : 12 Page : 0					R/W
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	0	1	1	0	0	1 / 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

BIT[9:0] : Input of the 10 bit ADAC.

16. SIM CARD REGISTERS

Name :VRPCSIM Description : SIM CARD Control Register										Address : 23 Page : 1					R/W
-	-	-	-	-	-	SIMLEN	SIMRSU	RSIMEN	SIMSEL	1	0	1	1	1	1 / 0
R	R	R	R	R	R	R/W	R	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

SIMSEL : Select VRSIM output voltage
'1' => 2.9 V '0' => 1.8V
RSIMEN : Enable the RSIM regulator
SIMRSU : VRSIM regulation status
'1' => regulation is ON, the SIM interface is correctly supplied
'0' => the regulator is not yet in regulation mode
SIMLEN : Enable the SIM interface level shifter (SIMCK, SIMIO, SIMRST are enable)

17. AUXILIARY DRIVER REGISTERS

Name :ACDLED Description : Auxiliary Driver Control Register										Address : 24 Page : 1					R/W
-	-	-	-	-	-	-	-	LEDB	LEDA	1	1	0	0	0	1 / 0
R	R	R	R	R	R	R	R	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

LEDA : When '1' , enable the LEDA driver
LEDB : When '1' , enable the LEDB driver

18. INTERNAL BUS AND INTERRUPT CONTROL REGISTERS

18.1 Interrupt 2 mask and status

Name : ITMASKREG				Description : Interrupt mask Register						Address : 26 Page : 0					R/W
-	-	-	-	ADCEND	-	CHRGER	PUSHOF	REMOT	-	1	1	0	1	0	1 / 0
R	R	R	R	R/W	R	R/W	R/W	R/W	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

REMOT_IT_MSK : If **1** the 'Remote Power' from ON to OFF interrupt is not generated
PUSHOFF_IT_MSK : If **1** the 'Push Button' from ON to OFF interrupt is not generated
CHARGER_IT_MSK : If **1** the Charger Plug IN or OUT interrupt is not generated
ADCEND_IT_MSK : If **1** the ADC End of Conversion interrupt is not generated

Name : IT_STS_REG				Description : Interrupt Status Register						Address : 27 Pages : 0 & 1					R/W
-	-	-	-	ADCEND	-	CHRGER	PUSHOF	REMOT	-	1	1	0	1	1	1 / 0
R	R	R	R	R/W	R	R/W	R/W	R/W	R	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

REMOT_IT_STS : 'Remote Power' from ON to OFF interrupt bit
PUSHOFF_IT_STS : 'Push Button' from ON to OFF interrupt bit
CHARGER_IT_STS : Charger Plug IN or OUT interrupt bit
ADCEND_IT_STS : ADC End of Conversion interrupt bit

18.2 Page selection

Name : PAGEREG				Description : Page Select Register						Address : 1 Pages : 0 & 1					R/W
-	-	-	-	-	-	BSPP1	BSPP0	UCP1	UCP0	0	0	0	0	1	0
						W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

UCP0 : Set Address Page 0 for USP access
UCP1 : Set Address Page 1 for USP access
BSPP0 : Set Address Page 0 for BSP access
BSPP1 : Set Address Page 1 for BSP access

USP access to this register don't affect current address page selected by the BSP and BSP access to fect current address page selected by the USP.
That means that USP access has no effect if trying to write BSPP1 or BSPP0 and BSP access has no effect if trying to write UCP1 or UCP0.

19. TEST ACCESS PORT REGISTERS

19.1 TAP control

Name : TAPCTL	Description : Tap Instruction Register									Address : 19	Pages : 1				R/W
-	-	-	-	-	-	-	-	-	TAPEN	1	0	0	1	1	1 / 0
R	R	R	R	R	R	R	R	R	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

TAPEN : Enable write in TAPREG

19.2 TAP instruction register

Name : TAPREG	Description : Tap Instruction Register									Address : 20	Pages : 1				R/W
VER3	VER2	VER1	VER0	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	1	0	1	0	0	1 / 0
R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	1	<--- VALUE AT RESET					

VER[3:0] : Version Number VER[3:0] (from IDCODE)
BIT[5:0] : JTAG Instruction Register data , TAPINST[5:0]