TRF6151 RITA Quadruple band GSM Single chip Transceiver

Specification

RIT000

Vers 3.0

File: RITA Specification.pdf

Department: WTBU Chipset 2G - 2.5G

	Originator	Approval	Quality
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Signature			

HISTORY

Version	Date	Author	Notes
Vers 1.0	12/20/01	Estelle PROUX Francois BELIN Angel EZQUERRA Jerome DEMAY	First version
Vers 2.0	03/28/02	Estelle PROUX Francois BELIN Angel EZQUERRA Jerome DEMAY	Second version
Vers 2.1	04/04/02	Jerome DEMAY	Third version
Vers 2.2	05/02/02	Francois BELIN Jerome DEMAY	Fourth version
Vers 2.3	05/30/02	Jerome DEMAY	Fifth version
Vers 3.0	12/03/02	Estelle PROUX Jerome DEMAY	Sixth version

NOTES :

1.0 Creation
2.0 Update following Designers'inputs – PA controller specification added
2.1 VCC pin swap
2.2 P.A.U.C. specification added
2.3 Current consumption table updated
3.0 Global Input 1dB blocking compression point table added
Update of serial interface
P.A.U.C. specification removed

TABLE OF CONTENT

INTRODUCTION

The TRF6151 is a quadruple band transceiver IC suitable for GSM 850, GSM 900, DCS 1800 and PCS 1900 GPRS class 12 applications. The chip integrates the receiver based on direct conversion architecture, the transmitter based on the modulation loop architecture, the frequency synthesis including a 26MHz VCXO, a MAIN N-integer synthesizer, 2 MAIN VCOs, a programmable MAIN loop filter, 2 TX VCOs, a TX loop filter, the voltage regulators to supply on chip and off chip RF functions and a power amplifier controller.
Few external components are required for a "quad band" application as a power amplifier and a front-end module.
It is housed in a 48 pins 7x7mm - 0.5mm pitch QFN package.
The TRF6151 transceiver is part of TI GSM chipset. It is compatible with Iota (TWL3014) and Syren (TWL3016) ABB chips and with Calypso, Calypso20G2, Calypso-plus and Perseus2 DBB chips.

The chip combines the following functions:

1. Transmit section:
   - an offset PLL with post IQ modulator and post offset mixer filters fully integrated on chip
   - two TX VCOs fully integrated on chip
   - a TX loop filter fully integrated on chip
   - a divider by 4 for the LO generation in GSM900 and GSM850
   - a divider by 2 for the LO generation in DCS1800 and PCS1900
   - a programmable M divider for the IF generation
   - a power amplifier controller including all the functions required to design a power sensing control loop except the sensing diodes

2. Receive section:
   - a GSM900/GSM850 LNA (LNAGSM) with switchable gain
   - a DCS1800 LNA (LNADCS) with switchable gain
   - a PCS1900 LNA (LNAPCS) with switchable gain
   - three quadrature demodulators for GSM900/GSM850 (MIXGSM), DCS1800 (MIXDCS) and PCS1900 (MIXPCS) bands with switchable gain
   - two base-band amplifiers with digitally programmable gain
   - two fully integrated base-band channel filters.
   - two DC offset compensation systems
   - a divider by 4 for the LO generation in GSM900 and GSM850 in order to minimize the DC offset generated by self mixing and the LO re-radiation
   - a divider by 2 for the LO generation in DCS1800 and PCS1900 in order to minimize the DC offset generated by self-mixing and the LO re-radiation.
   - an interferer detection system

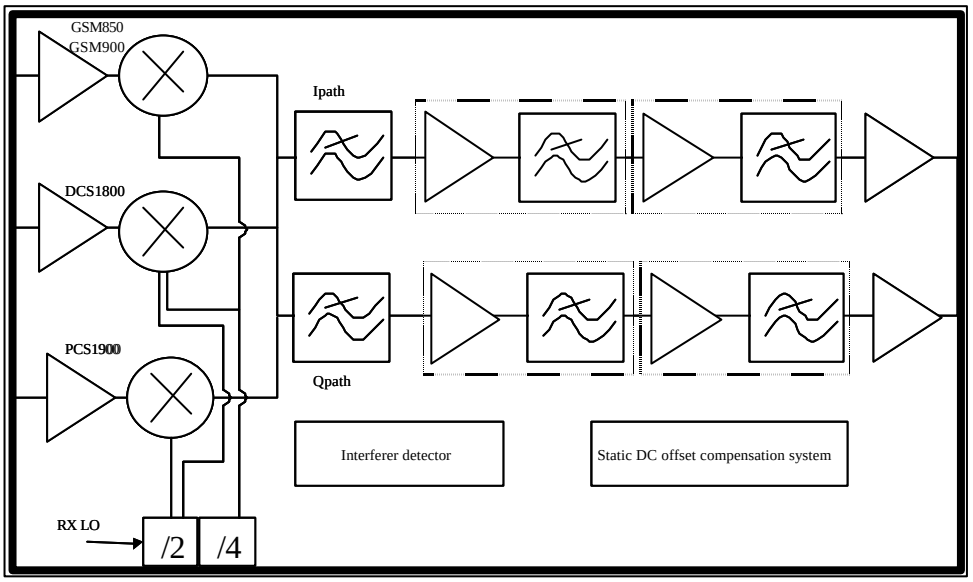


Figure 1 - Receiver block diagram

3. Common to both sections:
   - a 26MHz VCXO with external varactor and crystal
   - a 26 MHz buffer to drive the DBB
   - two MAIN VCOs fully integrated on chip
   - a MAIN N-integer synthesizer
   - a programmable MAIN loop filter fully integrated on chip
   - 3 voltage regulators to supply internal functions and external RF components
   - a digital serial interface

REFERENCES

[1] 3GPP TS05.05 version 8.10
"Digital cellular telecommunications system (phase 2+); Radio transmission and reception "

[2] 3GPP TS51.010-1 version 4.4.0
"Digital cellular telecommunications system (phase 2+); MS conformance specification "

[3] TWL3014 v1.2 specification (Iota) – Internal document – Texas Instruments

[4] Time serial port specification – HYP004 v1.0 – Internal document – Texas instruments

CHIPSET BLOCK DIAGRAM

TI chipset = HERC-Rxx + TWL3014 / TWL3016 + TRF6151

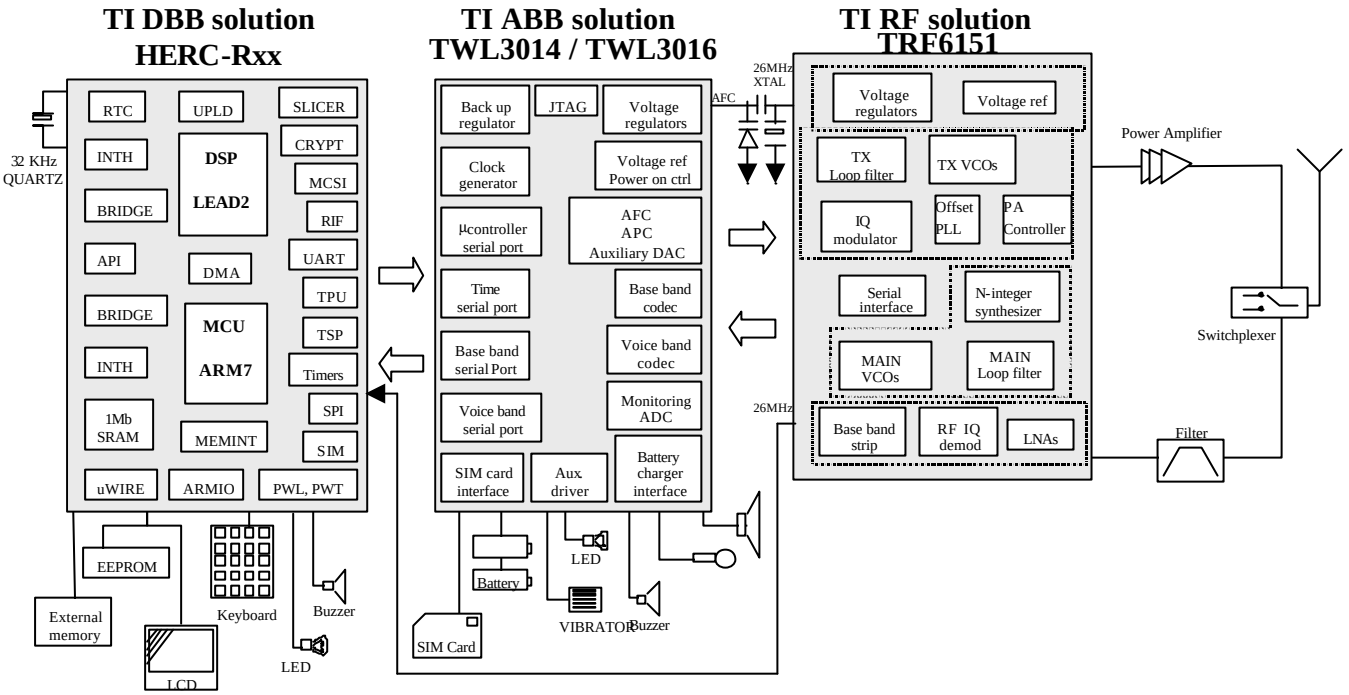


Figure 2 - Chipset block diagram

APPLICATION BOARD FUNCTIONAL BLOCK DIAGRAM

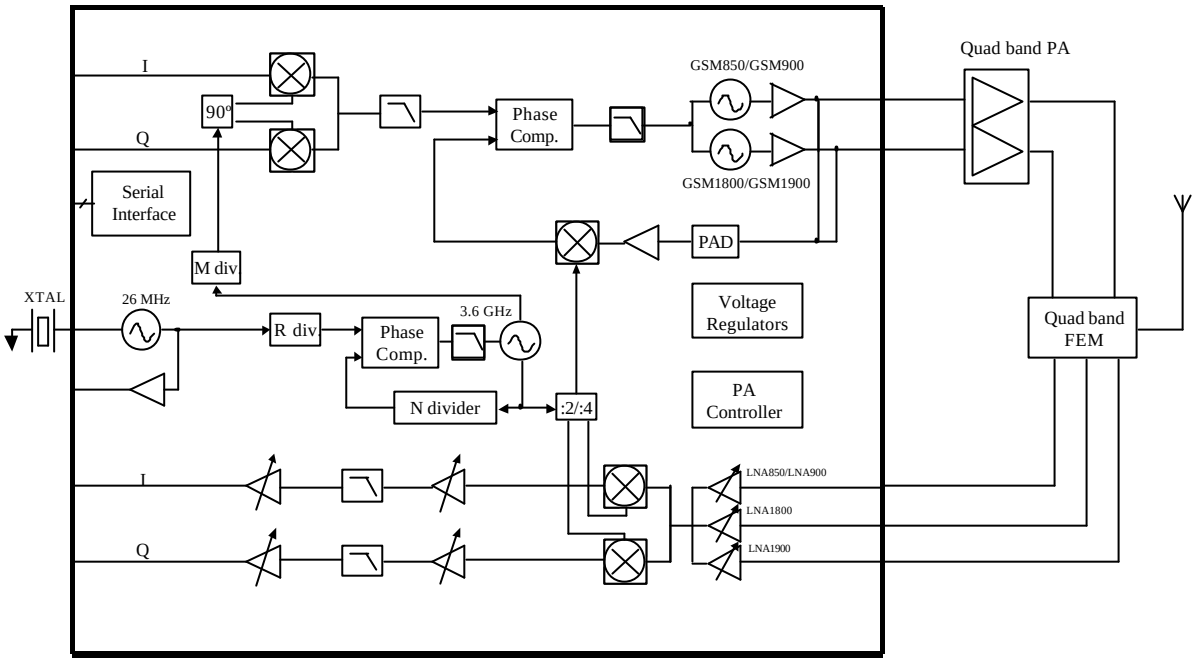


Figure 3 - TRF6151 block diagram

TERMINAL DIAGRAM

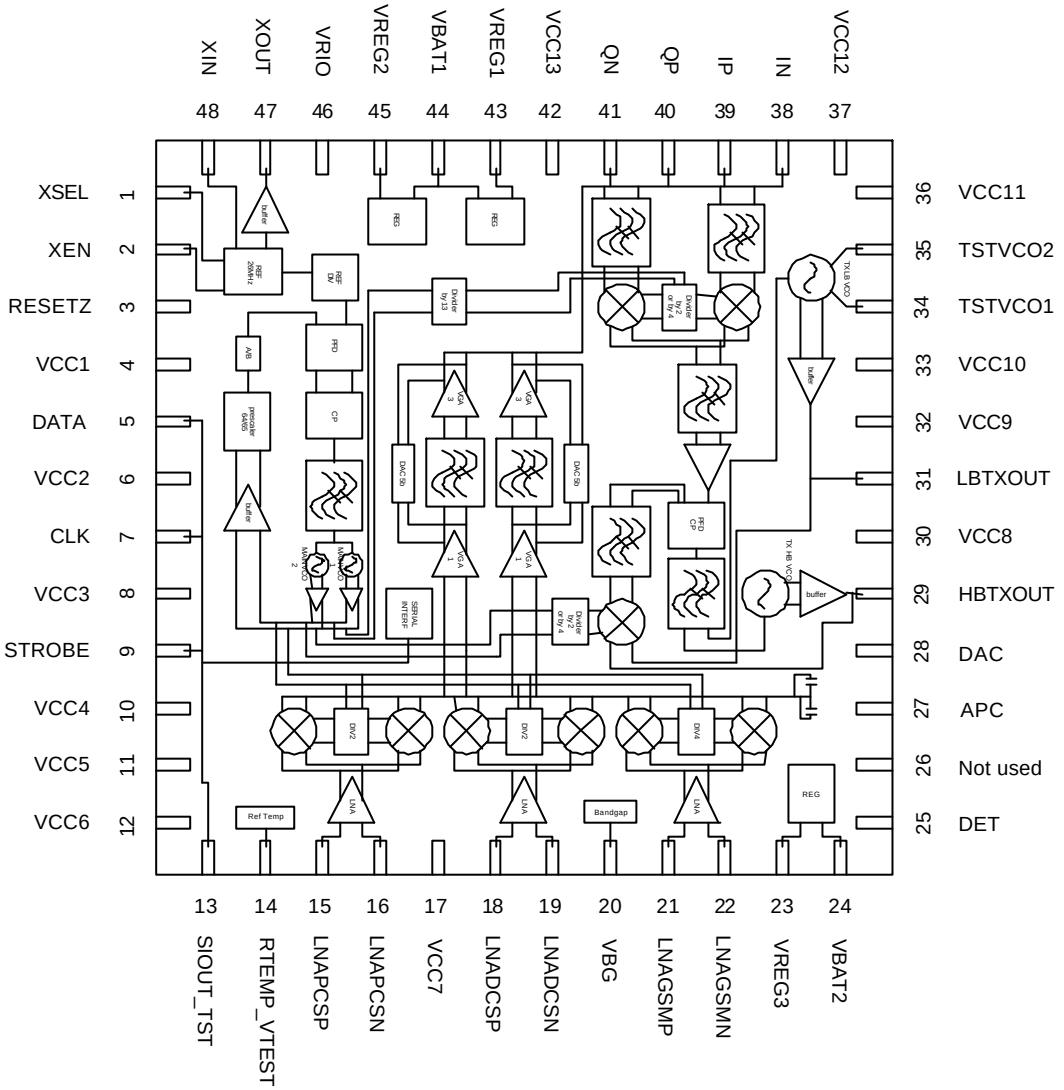


Figure 4 - TRF6151 terminal diagram (top view)

PINS DESCRIPTION

PIN NAME	PIN#	I/O	DESCRIPTION
XSEL	1	I	Xtal select external or internal
XEN	2	I	Xtal enable (VCXO and buffer supply)
RESETZ	3	I	Serial interface reset input
VCC1	4	VCC	PLL supply voltage
DATA	5	I	Serial interface data input
VCC2	6	VCC	PLL supply voltage
CLK	7	I	Serial interface clock input
VCC3	8	VCC	PLL supply voltage
STROBE	9	I	Serial interface strobe input
VCC4	10	VCC	MAIN VCO2 supply voltage (2.0Volts internally generated)
VCC5	11	VCC	VCO DIVIDER supply voltage
VCC6	12	VCC	MAIN VCO1 supply voltage (2.0Volts internally generated)
SIOUT_TST	13	O	Serial interface output multiplexed with PLL test
RTEMP_VTEST	14	O	Temperature sensor output and VCO test
LNAPCSP	15	I	RX PCS LNA input (+)
LNAPCSN	16	I	RX PCS LNA input (-)
VCC7	17	VCC	RX LNA supply voltage
LNADCSP	18	I	RX DCS LNA input
LNADCSN	19	I	RX DCS LNA input
VBG	20	O	Bandgap voltage output
LNAGSMP	21	I	RX GSM LNA input (+)
LNAGSMN	22	I	RX GSM LNA input (-)
VREG3	23	O	Regulator 3 output dedicated to VCC8, VCC10
VBAT2	24	I	Regulator 3 battery voltage supply
DET	25	I	PA controller DETECT input
Not used	26	-	Not used
APC	27	O	PA controller output
DAC	28	I	PA controller APC input
HBTXOUT	29	O	TX DCS/PCS output
VCC8	30	VCC	TX VCO buffer supply voltage (2.7V)
LBTXOUT	31	O	TX GSM900 / GSM850 output
VCC9	32	VCC	TX HB VCO core supply voltage (2.4V internally generated)
VCC10	33	VCC	TX VCO and RX mixer supply voltage
TSTVCO1	34	I/O	LB TX VCO test (tank if Pnoise spec not reached)
TSTVCO2	35	I/O	LB TX VCO test (tank if Pnoise spec not reached)
VCC11	36	VCC	TX LB VCO core supply voltage (2.4V internally generated)
VCC12	37	VCC	IQ modulator supply voltage and RX VGA supply voltage (2.7V)
IN	38	I/O	In phase baseband I/O (-)
IP	39	I/O	In phase baseband I/O (+)
QP	40	I/O	Quadrature phase baseband I/O (+)
QN	41	I/O	Quadrature phase baseband I/O (-)
VCC13	42	VCC	TX charge pump supply voltage (2.7V)
VREG1	43	O	Regulator 1 output dedicated to VCC7, VCC12, VCC13
VBAT1	44	I	Regulator 1 and regulator 2 battery voltage supply

VREG2	45	O	Regulator 2 output dedicated to VCC1, VCC2, VCC3, VCC5
VRIO	46	VCC	Serial interface supply voltage
XOUT	47	O	Xtal buffer output
XIN	48	I	Xtal input

PACKAGE CHARACTERISTICS

48 pins QFN 7x7mm – 0.5mm pitch

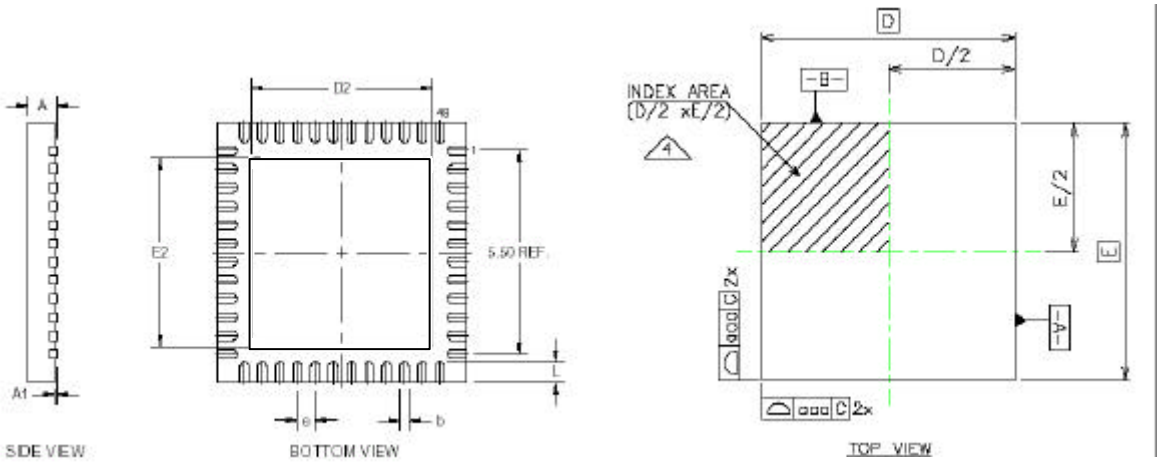


Figure 5 - Component Dimensions

BODY SIZE = 7.0 x 7.0mm, THICKNESS = 0.9mm

SYMBOL	Package Dimensions with Tolerance		
	MIN.	NOM.	MAX.
A	-	0.85	0.90
A1	0	0.02	0.05
D	6.85	7.00	7.15
D2	5.00	5.15	5.25
E	6.85	7.00	7.15
E2	5.00	5.15	5.25
L	0.30	0.40	0.50
b	0.18	0.23	0.30
e	-	0.50 BSC	-

All dimensions in Millimeters

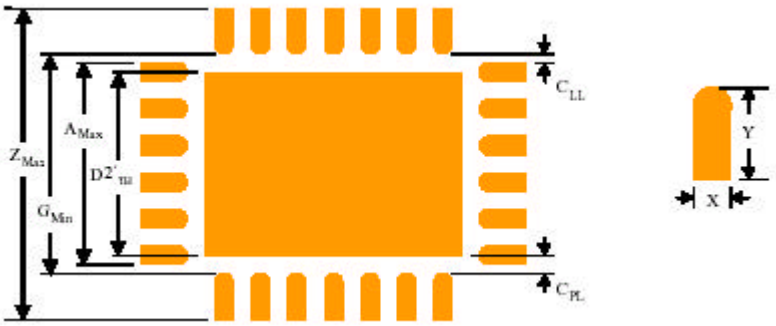


Figure 6 - PCB Land Pattern Dimensions

SYMBOL	Board Land Pattern Dimensions					
	Zmax	Amax	Gmin	Xmax	Yref	$D2'_{TH}$
	7.36	5.78	5.98	0.28	0.69	5.68

All dimensions in Millimeters

Note: Xmax dimension reduced to avoid solder bridging

TBD

Figure 7 - Thermal Pad Stencil Design

More information on Package Characteristics is available on: http://www1.itg.ti.com/msp_packaging/docs/qfn/qfn_home.htm, "Available QFN Package Information"

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

Chip supply voltage range: VBAT .....-0.3 V to 5.5 V
Input voltage to any other pin: .....tbd V
Power dissipation, Ta = 25 °C, 48 Pin QFN 7x7mm - 0.5mm pitch.....tbd mW
Storage temperature range .....-65 to +150 °C
ESD integrity[1] .....tbd HBM

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
VRIO Supply voltage	2.7	2.8	2.9	V
VIH High level input voltage	0.8*VRIO			V
VIL Low level input voltage			0.22 x VRIO	V
VOH High level output voltage	0.7*VRIO		VRIO+0.5	
VOL Low level output voltage	-0.5		0.3*VRIO	
VCC Supply voltage	2.7	2.8	2.9	V
VBAT Supply voltage	3.0[2]	3.6	5.5	V
Ta Operating Temperature range	-25		+85	°C

[1] Sensitive RF pins (LNA inputs, TXVCO outputs) are not protected against voltage stress higher than 300 V HBM (tbc).
[2] 3.0 V corresponds to VBATMIN ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at Rita regulators inputs

ELECTRICAL CHARACTERISTICS

Typical: Vcc = 2.8 V, Ta = +25°C
Max. and Min.: Ta= -25°C to +85°C

CURRENT CONSUMPTION[3]

Power mode	Test conditions	Band	Typical operating current
OFF mode			
ALL OFF	All functional blocks powered OFF	-	5 uA
ALL OFF except BG	Band gap ON and all others functional blocks powered OFF	-	80 uA
ALL OFF except BG and Regulators	Band gap and Regulators ON and all others functional blocks powered OFF	-	0.6 mA
Receive mode			
RX synthesizer ON	Main PLL is locking	GSM850 / GSM900	8.0 mA
		DCS1800	8.0 mA
		PCS1900	8.0 mA
RX synthesizer ON + DC offset calibration running	Main PLL and RX calibration process are ON	GSM850 / GSM900	44.0 mA
		DCS1800	46.0 mA
		PCS1900	46.0 mA
RX ON in High gain	Main PLL, LO generation, LNA, IQ demodulator and Baseband strip are ON	GSM850 / GSM900	53.0 mA
		DCS1800	55.0 mA
		PCS1900	55.0 mA
Transmit mode[4]			
Main TX synthesizer ON + PA controller ON	Main PLL is locking and PA controller powered ON	Low Band	11.0 mA
		High Band	11.0 mA
TX ON	Main PLL and Offset PLL, LO/IF generation, IQ modulator and PA controller are ON	Low Band	116.0 mA
		High Band	106.0 mA

[3] VCXO (supplied by an external voltage source) typical current consumption is 1.1 mA
[4] with P.A.U.C. the typical current consumption is 2.0 mA higher

Module	VCC line	Band	Typical operating current

RX ON in High gain

LNA	VCC7	All Bands	8.6 mA
IQ demodulator	VCC8	All Bands	8.4 mA
LO generation	VCC5	GSM850 / GSM900	18.4 mA
		DCS1800 / PCS1900	20.2 mA
Baseband strip	VCC12	All Bands	8.0 mA
Main Prescaler + Main CP + Main PFD	VCC2	All Bands	5.3 mA
Main loop filter	VCC3	All Bands	1.7 mA
Voltage regulator R1	VREG1	All Bands	15.9 mA
Voltage regulator R2	VREG2	GSM850 / GSM900	25.4 mA
		DCS1800 / PCS1900	27.2 mA
Voltage regulator R3	VREG3	All Bands	8.4 mA
VBAT1	-	GSM850 / GSM900	43.5 mA
		DCS1800 / PCS1900	45.4 mA
VBAT2	-	All Bands	8.9 mA

Module	VCC line	Band	Typical operating current
TX ON			
TX Charge pump	VCC13	All Bands	0.8 mA
Offset mixer and following low pass filter	VCC7	All Bands	11.7 mA
IQ modulator + post IQ modulator low pass filter	VCC12	All Bands	8.8 mA
TX VCO + Offset mixer buffer	VCC10	Low Band	18.2 mA
		High Band	18.1 mA
TX VCO buffer	VCC8	Low Band	24.4 mA
		High Band	15.7 mA
PA controller	VCC7	All Bands	2.8 mA
LO generation (L divider, M divider) + Main VCO regulator input	VCC5	Low Band	26.6 mA
		High Band	26.8 mA
Main Prescaler + Main charge pump + Main phase frequency detector	VCC2	All Bands	5.3 mA
Main loop filter	VCC3	All Bands	1.7 mA
Voltage regulator R1	VREG1	All Bands	24.1 mA
Voltage regulator R2	VREG2	Low Band	33.6 mA
		High Band	33.8 mA
Voltage regulator R3	VREG3	Low Band	42.6 mA
		High Band	33.8 mA
VBAT1	-	Low Band	70.6 mA
		High Band	70.4 mA
VBAT2	-	Low Band	44.9 mA
		High Band	35.6 mA

VOLTAGE REGULATION

C_{out}=1.0uF, $C_{bandgap}$=100nF unless otherwise specified.
Table specifies regulator and bandgap together unless otherwise specified.
If an external regulation is desired, the internal voltage regulators can be bypassed (regulators shut down).

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Band gap						
Turn-on time	speed up mode active				25	ms
Consumption current				80		uA
Regulator R1						
Input voltage		Vin	3.0[5]	3.6	5.5	V
Output voltage	@ Ioutmax	Vout	2.7	2.8	2.9	V
Max. output current		Ioutmax	60			mA
Ground pin current	@ Ioutmax @ Iout = 0 mA				6.0 0.3	mA
DC line regulation	From Vinmin to Vinmax @ Ioutmax				50	mV
AC line regulation Overshoot Undershoot	Vin step from Vout + 0.1 to Vout + 0.5 in 30 us Vin step from Vout + 0.5 to Vout + 0.1 in 30 us				 20 20	mV
DC load regulation	Iout = 0 mA to Ioutmax				50	mV
AC load regulation Overshoot Undershoot	Iout step from Ioutmax to Ioutmax/2 in 5 us Iout step from Ioutmax/2 to Ioutmax in 5 us				 30 30	mV
Output voltage noise	f =10 Hz to 100 kHz Iout = Ioutmax Vin = Vout + 0.2 V			50		uVrms
ESR of decoupling capacitor			0.01		1	Ohm
Response time	Iout step from 0 to Ioutmax Iout step from Ioutmax to 0 @ Vout = final +/-3 %			10 10		us
Turn-on time	Vout step from 0 to Voutmax +/-3% @ Ioutmax			100[6]		us
Ripple rejection	AC amplitude = 50 mVp f = 100 Hz @ Ioutmax f = 500 kHz @ Ioutmax Vin = 3.1 V			55 35		dB
Shutdown supply current	Vout = 0 V				1	uA

[5] 3.0 V corresponds to VBATMIN ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at Rita regulators inputs
[6] Band gap turn-on time not included

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Regulator R2						
Input voltage		Vin	3.0[7]	3.6	5.5	V
Output voltage	@ Ioutmax	Vout	2.7	2.8	2.9	V
Max. output current		Ioutmax	60			mA
Ground pin current	@ Ioutmax @ Iout = 0 mA				6.0 0.3	mA
DC line regulation	From Vinmin to Vinmax @ Ioutmax				50	mV
AC line regulation Overshoot Undershoot	Vin step from Vout + 0.1 to Vout + 0.5 in 30 us Vin step from Vout + 0.5 to Vout + 0.1 in 30 us				 20 20	mV
DC load regulation	Iout = 0 mA to Ioutmax				50	mV
AC load regulation Overshoot Undershoot	Iout step from Ioutmax to Ioutmax/2 in 5 us Iout step from Ioutmax/2 to Ioutmax in 5 us				 30 30	mV
Output voltage noise	f =10 Hz to 100 kHz Iout = Ioutmax Vin = Vout + 0.2 V			50		uVrms
ESR of decoupling capacitor			0.01		1	Ohm
Response time	Iout step from 0 to Ioutmax Iout step from Ioutmax to 0 @ Vout = final +/-3 %			10 10		us
Turn-on time	Vout step from 0 to Voutmax +/-3% @ Ioutmax			100[8]		us
Ripple rejection	AC amplitude = 50 mVp f = 100 Hz @ Ioutmax f = 500 kHz @ Ioutmax Vin = 3.1 V			55 35		dB
Shutdown supply current	Vout = 0 V				1	uA

[7] 3.0 V corresponds to VBATMIN ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at Rita regulators inputs

[8] Band gap turn-on time not included

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Regulator R3						
Input voltage		Vin	3.0[9]	3.6	5.5	V
Output voltage	@ Ioutmax	Vout	2.7	2.8	2.9	V
Max. output current		Ioutmax	60			mA
Ground pin current	@ Ioutmax @ Iout = 0 mA				6.0 0.3	mA
DC line regulation	From Vinmin to Vinmax @ Ioutmax				50	mV
AC line regulation Overshoot Undershoot	Vin step from Vout + 0.1 to Vout + 0.5 in 30 us Vin step from Vout + 0.5 to Vout + 0.1 in 30 us				 20 20	mV
DC load regulation	Iout = 0 mA to Ioutmax				50	mV
AC load regulation Overshoot Undershoot	Iout step from Ioutmax to Ioutmax/2 in 5 us Iout step from Ioutmax/2 to Ioutmax in 5 us				 30 30	mV
Output voltage noise	f =10 Hz to 100 kHz Iout = Ioutmax Vin = Vout + 0.2 V			50		uVrms
ESR of decoupling capacitor			0.01		1	Ohm
Response time	Iout step from 0 to Ioutmax Iout step from Ioutmax to 0 @ Vout = final +/-3 %			10 10		us
Turn-on time	Vout step from 0 to Voutmax +/-3% @ Ioutmax			100[10]		us
Ripple rejection	AC amplitude = 50 mVp f = 100 Hz @ Ioutmax f = 500 kHz @ Ioutmax Vin = 3.1 V			55 35		dB
Shutdown supply current	Vout = 0 V				1	uA

[9] 3.0 V corresponds to VBATMIN ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at Rita regulators inputs

[10] Band gap turn-on time not included

Regulators power domains

Functional blocks	Supply voltage	Regulated Supply	VCC line
Receiver			
LNAGSM, LNADCS, LNAPCS	VBAT1	Vreg1	VCC7
Analog part of VGA	VBAT1	Vreg1	VCC12
IQ demodulators (MIXGSM, MIXDCS and MIXPCS)	VBAT2	Vreg3	VCC8
Interferer detection system	VBAT2	Vreg3	VCC10
Transmitter			
Charge pump	VBAT1	Vreg1	VCC13
Phase frequency detector	VBAT1	Vreg1	-[11]
Offset mixer, post offset mixer low pass filter	VBAT1	Vreg1	VCC7
Offset mixer buffer	VBAT2	Vreg3	VCC10
IQ modulator, post IQ modulator low pass filter	VBAT1	Vreg1	VCC12
TX LB VCO	VCC10	2.4V internal regulator	VCC11[12]
TX HB VCO	VCC10	2.4V internal regulator	VCC9[12]
TX VCO output buffers	VBAT2	Vreg3	VCC8
PA controller	VBAT1	Vreg1	VCC7
Main synthesizer			
Prescaler, Charge pump, Phase frequency detector	VBAT1	Vreg2	VCC2
Loop filter (operational amplifier)	VBAT1	Vreg2	VCC3
Counters A, B	VBAT1	Vreg2	VCC1
LO generation for the RX/TX (L divider, M divider)	VBAT1	Vreg2	VCC5
MAIN VCO2	VCC5	2.0V internal regulator	VCC4[13]
MAIN VCO1	VCC5	2.0V internal regulator	VCC6[13]
VCO calibration machine	VBAT2	Vreg3	VCC10
Reference voltage source			
Band gap	VBAT2	-	-
Digital control			
PA controller timer, Digital clock generator, serial interface and associated buffer, VGA digital circuitry	VRIO supply from ABB chip	-	VRIO
Internal 26MHz VCXO			
VCXO core, Main PLL Reference divider	TCXOEN buffer (2.7V) from DBB chip	-	XEN
Internal VCXO selection	TCXOEN buffer (2.7V) from DBB chip	-	XSEL
RF front End module (external component)			
Front End Module	VBAT2	Vreg3	-

[11] Connection is done on chip (no decoupling using a VCC line)
[12] Decoupling line for 2.4V internal regulator output
[13] Decoupling line for 2.0V internal regulator output

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

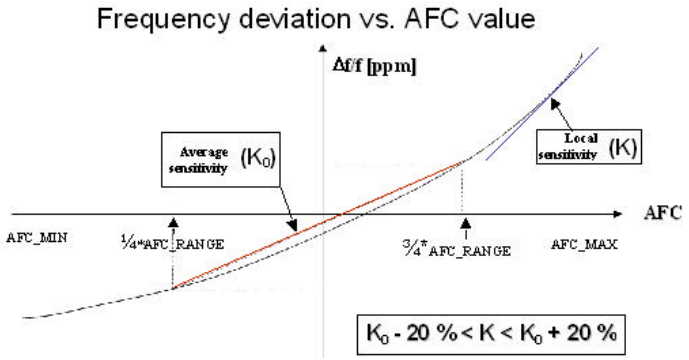
TEMPERATURE SENSOR[14]

Sensor voltage	@ Ta min. = -25°C @ Ta max. = +85°C		0.9 1.35		1.05 1.5	V
Sensor slope	Over -25 ~ +85°C		3.5		4.5	V/°C

SYNTHESIZER

Crystal and External Varactor network [15]

XEN supply pin	@ I = 2.0mA		2.5		2.9	V
Crystal						
Nominal frequency				26.0		MHz
Frequency tolerance	at 25°C ±3°C				±10.0	ppm
Temperature characteristics	in reference to +25°C over –20 ~ +75°C				±10.0	ppm
Aging 1st year after 5 years					±1.0 ±2.5	ppm ppm
Dips vs. temperature	–20 ~ +75°C				0.3	ppm/°C
Frequency versus temperature slope at 25°C	at 25° C ± 7°C		-0.5		0	ppm/°C
Equivalent Series Resistance			0		40	Ω
Standard load capacitance				9.3	12.0	pF
Shunt capacitance				1.5	1.7	pF
Motional capacitance			5.4	6.3	7.2	fF
Drive level					150	µW
Varactor network						
Voltage tuning		Vt	0		2.0	V
Tuning range			±26.0	±33.0	±41.0	ppm
Sensitivity accuracy[16]	Over temp and over the tuning range				20 %	Hz/step^2
Frequency step					0.01	ppm/step



[14] This temperature sensor is accessible at any time (not multiplexed with another signal)
[15] See Annex 6 (page 67) for connection schematic
[16] The sensitivity accuracy is how much the "local sensitivity" can differ from the average sensitivity. In other words, it is the derivate of the sensitivity. See the plot above.

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Reference clock input[17]

Input frequency				26		MHz
Input sensitivity			0.5	1.0	2.0	Vpp
Reference phase noise	@ 1 kHz offset				-129	dBc/Hz
Duty cycle					40/60 to 60/40	
Input resistance			10			kΩ
Input capacitance					5	pF

VCXO buffer output (XOUT pin)[18]

Output frequency				26		MHz
Output level			0.5	1.0	2.0	Vpp

[17] If use of an external VCTCXO (See Annex 6 (page 67) for connection schematic)

[18] Z_{LOAD} = 25pF in parallel with 10kΩ @ 26MHz

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Main synthesizer in RX mode for GSM 850 and E-GSM 900						
Specification at the mixers LO port						
Prescaler input frequency range			3476 to 3840			MHz
PFD operating frequency				400		kHz
N divider ratio			8692 to 9598			
L divider by 4 output frequency range			869 to 960			MHz
Close in phase noise	@ 1 kHz offset fcomp = 400 kHz @ 960 MHz				-81	dBc/Hz
Phase noise	@ 600 kHz offset @ 1.6 MHz offset @ 3.0 MHz offset @ 10 MHz offset @ 20 MHz offset				-120 -135 -140 -142 -145	dBc/Hz
Reference feedthrough	@ 400 kHz offset @ 800 kHz offset @ 1.6 MHz offset				-53 -68 -79	dBc
Lock time	1) GSM850: From 869MHz to 894MHz 2) GSM900: From 925MHz to 960MHz 3) PCS1900 ➔ GSM850: From 1990MHz to 869MHz 4) DCS1800 ➔ GSM900: From 1880MHz to 925MHz @ 20 Hz averaged frequency error over one burst			tbd	170	us

Power up/down time						
Power up time	Output power within 10 % of steady state values				5	us
Power down time					5	us

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Main synthesizer in RX mode for DCS 1800 and PCS 1900						
Specification at the mixers LO port						
Prescaler input frequency range			3610 to 3980			MHz
PFD operating frequency				400		kHz
N divider ratio			9026 to 9949			
L divider by 2 output frequency range			1805 to 1990			MHz
Close in phase noise	@ 1 kHz offset fcomp = 400 kHz @ 1990 MHz				-81	dBc/Hz
Phase noise	@ 600 kHz offset @ 1.6 MHz offset @ 3.0 MHz offset @ 20 MHz offset				-120 -132 -137 -146	dBc/Hz
Reference feedthrough	@ 400 kHz offset @ 800 kHz offset @ 1.6 MHz offset				-53 -69 -82	dBc
Lock time	1) DCS1800: From 1805MHz to 1880MHz 2) PCS1900: From 1930MHz to 1990MHz 3) GSM850 ➔ PCS1900: From 869MHz to 1990MHz 4) GSM900 ➔ DCS1800: From 925MHz to 1880MHz @ 40 Hz averaged frequency error over one burst			tbd	170	us
Power up/down time						
Power up time	Output power within 10 % of steady state values				5	us
Power down time					5	us

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Main synthesizer in TX mode for GSM 850 and E-GSM 900						
Specification at the offset mixer LO port						
Prescaler input frequency range			3269 to 3957			MHz
PFD operating frequency	For GSM 850: [824.2 ~ 837.0 MHz] [837.2 ~ 848.8 MHz] For GSM 900			472.73 866.67 742.86		kHz
N divider ratio			4186 to 8370			
L divider by 4 output frequency range			817 to 990			MHz
M divider ratio	For GSM 850: [824.2 ~ 837.0 MHz] [837.2 ~ 848.8 MHz] For GSM 900			26 52 52		
M divider output frequency range			62 to 153			MHz
Close in phase noise	GSM850: @ 1 kHz offset fcomp = 472.73 kHz @ 990 MHz GSM900: @ 1 kHz offset fcomp = 742.86 kHz @ 850 MHz				-81 -81	dBc/Hz
Phase noise	@ 400 kHz offset				-120	dBc/Hz
Reference feedthrough	GSM 850: @ 472.73 kHz offset @ 866.67 kHz offset GSM900: @ 742.86 kHz offset				 -69 -67 -67	dBc
Lock time	@ 20 Hz averaged frequency error over one burst			tbd	235	us

Power up/down time

Power up time	Output power within 10 % of steady state values				5	us
Power down time					5	us

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Main synthesizer in TX mode for DSC 1800 and PCS 1900

Specification at the offset mixer LO port

Prescaler input frequency range			3176 to 3547			MHz
PFD operating frequency				371.43		kHz
N divider ratio			8551 to 9549			
L divider by 2 output frequency range			1588 to 1774			MHz
M divider ratio				26		
M divider output frequency range			122 to 137			MHz
Close in phase noise	@ 1 kHz offset fcomp = 371.43 kHz @ 1774 MHz				-81	dBc/Hz
Phase noise	@ 400 kHz offset				-120	dBc/Hz
Reference feedthrough	@ 371.43 kHz offset				-69	dBc
Lock time	@ 40 Hz averaged frequency error over one burst			tbd	235	us

Synthesizer Power up / down time

Power up time	Output power within 10 % of steady state values				5	us
Power down time					5	us

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

TRANSMITTER

Transmitter inputs

I/Q inputs common mode voltage			1.215	1.35	1.485	V
I/Q inputs voltage swing	Single ended		0.44	0.47	0.49	Vpp
I/Q inputs resistance	Differential ended		10			kO
I/Q inputs capacitance	Differential ended				25	pF

Low Band Output

Dedicated to GSM850 and E-GSM900

GMSK modulated signal applied at the IQ inputs (unless otherwise specified)

Frequency range		f_{out}	824.2 to 914.8			MHz
Output impedance		Z_{out}		50		O
Output Return Loss					-10	dB
Output power level	into 50 O load	P_{out}	4	6	8	dBm
Phase error	Max. RMS phase error Max. Peak phase error				3 10	degree
TXVCOLB Pulling	VSWR = 2, all phases, open loop	PULL		tbd		MHz

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Low Band Output (continued)

68 kHz CW signal applied at the IQ inputs (unless otherwise specified)

Carrier Suppression	With respect to the carrier	CS	-35			dBc
Sideband Suppression	With respect to the carrier	SBS	-40			dBc
Spurs @ 4×fIQ	With respect to the carrier	S4C	-50			dBc
Phase Noise	@ 400 kHz offset from the carrier @ 20 MHz offset from the carrier	PN_{400} PN_{20M}		-117	-113 -164[19]	dBc/Hz
Settling time[20]	From power down to final frequency @ 20 Hz averaged frequency error over one burst				240	us

[19] Measured with a Spectrum Analyzer as defined by ETSI norm – No corrective factor applied – The specification of –164dBc/Hz with +6dBm output power is equivalent to a measurement of –108dBm into 100kHz RBW

[20] Including settling time of the MAIN PLL

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

High Band Output

Dedicated to DCS1800 and PCS 1900

GMSKmodulated signal applied at the IQ inputs (unless otherwise specified)

Frequency range		f_{out}	1710.2 to 1909.8			MHz
Output impedance		Z_{out}		50		O
Output Return Loss					-10	dB
Output power level	into 50 O load	P_{out}	4	6	8	dBm
Phase error	Max. RMS phase error Max. Peak phase error				3 10	degree
TXVCOHB Pulling	VSWR = 2, all phases, open loop	PULL		tbd		MHz

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

High Band Output (continued)

68 kHz CW signal applied at the IQ inputs (unless otherwise specified)

Carrier Suppression	With respect to the carrier	CS	-35			dBc
Sideband Suppression	With respect to the carrier	SBS	-40			dBc
Spurs @ 4×fIQ	With respect to the carrier	S4C	-50			dBc
Phase Noise	@ 400 kHz offset from the carrier @ 20 MHz offset from the carrier	PN_{400} PN_{20M}		-117	-113 -152[21]	dBc/Hz
Settling time[22]	From power down to final frequency @ 40 Hz averaged frequency error over one burst				240	us

[21] Measured with a SpectrumAnalyzer as defined by ETSI norm – No corrective factor applied – The specification of –152dBc/Hz with +6dBm output power is equivalent to a measurement of –96dBm into 100kHz RBW

[22] Including settling time of the MAIN PLL

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Modulated output spectrum

GSM 850 / E-GSM 900

Maximum allowed level	@ 200 kHz offset[23]				-30	dBc
	@ 250 kHz offset[23]				-33	dBc
	@ 400 kHz offset[23]			-64	-60	dBc
	>= 600 kHz < 1.8 MHz offset[23]				-60	dBc
	>= 1.8 MHz < 3.0 MHz offset[24]				-63	dBc
	>= 3.0 MHz < 6.0 MHz offset[24]				-65	dBc
	>= 6.0 MHz offset[24]				-71	dBc

DCS 1800

Maximum allowed level	@ 200 kHz offset[23]				-30	dBc
	@ 250 kHz offset[23]				-33	dBc
	@ 400 kHz offset[23]			-64	-60	dBc
	>= 600 kHz < 1.8 MHz offset[23]				-60	dBc
	>= 1.8 MHz < 6.0 MHz offset[24]				-65	dBc
	>= 6.0 MHz offset[24]				-73	dBc

PCS1900

Maximum allowed level	@ 200 kHz offset[23]				-30	dBc
	@ 250 kHz offset[23]				-33	dBc
	@ 400 kHz offset[23]			-64	-60	dBc
	>= 600 kHz < 1.2 MHz offset[23]				-60	dBc
	>= 1.2 MHz < 1.8 MHz offset[23]				-60	dBc
	>= 1.8 MHz < 6.0 MHz offset[24]				-65	dBc
	>= 6.0 MHz offset[24]				-73	dBc

[23] Observed in 30 kHz RBW
[24] Observed in 100 kHz RBW

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Spurious emissions[25]

Specification at the **antenna with the use of the TBD PA and the TBD FEM**

E-GSM 900

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [925 ~ 935 MHz]				-100	dBc
	in the band [935 ~ 960 MHz]				-112	dBc
	in the band [1805 ~ 1880 MHz]				-104	dBc
	in the bands [1900 ~1920 MHz], [1920 ~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-99	dBc

DCS 1800

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [925 ~ 935 MHz]				-97	dBc
	in the band [935 ~ 960 MHz]				-109	dBc
	in the band [1805 ~ 1880 MHz]				-101	dBc
	in the bands [1900 ~1920 MHz], [1920 ~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-96	dBc

GSM 850

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [869 ~ 894 MHz]				-112	dBc
	in the band [1930 ~ 1990 MHz]				-104	dBc

PCS 1900

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [869 ~ 894 MHz]				-109	dBc
	in the band [1930 ~ 1990 MHz]				-101	dBc

[25] Spurious emissions above the values specified in the table will be measured at the TX VCO output (HBTXOUT pin and LBTXOUT pin). This measurement is made for one allocated channel (chosen in the Mid ARFCN range) per band.

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Power Amplifier Controller

Low pass filter for DAC signal (1st order)

Cut off frequency			420	600		kHz

Sense amplifier

Slew Rate (pos and neg)			4	5		V/µsec
Input Offset Voltage			-10	0	10	mV
Unity gain bandwidth			5			MHz
Max Output Voltage			2.5			V
Min Output Voltage					100	mV
Input Voltage Range			0		2.7	V
Matching Ratio accuracy between Cap					1	%
Current leakage at negative input					20	pA

Integrator

Slew Rate (pos and neg)			4	5		V/µsec
Input Offset Voltage			-20	0	20	mV
Output current	Vout = 2.5V Rload = 300 Ω				8.4	mA
Unity gain bandwith			5			MHz
Max Output Voltage			2.5			V
Min Output Voltage					100	mV
Input Voltage Range			0		2.5	V
Rload			300			Ω
Cload			1		100	pF
R integrator range[26]		R int		150 to 300		kΩ
C integrator range[27]		C int		12.5 to 50		pF

Current generators

I1			21	30	39	uA
I2			210	300	390	uA
Temperature dependence	-25 to +85 C				5	%

Home position voltage

Mimimal Vhome[28]					0.5	V
Maximal Vhome[28]			1.3			
VHome step				27		mV

[26] R may be open by program for tests
[27] C may be open by program for tests
[28] VHome is programmable with a 5 bits DAC through the serial interface

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

Power up/down time

Power up time	Output power within 10 % of steady state values				5	us
Power down time					5	us

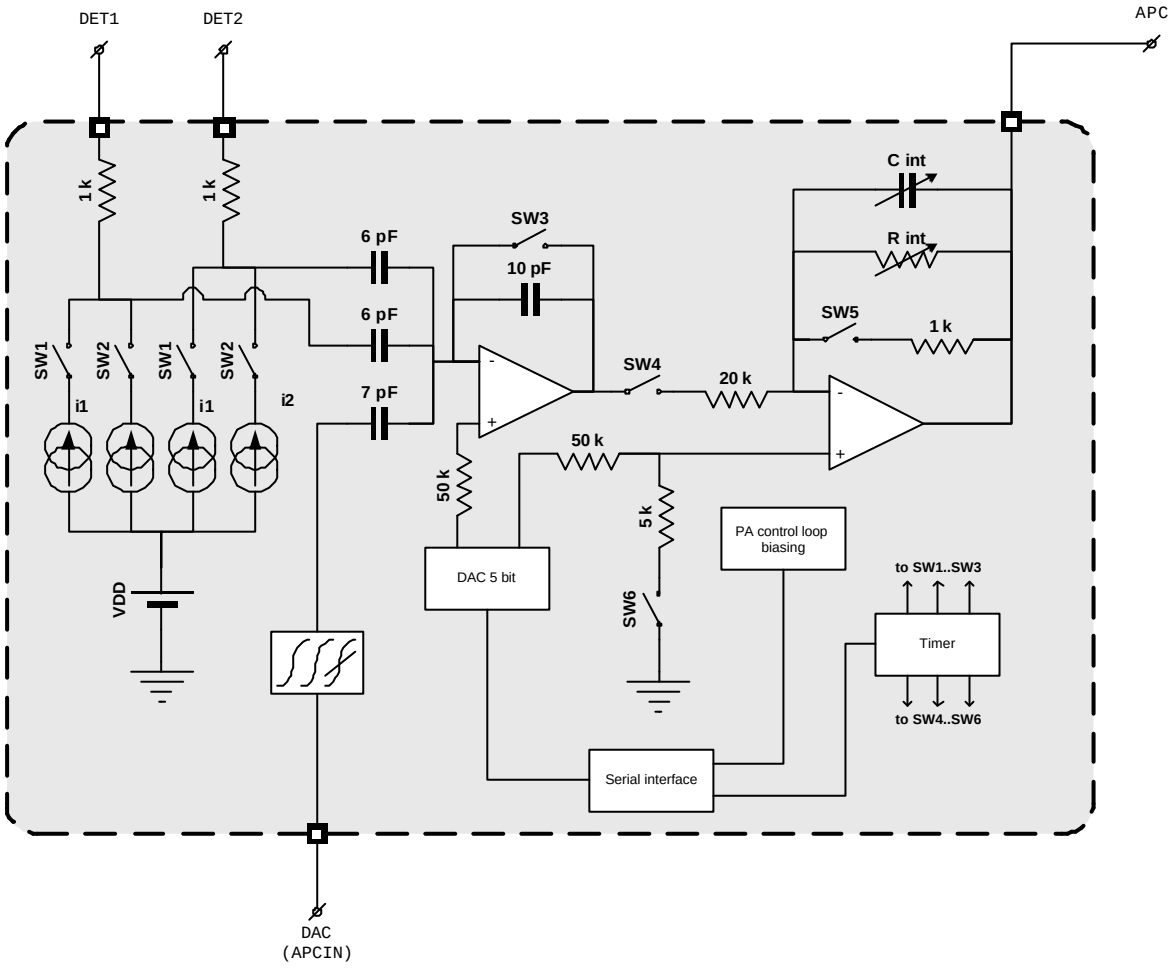


Figure 8 - PA controller block diagram

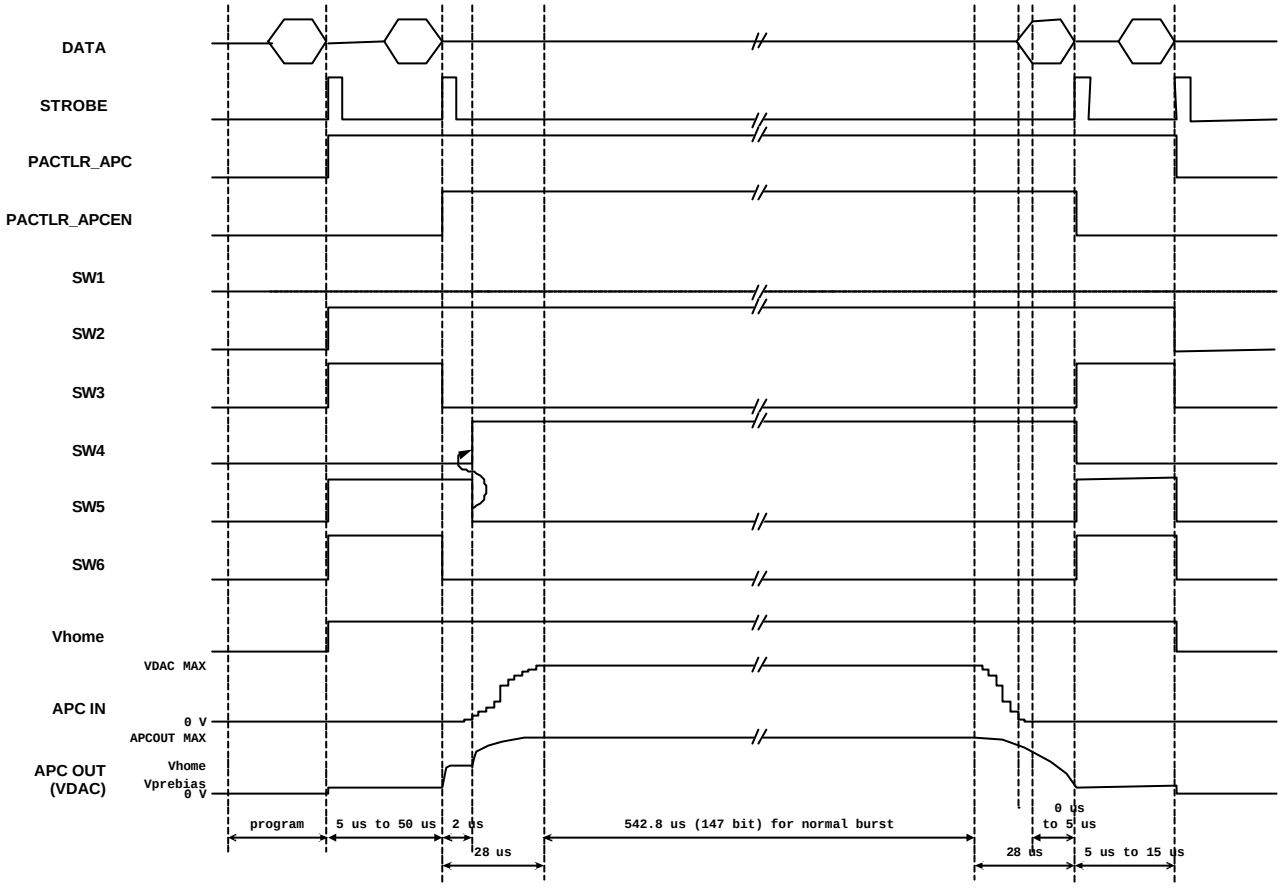


Figure 9 - PA controller timing diagram for I2 current solution – single slot configuration

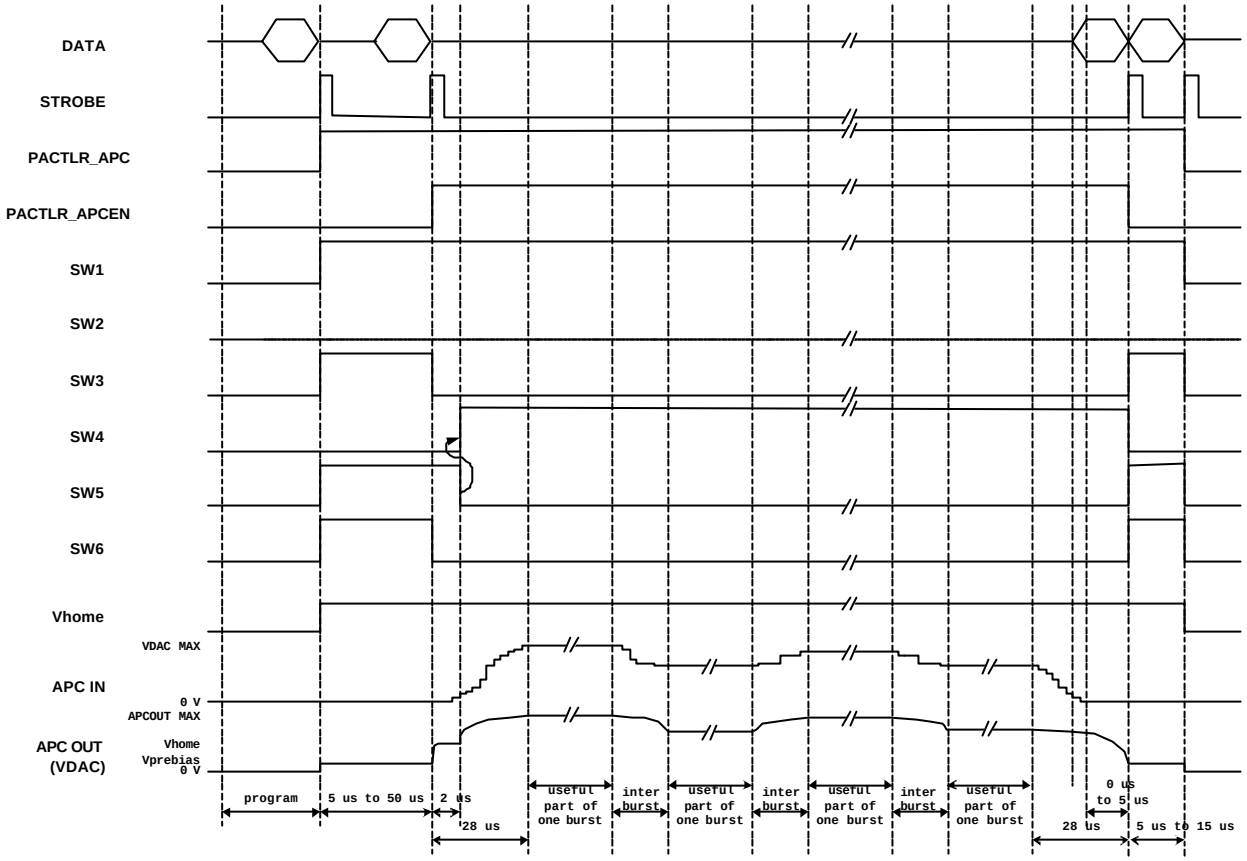


Figure 10 - PA controller timing diagram for I1 current solution – multislot configuration

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

RECEIVER

Global performances

RF input frequency	LNAGSMN/P pins		869	-	960	MHz
	LNADCSN/P pins		1805	-	1880	MHz
	LNAPCSN/P pins		1930	-	1990	MHz
Balanced RF input impedance	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins		-	100	-	Ω
RF input return loss	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins Receiver gain = G_HIGH or G_MID1		-	-	-10	dB
	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins Receiver gain = G_MID2 or G_LOW		-	-	-4	dB
Voltage gain [29]	All bands Front end and VGA high gain mode	G_HIGH	63	66	69	dB
	All bands Front end in intermediate gain mode and VGA in high gain mode	G_MID1	57	60	63	dB
	All bands Front end in low gain mode and VGA in high gain mode	G_MID2	43	46	49	dB
	All bands Front end and VGA in low gain mode	G_LOW	17	20	23	dB
Noise figure [30]	LNAGSMN/P pins; G=G_HIGH GSM900 band [925,960Mhz]		-	-	5	dB
	LNAGSMN/P pins[31]; G=G_HIGH GSM850 band [869,894Mhz]		-	-	5.2	dB
	LNADCSN/P pins; G=G_HIGH DCS band [1805,1880Mhz]		-	-	5	dB
	LNAPCSN/P pins; G=G_HIGH PCS band [1930,1990Mhz]		-	-	5	dB
	All bands; G= G_MID2		-	-	20.8	dB
Input 1dB compression point	All bands Gain = G_HIGH		-50	-	-	dBm
	GSM850-GSM900 bands G= G_LOW		-19.5	-	-	dBm
	DCS1800 – PCS1900 bands G= G_LOW		-25	-	-	dBm
Input 3rd order intercept point	All bands Gain = G_HIGH[32]		-20	-18	-	dBm

[29] From 50Ω single ended voltage source output (matched to LNA differential input) to one receiver differential output. See Annex 2 (page 60) for more details.
[30] NF is measured from LNA matched differential input to one receiver differential output (IN/P or QN/P pins). Matching losses with low Q components are in cluded. Noise is averaged over 1kHz to 100kHz.
[31] For quad band, GSM900 hardware is used to receive GSM850 signal as well. See Annex 3 (page 61) for more details
[32] For IIP3 tests, interferers are 2 sine waves at 800kHz and 1.6Mhz from carrier applied at LNA input with a power level=-51dBm.

Parameters	Test conditions	Min.	Typ.	Max.	Unit

Global performances (continued)

Input 1dB blocking compression point	See table in Annex 5 (page 66)				dBm
Noise figure in blocking conditions[33;34]	Receiver in high gain mode (G_HIGH):				
	LNAGSMN/P pins, GSM band	-		11	dB
	LNAGSMN/P pins, GSM850 band [35]	-		11.2	dB
	LNADCSN/P pins, DCS band	-		11	dB
	LNAPCSN/P pins, PCS band	-		11	dB
	Receiver is in "intermediate" gain mode (G_MID1):				
	LNAGSMN/P pins, GSM900 band	-		10.9	dB
	LNAGSMN/P pins, GSM850 band [35]	-		11.1	dB
	LNADCSN/P pins, DCS band	-		10.9	dB
	LNAPCSN/P pins, PCS band	-		10.9	dB
LO/2 feedthrough at RF port[36]	LNAGSMN/P pins, GSM850 band LNAGSMN/P pins, GSM900 band Gain=G_HIGH	-	-	-80	dBm
	LNAGSMN/P pins, GSM850 band LNAGSMN/P pins, GSM900 band Gain=G_MID1	-	-	-74	dBm
	LNAGSMN/P pins, GSM850 band LNAGSMN/P pins, GSM900 band Gain=G_LOW	-	-	-54	dBm
LO/4 feedthrough at RF port[36]	LNADCSN/P pins, DCS band LNAPCSN/P pins, PCS band Gain=G_HIGH	-	-	-80	dBm
	LNADCSN/P pins, DCS band LNAPCSN/P pins, PCS band Gain=G_MID1	-	-	-74	dBm
	LNADCSN/P pins, DCS band LNAPCSN/P pins, PCS band Gain=G_LOW	-	-	-44	dBm
IQ Phase unbalance	@ 67.7kHz, All bands, between IN/P and QN/P pins	-5	-	+5	Deg
IQ Amplitude unbalance	All bands, between IN/P and QN/P pins	-0.8	-	0.8	dB
TRF6151 filters	Global 3dB cut-off-frequency	109	141	204	kHz
	Global attenuation	See plots in Annex 4 (page 63)			dB

[33] NF is measured from LNA matched differential input to one receiver differential output (IN/P or QN/P pins). Matching losses with low Q components are included. Noise is averaged over 1kHz to 100kHz.
[34] Blocking signal power level and its frequency offset from carrier are defined in Table 1.
[35] For quad band, GSM900 hardware is used to receive GSM850 signal as well. See Annex 3 (page 61) for more details
[36] LO is the frequency delivered by the VCO RX.

Parameters	Test conditions	Min.	Typ.	Max.	Unit

Global performances (continued)

Static differential DC offset	On IN/P or QN/P path Gain=G_HIGH or G_MID1 LNA is OFF 600 kHz blocker applied at LNA input[37] After DC offset compensation	-	-	80	mV
	On IN/P or QN/P path Static DC offset calibrated Gain=G_HIGH or G_MID1 LNA is switched on after calibration 3Mhz blocker is applied at LNA input[37]	-	-	180	mV
Time-varying differential DC offset	On IN/P or QN/P path Static DC offset calibrated Gain= G_HIGH or G_MID1 LNA is switched on after calibration AM suppression ETSI test case[38]			0.5	DC ratio[39]
Output DC offset calibration time				50	usec
Receiver settling time	See Annex 8 (page 70) for test procedure			175	usec
Output common mode voltage	On one IN/P or QN/P pin, after DC offset compensation	0.9	Vcc/2	1.9	V
Output resistance	Differential ended		TBD		kΩ
Output load impedance	Differential ended			200 10	kΩ pF

[37] See Table 1 for blocker level specification.
[38] See Table 2 for AM suppression test case definition
[39] DC ratio = [Time-varying differential DC offset]/ [Vpeak(useful signal)]

Table 1: Receiver noise figure in blocking condition: blocker frequency and power levels:

Band	Offset from carrier	Power level at LNA input (dBm)
All bands	600 kHz	-45dBm
GSM850 – GSM900	3 MHz	-25dBm
DCS1800 – PCS1900	3 MHz	-28dBm
GSM900	10 MHz	-25dBm
GSM850	20 MHz	-22dBm
GSM900	20 MHz	-23dBm
DCS1800	20 MHz	-27dBm
PCS1900	20MHz	-23dBm
DCS1800	100MHz	-23dBm

Table 2 :AM suppression test case definition

For AM suppression test, the following signals are applied at LNA input:

- S1 = a GMSK useful signal in Mid ARFCN range, with a power level =-103 dBm
- S2 = a GMSK interferer signal, at 6Mhz offset from useful signal, synchronized with the useful signal, but delayed by 70 bits, with a power level = –33dBm

Test case #	Band	S1		S2	
		Power level	Frequency	Power level	Frequency
1	GSM850	-103dBm	882MHz	-33dBm	888MHz
2	GMS900		942Mhz		948Mhz
3	DCS1800		1842MHz		1848MHz
4	PCS1900		1960Mhz		1966Mhz

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Low band GSM850-GSM900 LNA (LNAGSM) + IQ demodulator (MIXGSM)						
RF input frequency	LNAGSMN/P pins		869	-	960	MHz
Balanced RF input impedance	LNAGSMN/P pins		-	100	-	Ω
RF input return loss	LNAGSMN/P Voltage gain = G1 or G2		-	-	-10	dB
	LNAGSMN/P pins Voltage gain = G3		-	-	-4	dB
Voltage gain[40]	High gain mode	G1	24	26	28	dB
	Intermediate gain mode[41]	G2	18	20	22	dB
	Low gain mode[42]	G3	4	6	8	dB
Noise figure[43]	GSM900 band, Voltage gain=G1[44]		-		4.7	dB
	GSM850 band, Voltage gain=G1		-		4.9	dB
	GSM850 or GSM900 band,Voltage gain=G2				8.8	dB
	GSM850 or GSM900 band,Voltage gain=G3		-		20	dB
Input 1dB blocking compression point	Voltage gain=G1 or G2 GSM850 and GSM900 bands Blocker @ 3 Mhz from carrier		-28	-27	-	dBm
	Voltage gain=G1 or G2 GSM900 band Blocker @ 10 Mhz from carrier		-28	-27	-	dBm
	Voltage gain=G1 or G2 GSM850 band Blocker @ 20 Mhz from carrier		-25	-24	-	dBm
	Voltage gain=G1 or G2 GSM900 band Blocker @ 20 Mhz from carrier		-26	-25	-	dBm
Input 1dB compression point	GSM850 or GSM900 band, Voltage gain=G3		-19	-	-	dBm
Noise figure in blocking conditions[45]	GSM900 band, Voltage gain=G1		-		9.1	dB
	GSM900 band, Voltage gain=G2		-		8.6	dB
	GSM850 band, Voltage gain=G1		-		9.3	dB
	GSM850 band, Voltage gain=G2		-		8.8	dB
Input 3rd order intercept point[46]	GSM850 and GSM900 bands Voltage gain=G1		-18	-17	-	dBm
LO/4 feedthrough at RF port[47]	GSM850 and GSM900 bands Voltage gain= G1		-	-	-80	dBm
	GSM850 and GSM900 bands Voltage gain= G2		-	-	-74	dBm
	GSM850 and GSM900 bands Voltage gain= G3		-	-	-54	dBm

[40] From 50Ω single ended voltage source output (matched to LNA differential input) to one IQ demodulator differential output (MIXIN/P or MIXQN/P internal pads). See Annex 2 (page 60) for more details.
[41] A 6 dB gain switch is implemented in the LNA.
[42] A 20 dB gain switch is implemented in the LNA/mixer
[43] NF is measured from LNA matched differential input to one receiver differential output (MIXIN/P or MIXQN/P internal pads). Matching losses with low Q components are included. Noise is averaged over 1kHz to 100kHz.
[44] GSM900 band in Rx mode is [925Mhz; 960 Mhz]. GSM850 band in Rx mode is [869Mhz; 894 Mhz].
[45] These figure are given for design purpose. They do not include LO phase noise contribution.
[46] For IIP3 tests, interferers are 2 sine waves at 800kHz and 1.6Mhz from carrier applied at LNA input with a P=-51dBm.
[47] LO is the frequency delivered by the VCO RX.

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

DCS LNA (LNADCS) + IQ demodulator(MIXDCS)

RF input frequency	LNADCSN/P pins		1805	-	1880	MHz
Balanced RF input impedance	LNADCSN/P pins		-	100	-	Ω
RF input return loss	LNADCSN/P pins Voltage gain= G1 or G2		-	-	-10	dB
	LNADCSN/P pins Voltage gain= G3		-	-	-4	dB
Voltage gain [48]	High gain mode	G1	24	26	28	dB
	Intermediate gain mode[49]	G2	18	20	22	dB
	Low gain mode[50]	G3	4	6	8	dB
Noise figure[51]	Voltage gain=G1		-		4.7	dB
	Voltage gain=G2		-		8.6	dB
	Voltage gain=G3		-		20	dB
Input 1dB blocking compression point	Voltage gain=G1 or G2 Blocker @ 3 Mhz from carrier		-31	-30		dBm
	Voltage gain=G1 or G2 Blocker @ 20 Mhz from carrier		-30	-29	-	dBm
	Voltage gain=G1 or G2 Blocker @ 100 Mhz from carrier		-26	-25		dBm
Input 1dB compression point	Voltage gain=G3		-25	-	-	dBm
Noise figure in blocking conditions[52]	Voltage gain=G1		-		9.1	dB
	Voltage gain=G2		-		8.6	dB
Input 3rd order intercept point[53]	Voltage gain=G1		-18	-17	-	dBm
LO/4 feedthrough at RF port[54]	Voltage gain= G1		-	-	-80	dBm
	Voltage gain= G2		-	-	-74	dBm
	Voltage gain= G3		-	-	-44	dBm

[48] From 50Ω single ended voltage source output (matched to LNA differential input) to one IQ demodulator differential output (MIXIN/P or MIXQN/P internal pads). See Annex 2 (page 60) for more details.
[49] A 6 dB gain switch is implemented in the LNA.
[50] A 20 dB gain switch is implemented in the LNA/mixer
[51] NF is measured from LNA matched differential input to one receiver differential output (MIXIN/P or MIXQN/P internal pads). Matching losses with low Q components are included. Noise is averaged over 1kHz to 100kHz.
[52] These figure are given for design purpose. They do not include LO phase noise contribution.
[53] For IIP3 tests, interferers are 2 sine waves at 800kHz and 1.6Mhz from carrier applied at LNA input with a power level=-51dBm.
[54] LO is the frequency delivered by the VCO RX.

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit

PCS LNA (LNAPCS) + IQ demodulator (MIXPCS)

RF input frequency	LNAPCSN/P pins		1930	-	1990	MHz
Balanced RF input impedance	LNAPCSN/P pins		-	100	-	Ω
RF input return loss	LNAPCSN/P pins Voltage gain= G1 or G2		-	-	-10	dB
	LNAPCSN/P pins Voltage gain= G3		-	-	-4	dB
Voltage gain[55]	High gain mode	G1	24	26	28	dB
	Intermediate gain mode[56]	G2	18	20	22	dB
	Low gain mode[57]	G3	4	6	8	dB
Noise figure[58]	Voltage gain=G1		-		4.7	dB
	Voltage gain=G2		-		8.6	dB
	Voltage gain=G3		-		20	dB
Input 1dB blocking compression point	Voltage gain=G1 or G2 Blocker @ 3 Mhz from carrier		-31	-30	-	dBm
	Voltage gain=G1 or G2 Blocker @ 20 Mhz from carrier		-26	-25	-	dBm
Input 1dB compression point	Voltage gain=G3		-25	-	-	dBm
Noise figure in blocking conditions[59]	Voltage gain=G1		-		9.1	dB
	Voltage gain=G2		-		8.6	dB
Input 3rd order intercept point[60]	Voltage gain=G1		-18	-17	-	dBm
LO/4 feedthrough at RF port[61]	Voltage gain= G1		-	-	-80	dBm
	Voltage gain= G2		-	-	-74	dBm
	Voltage gain= G3		-	-	-44	dBm

[55] From 50Ω single ended voltage source output (matched to LNA differential input) to one IQ demodulator differential output (MIXIN/P or MIXQN/P internal pads). See Annex 2 (page 60) for more details.
[56] A 6 dB gain switch is implemented in the LNA.
[57] A 20 dB gain switch is implemented in the LNA/mixer
[58] NF is measured from LNA matched differential input to one receiver differential output (MIXIN/P or MIXQN/P internal pads). Matching losses with low Q components are included. Noise is averaged over 1kHz to 100kHz.
[59] These figure are given for design purpose. They do not include LO phase noise contribution.
[60] For IIP3 tests, interferers are 2 sine waves at 800kHz and 1.6Mhz from carrier applied at LNA input with a power level=-51dBm.
[61] LO is the frequency delivered by the VCO RX.

Parameters	Test conditions	Min.	Typ.	Max.	Unit
Post IQ demodulator low pass filter					
Filter order			1		-
Filter cut off frequency		275	338	438	kHz
Base band amplifier (VGA)					
Global characteristics					
Maximum gain voltage		39	40	41	dB
Voltage gain control range		13 to 39	14 to 40	15 to 41	dB
Gain step		-	2	-	dB
Gain error linearity	In any 20dB window	-	±1	±1.5	dB
SSB Input averaged noise[62]	VGA gain ∈ [34; 40dB]	-		4.6	nVrms /√Hz
	VGA gain ∈ [14; 40dB]	See specification in figure 1			
Input 1dB blocking compression point	VGA gain ∈ [34; 40dB] Blocker @330kHz	-32	-31	-	dBvp
	VGA at max gain, Blocker @600 kHz	-34	-33	-	dBvp
	VGA at max gain, Blocker @1.6MHz	-30	-29	-	dBvp
	VGA at max gain, Blocker @ 3MHz	-26	-25	-	dBvp
Input 1dB compression point	VGA gain=14 to 40dB	See specification in figure 2			
Input 3rd order intercept point	VGA gain ∈ [34; 40dB], blocker @ 0.8 and 1.6MHz offset from carrier[63]	-10	-9		dBvp
Output load impedance	Differential ended			200 10	kΩ pF
Common mode output voltage		1	VCC/2	1.8	V
VGA output resistance	Differential ended			1	kΩ

[62] Noise is averaged over 1kHz to 100kHz

[63] Interferer for IIP3 tests are applied at antenna with a power level=-49dBm ⇒ at VGA input, we have: -40dBvp for the 800kHz interferer and -44dBvp for the 1.6Mhz interferer

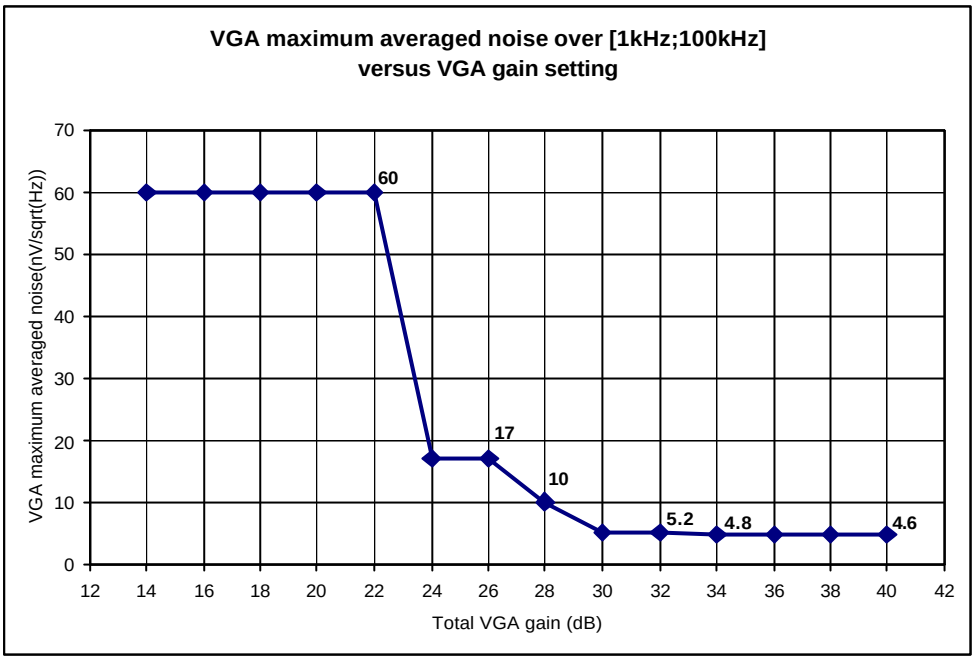


Figure 11 - VGA maximal noise vs gain setting

Gain	dB	14	16	18	20	22	24	26	28	30	32	34	36	38	40
Max. input noise	nV/sqrt(Hz)*	60	60	60	60	60	17	17	10	5.2	5.2	4.8	4.6	4.6	4.6

*Noise is averaged on [1kHz;100kHz] band

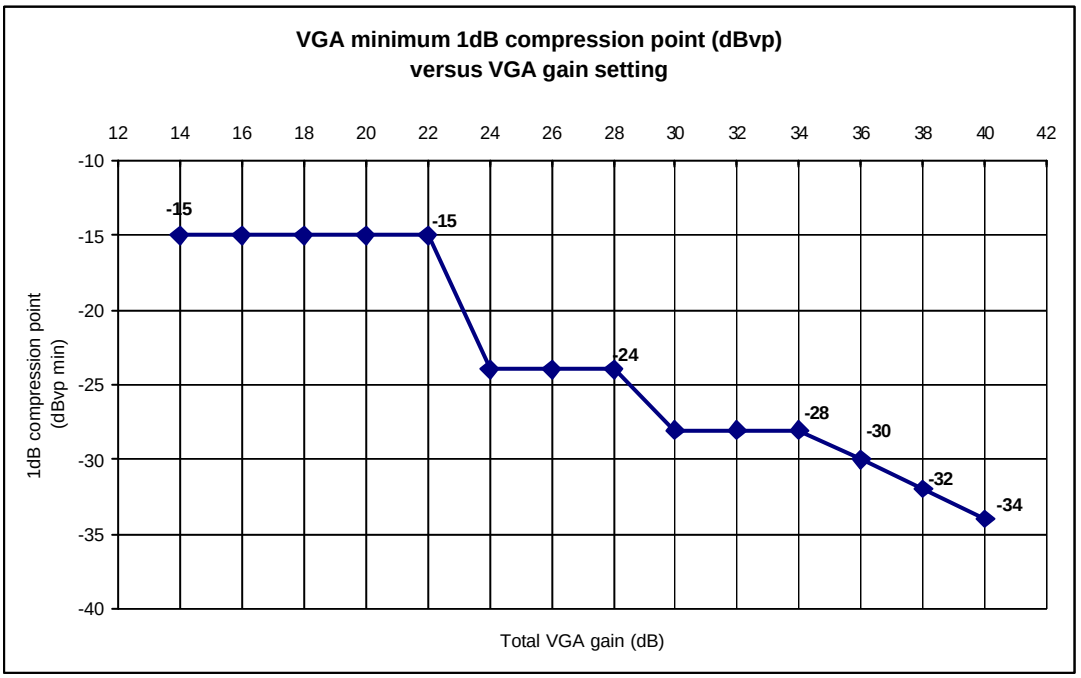


Figure 12 - VGA minimum P1dB vs gain setting

Gain	dB	14	16	18	20	22	24	26	28	30	32	34	36	38	40
PC1dBi min	dBv	-15	-15	-15	-15	-15	-24	-24	-24	-28	-28	-28	-30	-32	-34

Parameters	Test conditions	Min.	Typ.	Max.	Unit

VGA filters

VGA low pass filter #1	Order	-	1	-	-
	3dB cut-off-frequency	0.9	1.2	1.8	MHz
VGA low pass filter #2	Order	-	2	-	-
	Type	Butterworth			-
	3dB cut-off-frequency	120	155	230	kHz

DC offset compensation system

Output DC offset voltage	On IN/P or QN/P path RF Gain=G1 or G2 VGA gain ∈ [24; 40dB] LNA is OFF, 600 kHz blocker applied at LNA input[64] After DC offset compensation,	DCO0a			80	mV
	On IN/P or QN/P path RF Gain=G1 or G2 VGA gain ∈ [14; 22dB] LNA is OFF, 600 kHz blocker applied at LNA input[65] After DC offset compensation,	DCO0b			130	mV
	On IN/P or QN/P path Static DC offset calibrated RF Gain=G1 or G2 VGA gain is maximum LNA is switched on after calibration No signal at LNA input	DCO1			160	mV
	On IN/P or QN/P path Static DC offset calibrated RF Gain=G1 or G2 VGA gain is maximum LNA is switched on after calibration 3Mhz blocker is applied at LNA input[37]	DCO2			180	mV
Time-varying differential DC offset	On IN/P or QN/P path Static DC offset was calibrated Gain= G_HIGH or G_MID LNA is switched on after calibration AM suppression ETSI test case[66]	DCO3			0.5	DC ratio[67]
Output DC offset calibration time					50	usec

Note: those values must be met for all RF bands: GSM850, GSM900, DCS or PCS, with no DC offset voltage drift during RX slot.

[64] See Table 1 for blocker level specification according band.
[65] See Table 1 for blocker level specification according band.
[66] See Table 2 for AM suppression test case definition
[67] DC ratio = [Time-varying differential DC offset]/ [Vpeak(useful signal)

Interferer detection system[68]

Parameters	Test conditions	Min.	Typ.	Max.	Unit
Detection threshold	on active LNA input pins LNA/mixer gain = G1 or G2[69] With GMSK useful signal @ Freq=F1, P1= -103dBm and a sinus interferer signal @ Freq=F2, P= [P2i to P2f] with 1dB step increment (See Table 3)	-40	-37.5	-35	dBm

Table 3: Test signals for interferer detection system:

Band	F1	F2	P2i	P2f
	MHz	MHz	dBm	dBm
GSM850	882	888	-42	-33
GSM900	942	948		
DCS1800	1842	1848		
PCS1900	1960	1966		

Receiver Power up / down time

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Power up time	Output power within 10% of steady state values				5	usec
Power down time					5	usec

[68] See Annex 7 (page 68) for more details

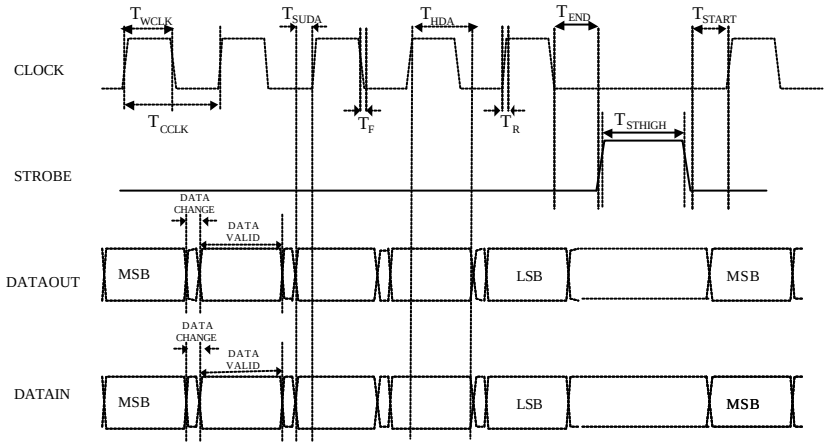
[69] This requires 2 different hardware thresholds at the mixer output, separated by G1-G2+2dB = 8dB.

SERIAL DATA INTERFACE DESCRIPTION

The serial interface of TRF6151 consists of a 4-wire serial bus, comprising DATAIN, DATAOUT, CLOCK and STROBE signals. These signals are used to communicate with the serial port TSP of digital base band chip:

- In the uplink path (from DBB to RF), to enter control words into the RF chip. The control words contain information for programming the regulators, the synthesizers, the receiver and the offset PLL according to the protocol described in this document.
- In the downlink path (from RF to DBB), to inform the digital base band chip (DBB) with data about RF environment. DATAOUT is also used for test purpose.

Serial interface timing



Symbol	Description	Min	Typ.	Max	Unit
T_{CCLK}	CLOCK: Cycle time	153.8	-	-	ns
T_{WCLK}	CLOCK: Pulse duration	69	-	-	ns
T_F	CLOCK: fall time (at max rating)	-	-	5	ns
T_R	CLOCK: rise time (at max rating)	-	-	5	ns
T_{SUDA}	Setup, Data valid before CLOCK ↑	15	-	-	ns
T_{HDA}	Hold time, Data valid after CLOCK ↑	15	-	-	ns
T_{END}	Delay time, CLOCK ↓ before STROBE ↑	70			ns
T_{START}	Delay time, STROBE ↓ before CLOCK ↑	70			ns
T_{STHIGH}	Pulse width: STROBE high	150			ns

DATAOUT is sampled by the DBB on CLOCK rising edge. DATAIN is provided by the DBB on each CLOCK falling edge and sampled by TRF6151 in a shift register on each CLOCK rising edge. The shift register content is copied into latches on the STROBE signal rising edge. Most significant bit is clocked in first.

At TRF6151 initialization, reset of serial interface registers is done by a digital signal (active low) applied on the RESETZ pin.

SERIAL INTERFACE PROGRAMMING

The serial interface is divided into 8 different registers. The serial word contains a total of 16 bits. The serial mode controller selects a register by reading the 3 LSB of the serial word.

Serial word format

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Registers table

Address			Serial word format	Register name	Definition
0	0	0	16 bits	REG_RX	RF general settings
0	0	1	16 bits	REG_PLL	PLLs settings
0	1	0	16 bits	REG_PWR	Power on/off all functional block of the transceiver
0	1	1	16 bits	REG_CFG	Transceiver config, PA Controller setting
1	0	0	16 bits	REG_TEST1	Reserved for test[70]
1	0	1	16 bits	REG_TEST2	
1	1	0	16 bits	REG_TEST3	
1	1	1	16 bits	REG_TEST4	

[70] See design specification for the test registers.

REG_RX register

This register is used to configure the receiver, to launch RX calibration process and to read/reset the "interferer detector" results.

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	0	0	0

Bit	Name	Description	Value at reset
15:11	VGA_GAIN	**00000 - 00101:** reserved **00110:** VGA gain =14dB **00111:** VGA gain =16 dB **01000:** VGA gain =18 dB **01001:** VGA gain =20 dB **01010:** VGA gain =22 dB **01011:** VGA gain =24 dB **01100:** VGA gain =26 dB **01101:** VGA gain =28 dB **01110:** VGA gain =30 dB **01111:** VGA gain =32 dB **10000:** VGA gain =34 dB **10001:** VGA gain =36 dB **10010:** VGA gain =38 dB **10011:** VGA gain =40 dB **10100 - 11111:** reserved	10011
10:9	RF_GAIN	**00:** low RF gain (G3) **01**: intermediate RF gain (G2) **10:** reserved **11**: high RF gain (G1)	11
8	RX_CAL_MODE[71]	**0**: Stop RX calibration process **1**: power on DC offset calibration system and start RX calibration process.	0
7	READ_EN	**0:** Data serialized on SIOUT pin are 0 **1:** Data serialized on SIOUT pin are REG_RX content => this enables the reading of BLOCK_DETECT value by the Digital base band chip.	0
6	RST_BLOCK_DETECT[1]	**0:** no action **1:** Reset BLOCK_DETECT[1][72]	0
5	RST_BLOCK_DETECT[0]	**0:** no action **1:** Reset BLOCK_DETECT[0][72]	0
4	BLOCK_DETECT[1]	Result of interferer detection on the current and last RX burst. Those bits are READ ONLY[73].	0
3	BLOCK_DETECT[0]		0

See Annex 7 for more details about blocker detection system.

[71] RX calibration process ends automatically. But, setting RX_CAL_MODE=0 may force the process to be stopped before its normal end.
[72] RST_BLOCK_DETECT[1:0] are TOGGLE bits, no need to write 0!
[73] BLOCK_DETECT content is updated according interferer detection value during each RX burst (mode B). BLOCK_DETECT cannot be directly updated by user using serial interface, but can be forced to 0 by setting RST_BLOCK_DETECT bits to 1. BLOCK_DETECT is also reset by RESETZ pin.

REG_PLL register

This register is used to program the synthesizer frequency according the desired RX/TX channel.

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	0	0	1

Bit	Name	Description	Value at reset
15:9	PLL_REGB	B = [64; 66; 67 ...155][74]	0000000
8:3	PLL _REGA	A = [0; 1; 2..63]	000000

Useful formulas for synthesizers are:

	P	R	L	M	B range	A range	RX/TX RF Frequency (MHz)
RX Low band	64	65	4	-	[135; 150]	[0; 62]	$\frac{(B*P+A)}{R*L}*26$
RX High band	64	65	2	-	[141; 155]	[0; 63]	
TX mode GSM850_1	64	55	4	26	[128; 130]	[0; 62]	$(\frac{1}{L}-\frac{1}{M})*\frac{(B*P+A)}{R}*26$
TX mode GSM850_2	64	30	4	52	[65; 66]	[0; 63]	
TX mode GSM900	64	35	4	52	[68; 71]	[0; 63]	$(\frac{1}{L}+\frac{1}{M})*\frac{(B*P+A)}{R}*26$
TX mode High band	64	70	2	26	[133; 149]	[0; 63]	

[74] B is varying on the [64;155] range but is coded on 7 bits.
To have B=64 in the PLL, user should program dec2bin(B-64)=dec2bin(0)=0000000
To have B=155 in the PLL, user should program dec2bin(B-64)=dec2bin(91)=1011011
In TRF6151 core, PLL_REGB contents is added with 64 and stored in an 8 bits register, used by PLLS.

REG_PWR register

This register is used to power on/off all functional block of the transceiver and to choose the RX/TX band.

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	0	1	0

Bit	Name	Description	Value at reset
15	PACTLR_APCEN	**0:** PA controller is disabled[75] **1:** PA controller is enabled	0
14	PACTLR_APC	**0:** PA controller is OFF[75] **1:** PA controller is ON	0
13	TX_MODE	**0:** Transmitter is OFF **1:** Transmitter is ON	0
12:11	RX_MODE	**00:** Receiver +interferer detection system are OFF **01:** Receiver is ON (RX mode A) **10:** Receiver +interferer detection system is ON (RX mode B1) **11:** Receiver +interferer detection system is ON (RX mode B2)	00
10:9	SYNTHE_MODE[76]	**00:** Synthesizer, transmitter and receiver are off **01:** RX Synthesizer is ON **10:** TX Synthesizer is ON **11:** not used	00
8:6	BAND	**000-001:** GSM900 **010-011:** DCS **100:** GSM850 (Low part) **101:** GSM850 (High part) **110-111:** PCS	000
5	REGUL_MODE	**0:** Regulators are OFF **1:** Regulators are ON	0
4:3	BANDGAP_MODE	**00-01:** Band gap is OFF **10:** Band gap is ON; speed up mode is disabled **11:**Band gap is ON; speed up mode is enabled	00

Table 4 Receive Mode description

Mode	Receiver status	Interferer detector
RX mode A	Receiver is ON i.e RX path (LNA, mixer, VGA) and RX synthesizer are ON.	OFF
RX mode B1		Interferer detector is ON and detection result is stored in REG_RX bit#3 at the end of the RX window
RX mode B2		Interferer detector is ON and detection result is stored in REG_RX bit#4 at the end of the RX window

[75] See PA controller timing diagram for details about all control associated with PACTLR_APC and PACTLR_APCEN bit.
[76] VCO calibration is launched when SYNTHE_MODE is set from '0' to '1' (when RX synthesizer ON or TX synthesizer ON is programmed)

REG_CFG register

This register is used to configure the transceiver and set the PA controller at mobile initialization.

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	0	1	1

Bit	Name	Description	Value at reset
15	ILOGIC_INIT_DIS	**0:** Initialize internal logical blocks[77], once regulators are switched on. **1:** Disable initialization of internal logical blocks	0
14	TEMP_SENSOR	**0:** Temperature sensor is OFF **1:** Temperature sensor is ON	0
13:12	PACTLR_CAP	**00:** 0 pF **01:** 12.5 pF **11:** 25 pF **10:** 50 pF	10
11:10	PACTLR_RES	**00:** open **01:** 150 kΩ **10:** 300 kΩ **11:** not used	10
9:5	PACTLR_VHOME	PA controller detection voltage setting:[78] **00000:**0*Vstep+Vlow ~ 0.46 V **00001:**1*Vstep+Vlow ~ 0.49 V **00010:** 2*Vstep+Vlow ~ 0.52 V … **11111:** 31*Vstep+Vlow ~ 1.39 V	01100
4	PACTLR_IDIOD	**0:** Diode bias current is low (30 uA) **1:** Diode bias current is high (300 uA)	0
3	PACTLR_TYPE	**0:** Power sensing **1:** Current sensing (for test purpose only)	0

[77] Caution! This bit **is not** a global reset of the RF chip contents. This only resets, when regulators are powered on, some specific internal blocks of TRF6151.
[78] Vstep = 30mV; Vlow = 0.460 V

ANNEX 1: PLL_MODE

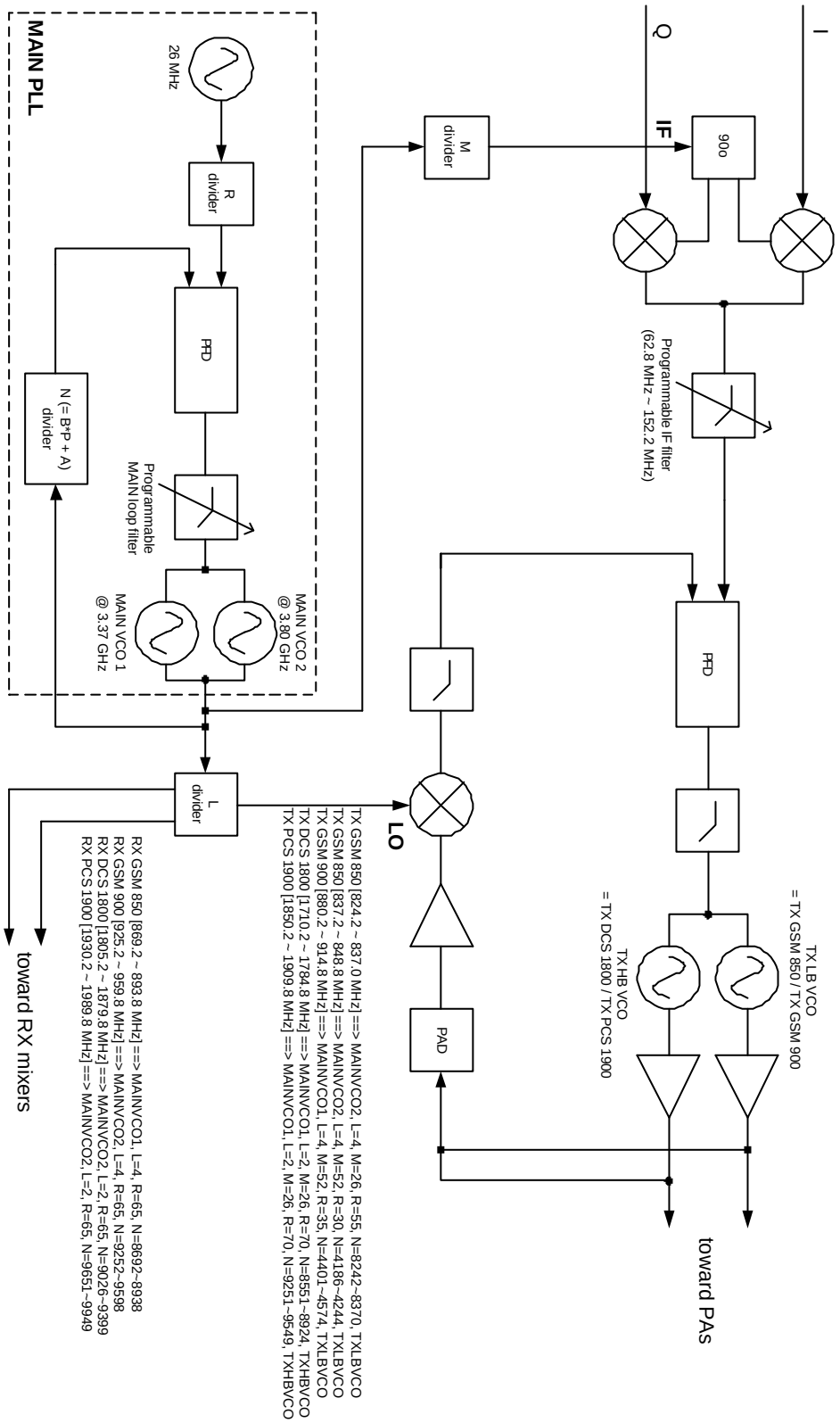


Figure 13 - Synthesizer block diagram

Four VCOs are used :

- a TX LB VCO [824.2 ~ 914.8 MHz] to generate the TX GSM 850 / TX GSM 900,
- a TX HB VCO [1710.2 ~ 1909.8 MHz] to generate the TX DCS 1800 / TX PCS 1900,
- a MAIN VCO 1 [3176.1 ~ 3575.2 MHz] (see below) to generate the RX GSM 850 / LO (and IF) for TX GSM 900, TX DCS 1800 and TX PCS 1900,
- a MAIN VCO 2 [3610.4 ~ 3979.6 MHz] (see below) to generate the RX GSM 900 / RX DCS 1800 / RX PCS 1900 / LO (and IF) for the two parts of TX GSM 850.

- MAIN VCO 1 at 3.37 GHz to generate in TX mode the LO (and IF) for GSM 900, DCS 1800 and PCS 1900 and also used to cover GSM 850 in RX mode :

Standard	RX band [MHz]	L divider	MAIN VCO range [MHz]
GSM 850	869.2 ~ 893.8	4	3476.80 ~ 3575.20
	TX band [MHz]	-	-
GSM 900	880.2 ~ 914.8	4	3269.31 ~ 3397.83
DCS 1800	1710.2 ~ 1784.8	2	3176.09 ~ 3314.63
PCS 1900	1850.2 ~ 1909.8	2	3436.09 ~ 3546.77
		TOTAL	3176.09 ~ 3575.20

➔ D**f = 399 MHz**

- MAIN VCO 2 at 3.80 GHz to cover GSM 900, DCS 1800 and PCS 1900 in RX mode and also used in TX mode to generate the LO (and IF) for the two parts of GSM 850 :

Standard	RX band [MHz]	L divider	MAIN VCO range [MHz]
GSM 900	925.2 ~ 959.8	4	3700.80 ~ 3839.20
DCS 1800	1805.2 ~ 1879.8	2	3610.40 ~ 3759.60
PCS 1900	1930.2 ~ 1989.8	2	3860.40 ~ 3979.60
	TX band [MHz]	-	-
First part of GSM 850	824.2 ~ 837.0	4	3896.22 ~ 3956.73
Second part of GSM 850	837.2 ~ 848.8	4	3627.87 ~ 3678.13
		TOTAL	3610.40 ~ 3979.60

➔ D**f = 370 MHz**

- MAIN PLL in RX mode : the reference frequency is 26.0 MHz

Standard	MAIN RX band [MHz]	R divider	Comparison frequency [kHz]	N range
GSM 850	3476.80 ~ 3575.20	65	400.0	8692 ~ 8938
GSM 900	3700.80 ~ 3839.20	65	400.0	9252 ~ 9598
DCS 1800	3610.40 ~ 3759.60	65	400.0	9026 ~ 9399
PCS 1900	3860.40 ~ 3979.60	65	400.0	9651 ~ 9949

The step frequency at the RX LO port is 100 kHz for GSM 850 / GSM 900 and 200 kHz for DCS 1800 / PCS 1900.

- LO / IF ranges in TX mode :

Standard	MAIN TX band [MHz]	L divider	LO range [MHz]	M divider	IF range [MHz]	RF
First part of GSM 850	3896.22 ~ 3956.73	4	974.06 ~ 989.18	26	149.85 ~ 152.18	LO – IF
Second part of GSM 850	3627.87 ~ 3678.13	4	906.97 ~ 919.53	52	69.77 ~ 70.73	LO – IF
GSM 900	3269.31 ~ 3397.83	4	817.33 ~ 849.46	52	62.87 ~ 65.34	LO + IF
DCS 1800	3176.09 ~ 3314.63	2	1588.04 ~ 1657.31	26	122.16 ~ 127.49	LO + IF
PCS 1900	3436.09 ~ 3546.77	2	1718.04 ~ 1773.38	26	132.16 ~ 136.41	LO + IF

➔ 3 different IF: IF1 = 66.8 MHz - Δf = 7.9 MHz
IF2 = 129.3 MHz - Δf = 14.3 MHz
IF3 = 151.0 MHz - Δf = 2.4 MHz

- MAIN PLL in TX mode : the reference frequency is 26.0 MHz

Standard	MAIN TX band [MHz]	R divider	Comparison frequency [kHz]	N range
First part of GSM 850	3896.22 ~ 3956.73	55	472.73	8242 ~ 8370
Second part of GSM 850	3627.87 ~ 3678.13	30	866.67	4186 ~ 4244
GSM 900	3269.31 ~ 3397.83	35	742.86	4401 ~ 4574
DCS 1800	3176.09 ~ 3314.63	70	371.43	8551 ~ 8924
PCS 1900	3436.09 ~ 3546.77	70	371.43	9251 ~ 9549

The step frequency at the RF output is 100 kHz for the first part of GSM 850 and 200 kHz for the second part of GSM 850 / GSM 900 / DCS 1800 / PCS 1900.

Synthesizer configuration according to REG_PWR register is:

Synthesizer mode	**P**	**L**	**M**	**R**	Main VCO
OFF	-	-	-	-	OFF
TX High band	64	2	26	70	Main VCO 1
TX GSM900	64	4	52	35	Main VCO 1
TX GSM850_low	64	4	26	55	Main VCO 2
TX GSM850_high	64	4	52	30	Main VCO 2
RX_GSM850	64	4	-	65	Main VCO 1
RX GSM900	64	4	-	65	Main VCO 2
RX high band	64	2	-	65	Main VCO 2

Synthesizer mode	IF filter	TX VCO	Main PLL charge pump current	Main PLL filter settings
OFF	OFF	OFF	tbd	tbd
TX High band	IF2	TXHBVCO	tbd	tbd
TX GSM900	IF1	TXLBVCO	tbd	tbd
TX GSM850_low	IF3	TXLBVCO	tbd	tbd
TX GSM850_high	IF1	TXLBVCO	tbd	tbd
RX_GSM850	-	-	tbd	tbd
RX GSM900	-	-	tbd	tbd
RX high band	-	-	tbd	tbd

When SYNTHE_MODE =’00’ to ‘01’ or ‘10’, synthesizer is powered up according to the settings defined in the table above. Main VCO and TX VCO calibration processes are activated.

ANNEX 2: FRONT END MEASUREMENT SCHEMATIC

To measure front-end characteristics, considering its 100 ohms input, following schematic is proposed:

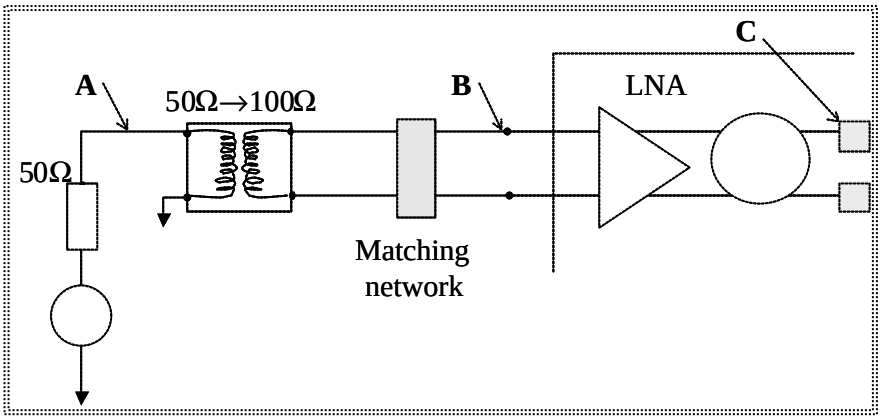


Figure 14 - RX RF gain definition

For the 50 to 100 Ω balun, following components can be used:

- Murata LDB20C101A0900
  Unbalance Impedance: 50 ohm
  Balance Impedance (Differential): 100 ohm
  Frequency range: 900 ± 100 MHz band
  Maximum insertion loss: 0.8dB (25°C); 0.9dB max. (-25~+85°C)
- Murata LDB20C101A1900
  Unbalance Impedance: 50 ohm
  Balance Impedance (Differential): 100 ohm
  Frequency range: 1900 ± 100 MHz band
  Maximum insertion loss: 0.8dB (25°C); 0.9dB max. (-25~+85°C)

All front-end data are specified and should be measured with:

- input point = A
- output point = C (internal pads or test outputs)
- Balun losses have to be removed from measurement. They are not included in specification.
- Matching network must be built with standard capacitors and "LQG series" inductors. Its losses must be included in receiver noise figure.

Recommended Matching network structure is the following: C1+C2+L or C3+C4+L.

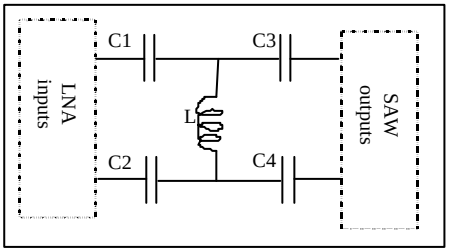


Figure 15 - Recommended matching network

ANNEX 3: TRF6151 RECEIVER CONFIGURATIONS

European dual band configuration:

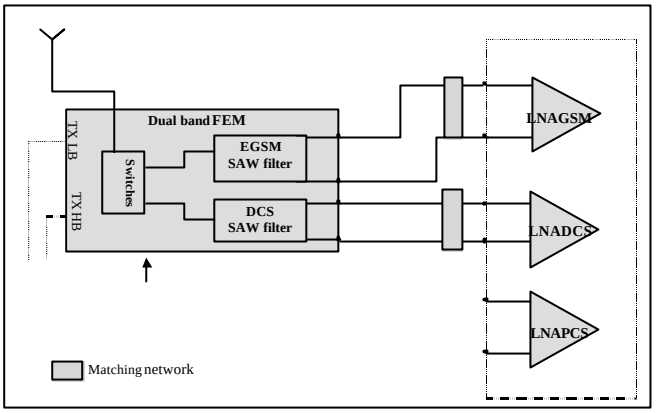


Figure 16 - European dual band RX block diagram

US dual band configuration:

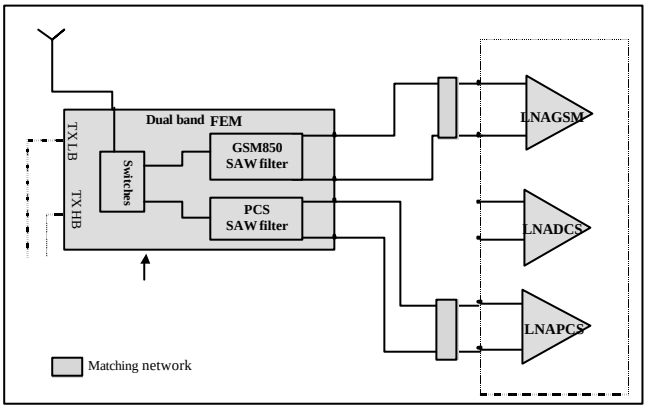


Figure 17 - US dual band RX block diagram

"European triple band" configuration:

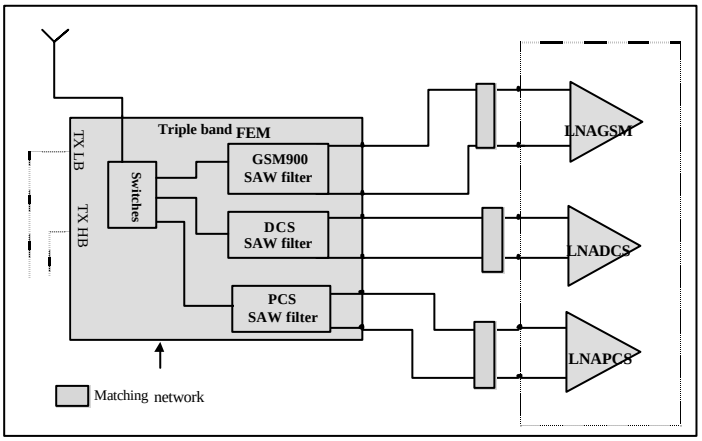


Figure 18 - European triple band RX block diagram

"US triple band" configuration:

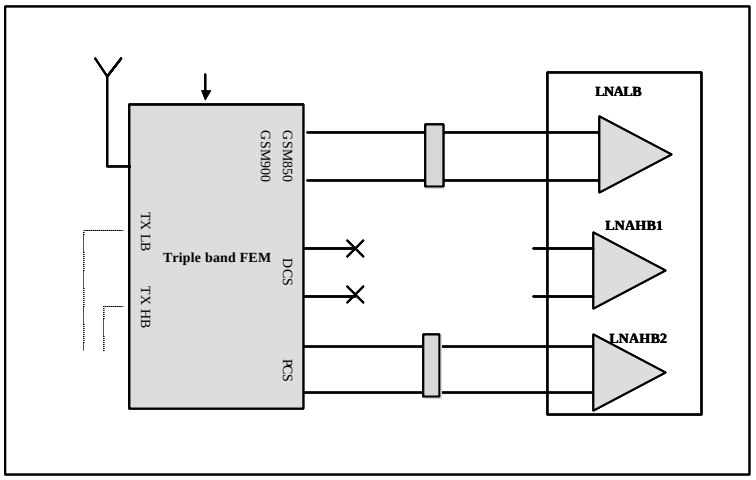
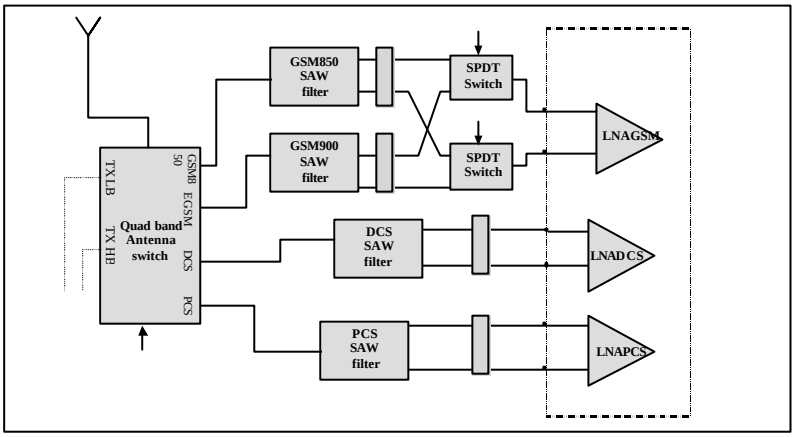


Figure 19 - US triple band RX block diagram

"Quad band" configuration:



Or…

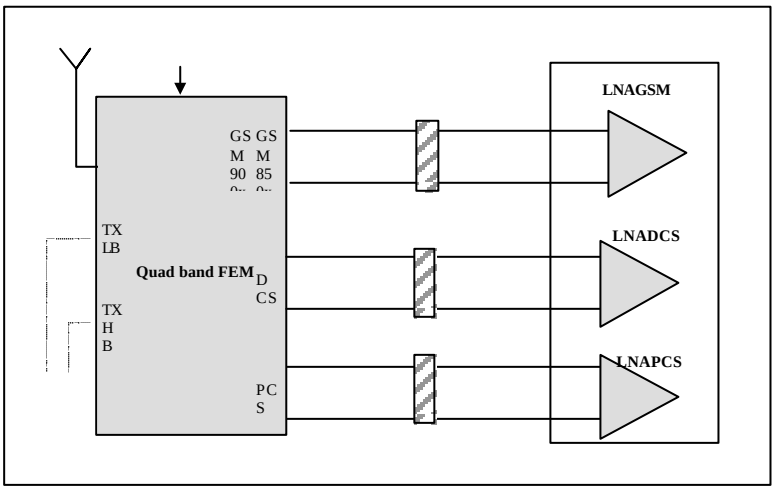


Figure 20 - Quad band RX block diagram

ANNEX 4: TRF6151 FILTERS

Cascaded filters:

Following plots are showing the attenuation characteristics of the 3-cascaded low pass filters included in TRF6151.

Worst-case curves are “cascaded worst case” on all filters (cut-off-frequencies are maximal).

Best-case curves are also “cascaded best case” on all filters (cut-off-frequencies are minimal).

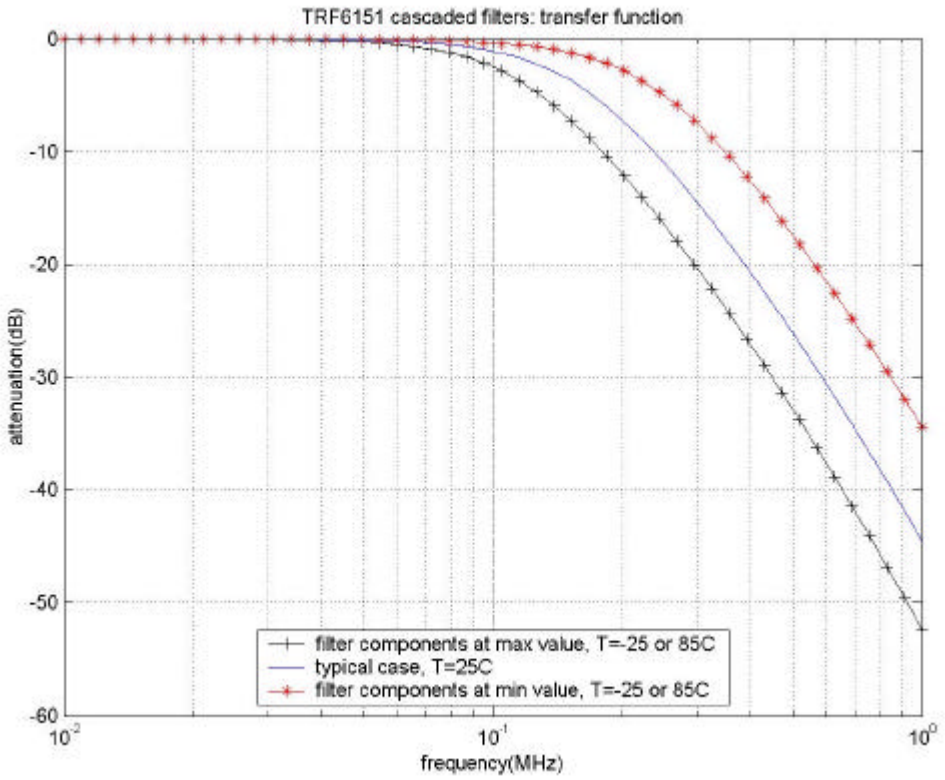


Figure 21 - TRF6151 cascaded filters characteristic

Post IQ demodulator filter:

Parameters	Test conditions	Min.	Typ.	Max.	Unit
Filter order			1		-
Filter cut off frequency		275	338	438	kHz
Filter attenuation	f=330kHz	2	2.9	3.9	dB
	f=600kHz	4.6	6.2	7.6	dB
	f=800kHz	6.4	8.2	9.8	dB
	f=1.6MHz	11.6	13.7	15.4	dB
	f=3MHz	16.8	19	20.8	dB
	f=10MHz	27.2	29.4	31.2	dB
	f=20MHz	33.2	35.4	37.2	dB

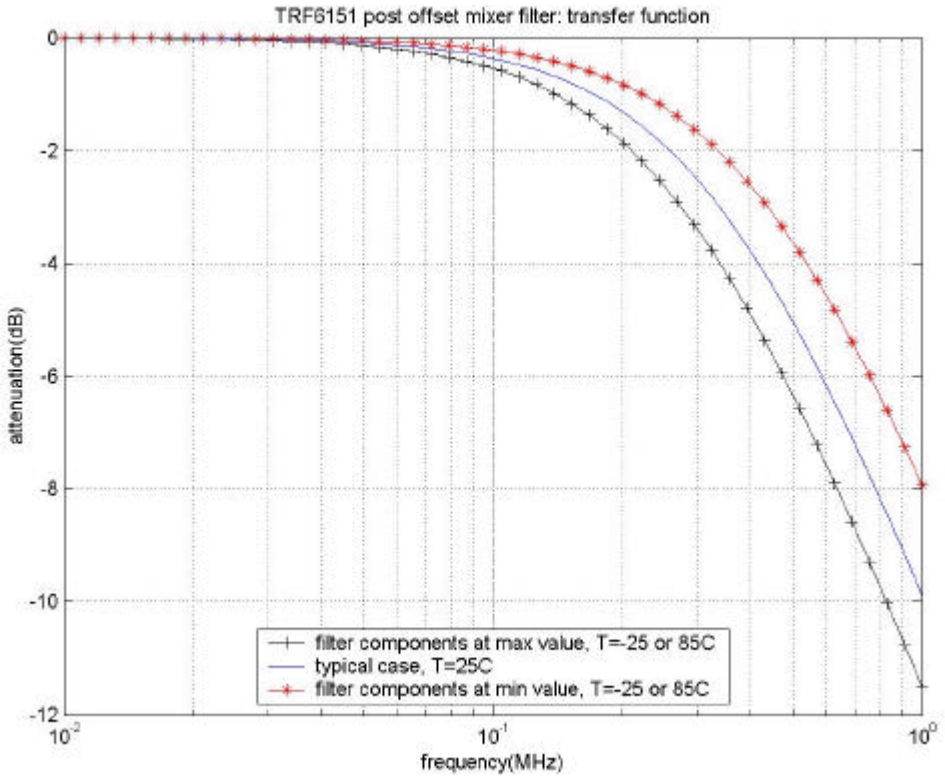


Figure 22 - TRF6151 post mixer filter characteristic

VGA low pass filters:

Parameters	Test conditions	Min.	Typ.	Max.	Unit
VGA low pass filter #1	Order		1		
	3dB cut-off-frequency	0.9	1.2	1.8	MHz
VGA low pass filter #2	Order		2		
	Type		Butterworth		
	3dB cut-off-frequency	120	155	230	kHz
VGA Filters global attenuation[79]	f=330kHz	7.2	13.7	18.8	dB
	f=600kHz	17	24.5	30.1	dB
	f=800kHz	22.1	30.1	36.1	dB
	f=1.6MHz	36	45	51.8	dB
	f=3MHz	50.2	60.1	67.3	dB
	f=10MHz	80.3	60.9	98.4	dB
	f=20MHz	98.3	108.9	116.4	dB

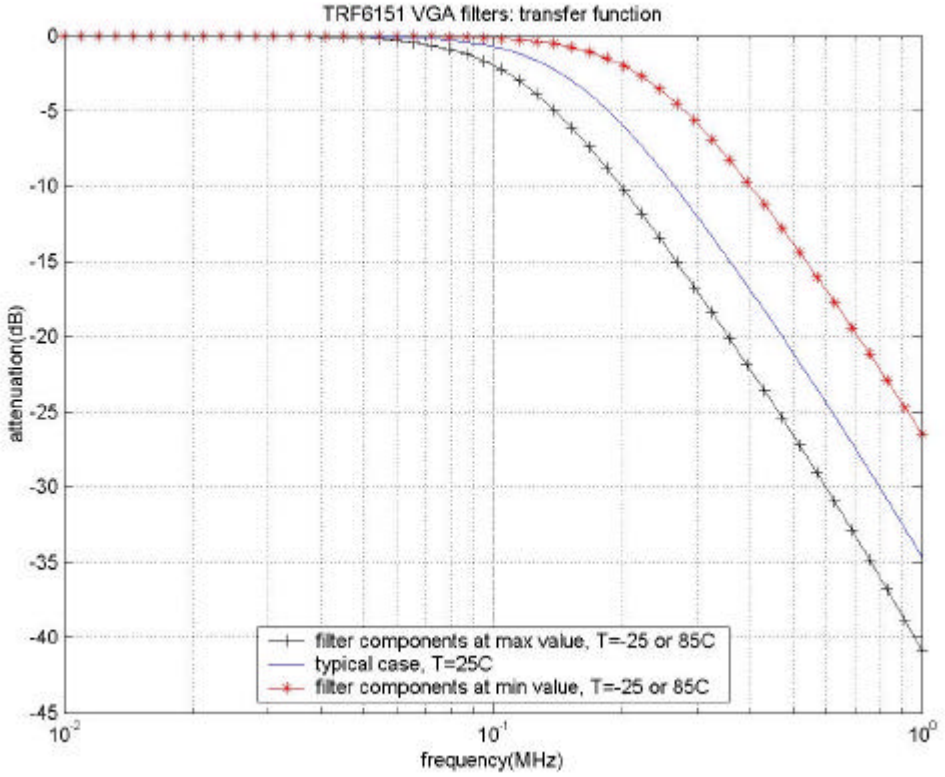


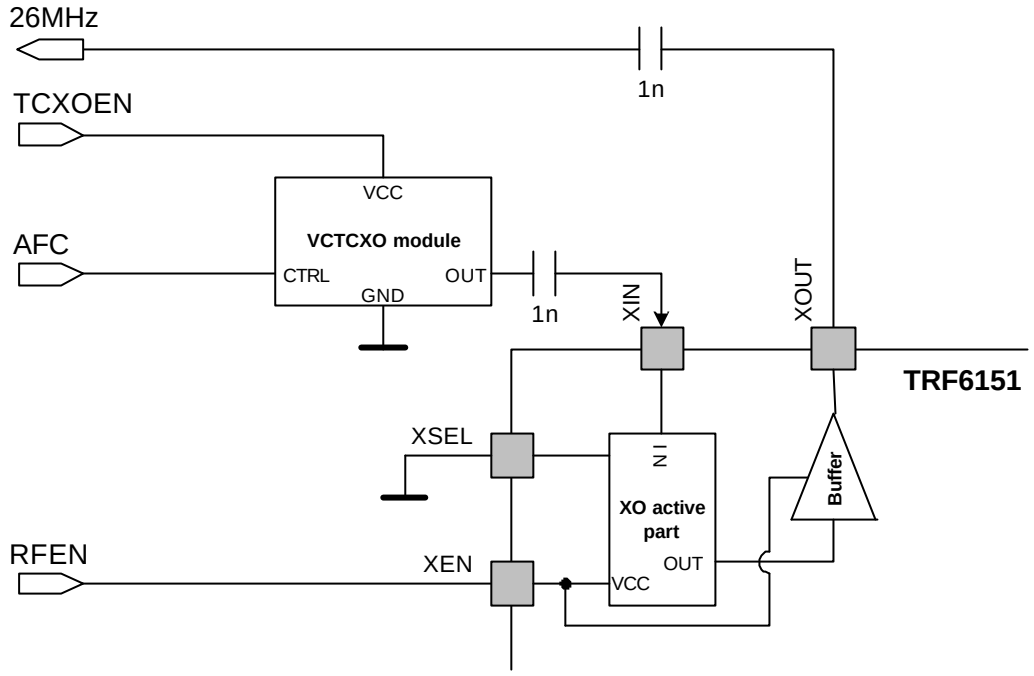
Figure 23 - TRF6151 base band filters characteristic

[79] Filters included in VGA are cascaded (1rst order low pass filter with cut-off-frequency at 1.2MHz + 2nd order Butterworth low pass filter with cut-off-frequency at 155 kHz)

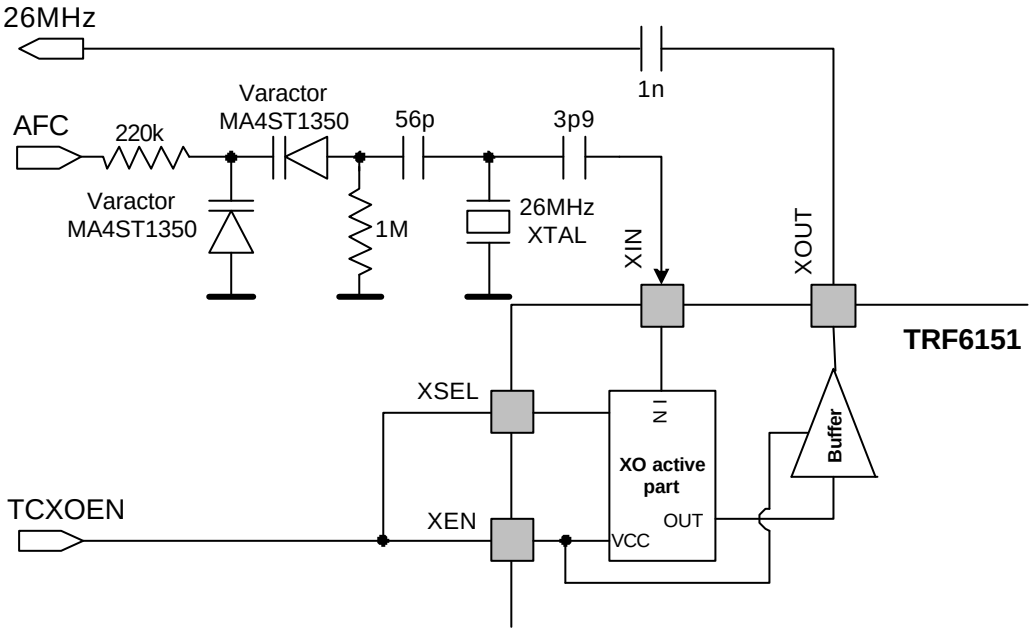
ANNEX 5: INPUT 1DB BLOCKING COMPRESSION POINT TABLE

Input 1dB blocking compression point	Voltage gain=G1 All bands Blocker @ 0.33 Mhz from carrier		-48	-44.5	-	dBm
	Voltage gain=G2 All bands Blocker @ 0.33 Mhz from carrier		-42	-38.5	-	dBm
	Voltage gain=G1 All bands Blocker @ 0.6 Mhz from carrier		-47.5	-43	-	dBm
	Voltage gain=G2 All bands Blocker @ 0.6 Mhz from carrier		-41.5	-37.5	-	dBm
	Voltage gain=G1 All bands Blocker @ 1.6 Mhz from carrier		-37	-33	-	dBm
	Voltage gain=G2 All bands Blocker @ 1.6 Mhz from carrier		-33	-30.5	-	dBm
	Voltage gain=G1 GSM850 and GSM900 bands Blocker @ 3 Mhz from carrier		-30	-28	-	dBm
	Voltage gain=G1,G2 DCS1800 and PCS1900 bands Blocker @ 3 Mhz from carrier		-32	-30.5	-	dBm
	Voltage gain=G2 GSM850 and GSM900 bands Blocker @ 3 Mhz from carrier		-28.5	-27	-	dBm
	Voltage gain=G1,G2 GSM900 band Blocker @ 10 Mhz from carrier		-28	-27	-	dBm
	Voltage gain=G1,G2 GSM850 band Blocker @ 20 Mhz from carrier		-25	-24	-	dBm
	Voltage gain=G1,G2 GSM900 band Blocker @ 20 Mhz from carrier		-26	-25	-	dBm
	Voltage gain=G1,G2 DCS1800 band Blocker @ 20 Mhz from carrier		-30	-29	-	dBm
	Voltage gain=G1,G2 PCS1900 band Blocker @ 20 Mhz from carrier		-26	-25	-	dBm
	Voltage gain=G1,G2 DCS1800 band Blocker @ 100 Mhz from carrier		-26	-25	-	dBm

ANNEX 6: REFERENCE CLOCK CONNECTION[80]



EXTERNAL VCTCXO



INTERNAL VCXO

Figure 24 – Reference clock connection

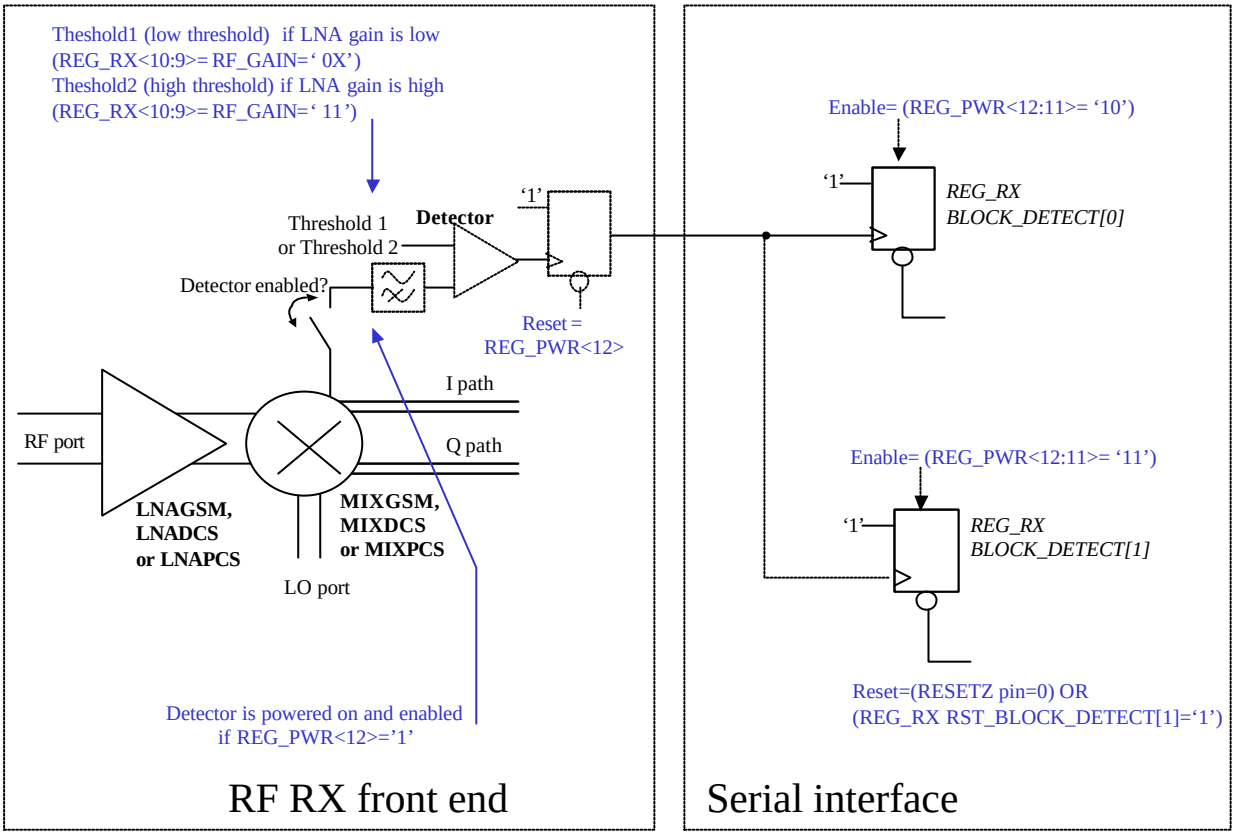
[80] The components values are given only for indication – They come from EVARITA application board

ANNEX 7: INTERFERER DETECTION SYSTEM

Principle

Today, the AGC strategy is only based on the useful signal input power level and quality. We propose also to inform the DBB when a large interferer appears at the TRF6151 input, during a RX session.

Block diagram



Detection process

The DBB can use the serial interface to start an RX session with the "interferer detector enabled". Then, the receiver is switched on with a detector system at the mixer output, which sets a control bit to 1 if a large signal is present at the mixer output. This detector includes 2 thresholds, automatically switched according the RF gain setting. If LNA-mixer gain is high, high threshold is used; otherwise, low threshold is used.

The control bit is stored in one bit of the serial interface registers, with two possible storing addresses: REG_RX<4> or REG_RX<3>. The DBB selects alternatively each address to ensure the double buffering of the detector output. This is necessary for the L1 software.

At the end of the RX session, DBB reads REG_RX contents and reset REG_RX<4:3> before the next RX session. For that purpose, following TPU scenario is recommended:

#	Programming	Explanations
1	Set DBB REG_SPI_CTRL2 = '1'	DBB serial port is in RX/TX mode
2	Word #1 'XXXXXXX0100XX000'	Word #1 means that during the next serial interface programming, REG_RX register content will be serialized on SIOUT pin.
3	Word #2 'XXXXXXX0011XX000'	During Word #2 reception, REG_RX register content is received by the DBB. Word#2 means that during the next serial interface programming, no data will be serialized on SIOUT pin and that BLOCK_DETECT contents is reset.
4	Set DBB REG_SPI_CTRL2 = '0'	DBB serial port is in TX mode only. (BLOCK_DETECT is now stored in REG_RX_LSB [4:3])

Finally, according detection results, DBB can decide to reduce the RF gain to limit dynamic DC offset due to the presence of powerful interferer at the antenna.

ANNEX 8: TEST PROCEDURE FOR RX LOCK TIME

Test #1: locking time from "OFF" to "RX" state

Test procedure:

1. TRF6151 is in idle mode, only the bandgap and the regulators are ON,
2. Set the LNA in high gain, and VGA in low gain. RX DC offset compensation is not required,
3. A sinewave signal @ freq = F_1+68kHz is applied at receiver input,
4. At t=t_0, entire receiver is switched on (RX synthesizer + RX path),
5. 68kHz signal is observed at IQ P/N outputs of TRF6151. The receiver lock time is $t_L=t_1-t_0$, where t_1 is the time when frequency error is within 20 Hz averaged over 1 burst time.

Test signal settings for lock time measurement:
Test signal power level at antenna = -50dBm
Test signal frequency at antenna = F_1+68kHz (see table below for F_1 value)

Band	Frequency F_1 (MHz)	Receiver input port
GSM 850	869.2	LNAGSM
	881.6	
	893.8	
GSM 900	925.2	LNAGSM
	942.6	
	959.8	
DCS 1800	1805.2	LNADCS
	1842.6	
	1879.8	
PCS 1900	1930.2	LNAPCS
	1960.0	
	1979.8	

TRF6151 Programming sequence example (RX EGSM @925.2MHz):

Task #	Action	Programming	Timing
#1	TRF6151 is in idle mode, only the bandgap and the regulators are ON	REG_PWR<15:0>= 0000000XXX111010	Wait at least 25msec before #2
#2	Set PLL channel RX EGSM = 925.2MHz with A=36 B=144 freq = (144*64+36)/(65*4)*26	REG_PLL<15:0>= 1010000100100001	before #3
#3	Set LNA gain = high, VGA gain = low	REG_RX<15:0>= 00110XX0011XX000	before #4
#4	Set RX band (EGSM), power on synthesizer, and RX path. After 175usec, Main VCO is calibrated and main PLL should be locked	REG_PWR<15:0>= 000010100X111010	t_0
#5	Measure signal on VGA IQ output with frequency error<= 20Hz over 1 burst	-	t_1

Test #2: locking time from "RX GSM" to "RX DCS" state

Test procedure:

1. A sinewave signal @ freq = F_1+68kHz is applied at receiver input,
2. TRF6151 is in RX GSM mode,
3. Stop TRF6151 RX GSM session,
4. Set PLL for RX DCS session,
5. At $t=t_0$, entire receiver is switched on (RX synthesizer + RX path) in DCS mode,
6. 68kHz signal is observed at IQ P/N outputs of TRF6151. The receiver lock time is $t_L=t_1-t_0$, where t_1 is the time when frequency error is within 20 Hz averaged over 1 burst time.

Test signal settings for lock time measurement:
Test signal power level at antenna = -50dBm
Test signal frequency at antenna = F_1+68kHz (see table below for F_1 value)

Band	Frequency F_1 (MHz)	Receiver input port
DCS 1800	1805.2	LNADCS
	1842.6	
	1879.8	

TRF6151 Programming sequence example:

From EGSM RX=925.2MHz to DCS RX=1879.8MHz

Task #	Action	Programming	Timing
#1	TRF6151 is in RX GSM mode with freq = 925.2MHz	REG_PLL<15:0>= 1010000100100001 REG_RX<15:0>= 00110XX0011XX000 REG_PWR<15:0>= 000010100X111010	Wait at least 25msec before #2
#2	Stop RX GSM session, set TRF6151 is in idle mode, only the bandgap and the regulators are still maintained ON.	REG_PWR<15:0>= 0000000XXX111010	Before #3
#3	Set PLL channel RX DCS = 1879.8MHz with A=55 B=146 freq = (146*64+55)/(65*2)*26	REG_PLL<15:0>= 1010010110111001	before #4
#4	Set RX band (DCS), power on synthesizer, and RX path. After 175usec, Main VCO is calibrated and main PLL should be locked	REG_PWR<15:0>= 000010101X111010	t_0
#5	Measure signal on VGA IQ output with frequency error<= 20Hz over 1 burst	-	t_1