Schematic sanity checks for Calypso/Iota based PCBs

APN06
Ver 1.0

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Department: EWTBU

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HISTORY

Version	Date	Author	Notes
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Ver: 2.0			2
Ver: 3.0			3
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NOTES :

1. Creation
2. ……..
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GLOSSARY

REFERENCE DOCUMENTS

APN0 ver 1.1

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1 Introduction

The intent of this document is to regroup all checks and TI recommendations regarding design of Calypso/Iota/Clara based PCBs

2 Iota

The following recommendations list is divided into three parts, Mandatory connections, Recommended connections and Warnings.

2.1 Mandatory connections

- RPWON and PWON signals use internal pull up (10 uA) on the VBAT power domain. If external pull up should be used (long connections) this must be on VBAT and not on UPR pins.
- Ibias resistor must be 100K +/- 1%
- VFS,VCK,VDR,VDX signal have to be loaded with the same wire load.
- GND1 to GND2, LEDB1 to LEDB2, VRIO1 to VRIO2 must be respectively connected externally
- All ground signals GNDL, GNDD, GNDAV, GNDA, must be connected externally to the ground plane. They are not internally connected.
- No current has to be driven out to VRRTC power domain. I/O's supplied on this power domain (ON_nOFF, IT_WAKEUP, nRESPWONZ, CLK32K) must not be loaded.
- Minimize capacitive load on nTESTRESTZ pin
- Place a 100k pull down on Iota UDX pin

2.2 Recommended connections

- Place an external 100k pull up to UPR on nTESTRSTZ pin.
- Some 4 wires RF chips may require a filter on I/Q signals as illustrated in the schematic below

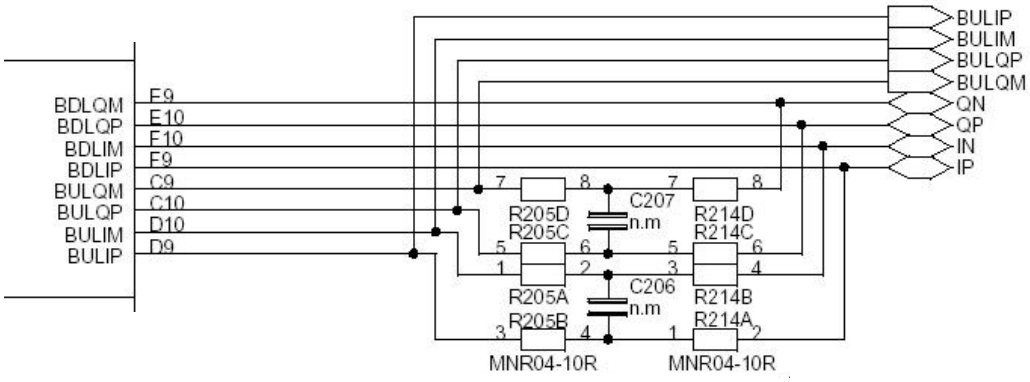

Figure 1 I/Q T filter connections

- Foresee for debug purposes following test point on the signals:

  nTESTRSTZ
  ON_nOFF
  nRESPWONZ
  INT1
  INT2
  UDX
  UDR
  UEN
  CLK13M
  IT_WAKEUP
  BFSX
  BDX
  BDR

- **Foresee pull up to UPR and pull down to GND for both VLRTC & VLMEM signals, this will provide PCB compatibility to Calypso c05 and c035.**
- Refer to Iota datasheet to check the test port pin state (TDO,TD,TMS,TCLK).

2.3 Warnings

- Double-check VRRTC, VBAKUP, VRRAM and UPR connections. Tricky connections (diodes other stuff must be reported to application/Validation group to be approved)
- Check consistency of LDO's capacitor values with the specification
- Report to Application group any not standard connection on the VRRTC power domain.
- Adopt the D-Sample schematic as reference.

3 Calypso

Many of useful information's regarding Iota to Calypso interconnect are indicated in APN0 ver 1.1 please refer to this application note also.

3.1 CALYPSO DPLL PCB LAYOUT RECOMMENDATIONS

3.1.1 Purpose:

The objective of this document is to provide to application engineers, PCB recommendations to be applied to optimize performances of the Calypso DPLL oscillator. Some of the recommendations are generic and can be applied in any case but others are more specific to Calypso device.

3.1.2 Power supply distribution

DPLLs are generally sensitive to power supply noise bump or power supply ripple. Important noise in the power supply or voltage change may affect the jitter performances and may cause problem of frequency lock. For these reasons, care has to be taken to the quality of power supply to be applied and to the way the PCB is routed.

3.1.3 Vdd layout considerations

The best practice to obtain good performances is to power the DPLL module separately or to share a low current power supply. In the Calypso Chip Set application the supply of the DPLL is supported by the same LDO as for the supply of the CORE.
In general , VDD_PLL must not be connected to the peripheral power supply due to the important voltage drops which may occur in this specific power supply.
Traces on the PCB that supply the VDD core and the VDD_PLL have to be routed and filtered separately to avoid any noise or drop voltage due to logic core switching to degrade the PLL performances
Typical VDD routing are shown on the figure (1 an 2). Figure (1) represents a bad layout The result of routing in series the power supply line from the LDO is a coupling of noise and voltage drop to VDD_PLL. Figure(2) represents a better layout in with the transitions of switching current through VDD have been isolated from PLL power supply.
To be efficient , the filtering capacitor C1 has to be placed as close as possible to VDD pin with connections as short as possible

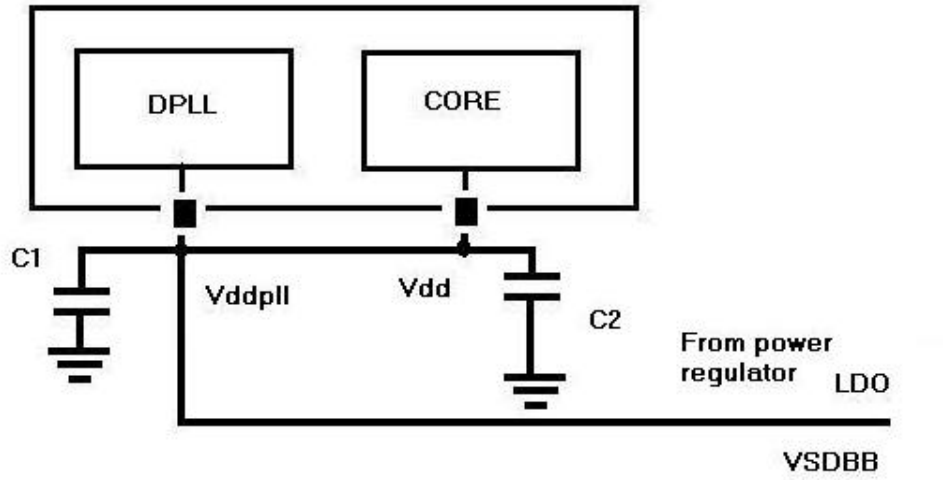

Figure 2 Bad layout (noise coupling between Vdd and Vddpll)

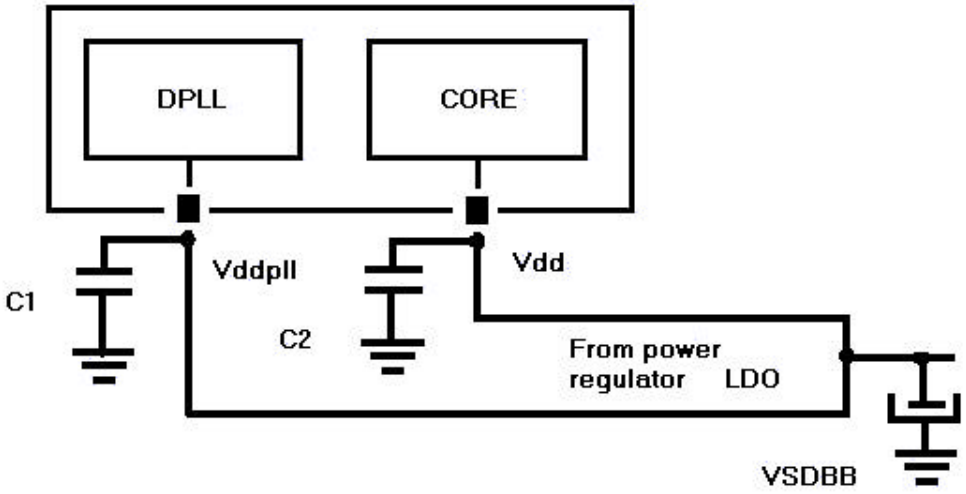

Figure 3 Good layout (Power line routed in star mode)

3.1.4 Grounding path

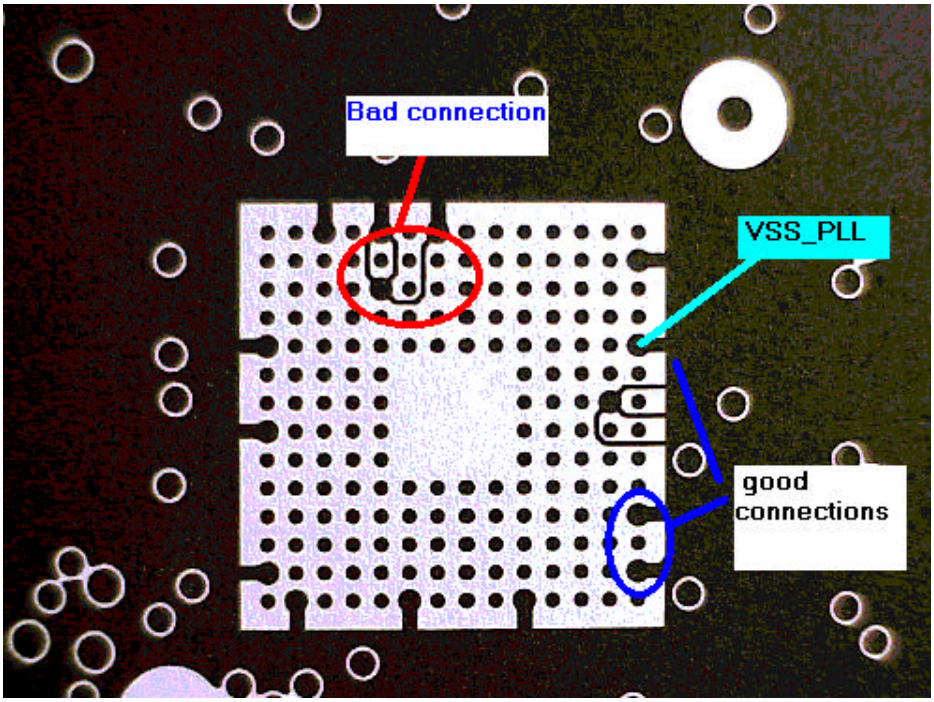

Figure 4 Vss balls assignment and PCB ground layer

UBGA package does not provide capability to build under the device good ground plan. For this reason to minimize ground coupling effect or common mode effect, all the ground connections, on calypso have been placed to the ball close to the package side so these connections to the PCB ground plan can be done with very short length. It is particularly true for the ground reference of the DPLL, VSS_PLL (ball E14). The VSS ball has to be routed on the PCB directly to the ground reference plan avoiding to cross under the package or circling other balls.

3.1.5 PACKAGE CONSIDERATION

For better filtering efficiency, on calypso package the DPLL module is located close to the package side and close to the power supply connection.
As seen on previous chapter, the ground pin is located close to the package side to be directly connected to the ground plan.
For the power line, connection is also located to a ball close the package side. The PLL module power supply is completely isolated, VSS being separated from the general ground ring on the die.
The best performance is obtained when the filtering capacitor is placed close to the PLL package side with connections as short as possible.

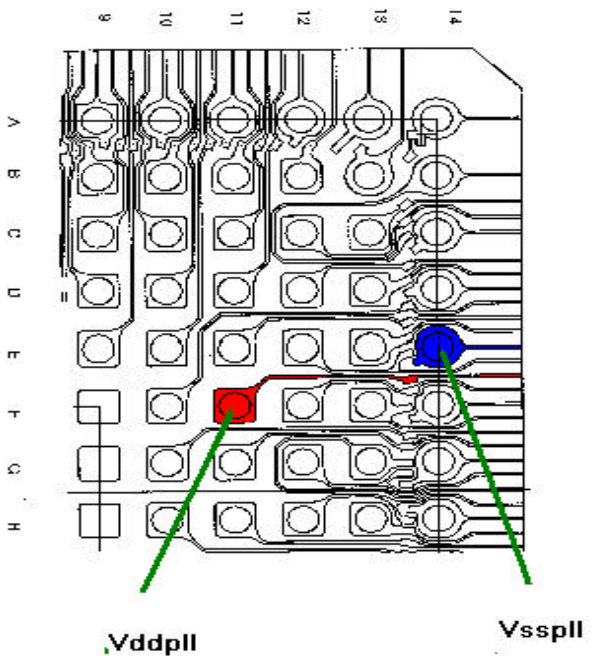

Figure 5 DPLL VDD/Vss ball connections

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3.1.6 PCB layout recommendations summary

1. Use separate VDD supply to power the DPLL oscillator if possible.
2. If the DPLL cannot powered by an isolated power supply, share DPLL power supply with low current, low noise power supply. VDD core not VI/O.
3. Place filtering ceramic capacitor close to the DPLL package side and close to DPLL pins with connection as short as possible.
4. Connect DPLL GND pin directly to the ground plan trough connection as short as possible.
5. When sharing an other power supply, route the different power line separately in star mode avoiding to make large loop circling critical signals.
6. Check APN0 for more details on 32Khz clock application schematic and LDO decoupling recommendations.