# **Iota SIM card Interface**

# APN04 Ver 1.0

# File: G:\lota\Application Notes\APN4.doc

## Department: EWTBU

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## HISTORY

Version	Date	Author	Notes
Ver: 1.0	04/02/02	Lorenzo Indiani	1
Ver: 2.0			2
Ver: 3.0			3
Ver: 4.0			4

### NOTES :

- 1. Creation
- 2. .....
- 3. .....

4.

GLOSSARY

REFERENCE DOCUMENTS

[1] APN0	Calypso/lota/Clara System application note	ver 1.1
[2] CAL207	Calypso register mapping	ver 0.8
[3] TWL3014	lota specification	ver 2.0



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### 1 The lota SIM card interface

The lota SIM interface is composed by a dedicated LDO and I/O level shifters. It is able to support 3V and 1.8V SIM cards.



1.1 Iota SIM card interface – Block schematic

### 1.1 The VRPCSIM control register

SIM card interface is controlled through the VRPCSIM lota register at address 23 Page 1.

Name	:VRPCS	IM De	escriptio	n: SIM	CARD	Contro	I Regis	ter			Addre	ess: 23	Page	: 1	R/W
-	-	-	-	-	-	SIMLEN	SIMRSU	RSIMEN	SIMSEL	1	0	1	1	1	1/0
R	R	R	R	R	R	R/W	R	R/W	R/W		< A	CCESS TY	'PE		
0	0	0	0	0	0	0	0	0	0		< V	ALUE AT	RESET		
01140			0 1 1												

SINSEL	•	Select VRSIN output voltage
		'1' => 2.9 V '0' => 1.8V
RSIMEN	:	Enable the RSIM regulator
SIMRSU	:	VRSIM regulation status
		'1' => regulation is ON, the SIM interface is correctly supplied
		'0' => the regulator is not yet in regulation mode
SIMLEN	:	Enable the SIM interface level shifter ( SIMCK, SIMIO, SIMRST are enable )

The VRPC state machine does not automatically enable SIM LDO at start up, its enable has to be done in the SIM initialization routine.

A particular enable sequence must be respected in order to grant a proper initialization of the interface.



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#### 1.2 The SIM interface enable sequence

As the SIM LDO is not enabled care should be paid to level shifter enable respect the presence of the SIM power supply. For that reason correct enabling sequence is the following:

- 1. Selection of the SIM voltage and enable of the SIM LDO( SIMSEL and SIMEN bits).
- 2. Wait for the SIM LDO output voltage set up (SIMRSU bit).
- 3. Enable SIM level shifter when SIMRSU = 1 (SIMLEN bit).

Assuming a 3V SIM to be driven this could be the flow diagram of the interface enabling SW.



1.2 SIM enabling flowchart

The  $T_{SIMSU}$  parameter is related to the SIM LDO setup time. Typical value for LDO set up time is less than 4 ms.



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### 2 Selection of the pull up resistor for the SIM interface

Selection of pull -up resistor is trade-off between the SIM IO rising time and current consumption. Indeed, during the transmission of a low state from the SIM card to the DBB or from the DBB to the SIM card, the current consumption of the I/O interface is VRIO/R + VRSIM/R.

Relation between the rising time and the pull-up resistor could be evaluated considering the I/O rising time as  $t_r = t_2 - t_1$ 



Where

$$90\%V_0 = V_0 (1 - e^{-t2/\tau}) \Longrightarrow t_2 = -\tau \ln (0.1)$$
$$10\%V_0 = V_0 (1 - e^{-t1/\tau}) \Longrightarrow t_1 = -\tau \ln (0.9)$$

$$t_r = t_2 - t_1 = t [ln (0.9) - ln (0.1)] = 2.19 t$$

with  $\tau = RC$ ,

C is the output capacitance and R is the pull-up restor.

So, if  $C_{max} = 70pF$  and  $t_{rmax} = 1us \Rightarrow R_{max} = 6.52kohms$  or if

 $C_{max}$  = 30pF and  $t_{rmax}$  = 1us => R  $_{max}$  = 15.2 kohms

Rise time and load capacitance constraints for each interface signal are described in APN0 [1] please check paragraph 7.1.1 page 42.



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### 3 Interface configuration during off and sleep modes

#### 3.1 OFF Mode

When SIMLEN is low, level shifters are disabled, SIMIO is driven to a low logical state. In that case VRSIM is connected to ground via the pull-up resistance.

### 3.2 Sleep Mode

During sleep mode the SIM interface assumes the following configuration:

Iota VRRSIM enabled Iota level shifters enabled Calypso SIM\_RST signal at the inactive level (logic one) Calypso SIM\_CLK freeze at high or low level ( depending on SIM card) Calypso SIM\_IO in input mode (Pulled up at high logical level through Rpu) Calypso SIM\_PWCTRL at high logical level.

In this configuration Sleep consumption of the SIM interface is mainly related to the SIM card leakage current.



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