APN02

Current consumption of Calypso/Iota based chipset in idle modes
Ver 1.1

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Department: EWTBU

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HISTORY

Version	Date	Author	Notes
Ver: 1.0		Lorenzo Indiani	1
Ver: 1.1	1/9/02		2
Ver: 3.0			3
Ver: 4.0			4

NOTES :

1. Creation
2. Modification of switch off sequence
3. ……..
4.

GLOSSARY

MB Main Battery
BB Back Up Battery
DRX9 Indicates the periods of paging block decode activity, in this case period is 9*51*4.615ms where 51 is the number of GSM frames(4.615ms) included in a multitrame.

REFERENCE DOCUMENTS

[1] APN0 Calypso/Iota/Clara System application note ver 1.2
[2] CAL207 Calypso register mapping ver 0.8
[3] TWL3014 Iota specification ver 2.0

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1 The Emi-Conso bench environment

The Emi-Conso board is a development tool adopted to evaluate mainly Electro Magnetic Interference of the baseband part of chipset and system current consumption.

This evaluation board includes:

- Calypso digital baseband revision B
- Iota analog baseband revision 2.0
- Connectors for bus visibility and UART modem link
- RF connector compatible wit C sample RF connector and with I/Q expansion board.
- JTAG connector for emulation purposes
- 32Mbit external flash and 4Mbit external SRAM in a combo device.

The evaluation board memory mapping is C sample compatible.

This bench has been adopted to develop and integrate to L1 the new Iota power management functionalities.

Verification of the power consumption improvement features has been done measuring idle period current consumption and system baseband part current consumption running completes GSM paging scenarios in I/Q mode.

2 Current consumption measurements in Backup mode

Following tables summarize the system current consumption in Backup mode. System is in back up either with both batteries or just with the BB inserted. Measurements below take in account those two cases at room temperature. RTC functionality was monitored during all tests to verify system integrity.

2.1 System without Main battery

Assumptions:
Main Battery voltage = floating
Back up voltage = 2.8V
RTC_RES_REG = 0x27 (default value)

	Current Consumption from BB(µ A)
Iota	3
VRRTC regulator & POR logic	
MB vs BB comparator	
Calypso	9.5
RTC & Power Split Logic	
XO32K	
XO32K IO	
Clara	-
None	
Total	**12.5**

Assumptions:
Main Battery voltage = floating
Back up voltage = 2.8V
RTC_RES_REG = 0x20 (max value of XO32K bias resistor)

	Current Consumption from BB(µ A)
Iota	3
VRRTC regulator & POR logic	
MB vs BB comparator	
Calypso	2.8
RTC & Power Split Logic	
XO32K	
XO32K IO	
Clara	
None	-
Total	**5.8**

2.2 System with main battery

Assumptions:

Main Battery voltage = 3.8V
Back Up battery voltage = 2.8V
RTC_RES_REG = 0x27 (max value of XO32K bias resistor)
Charge of Back Up Battery disabled

	Current Consumption from MB (µ A)
Iota	14.5
VRRTC regulator & POR logic	
MB vs BB comparator	
Band Gap	
Calypso	9.5
RTC & Power Split Logic	
XO32K	
XO32K IO	
Clara	
None	
Total	**24**

Assumptions:

Main Battery voltage = 3.8V
Back Up battery voltage = 2.8V
RTC_RES_REG = 0x20 (max value of XO32K bias resistor)
Charge of Back Up Battery disabled

	Current Consumption from MB (µ A)
Iota	14.2
VRRTC regulator & POR logic	
MB vs BB comparator	
Band Gap	
Calypso	2.8
RTC & Power Split Logic	
XO32K	
XO32K IO	
Clara	
None	
Total	**17**

3 Current consumption measurements in paging modes

3.1 How L1 manages active to sleep transitions

L1 SW has been modified in three main sections in order to achieve power consumption optimization using Iota device:
ABB static configuration
ABB dynamic configuration entering L1 deep sleep mode
ABB dynamic configuration exiting the L1 deep sleep mode

Paragraph below will describe those modifications:

3.2 Configuring Iota Sleep parameters

This configuration is usually done once at system initialization and consists in the selection of the Sleep delay interval and of the LDO's sleep configuration.

The sleep delay is the time interval imposed by the Iota VRPC state machine between the reception of the DEVSLP command and the effective configuration of Iota LDO in sleep mode.
This delay has been introduced to let the L1 SW be able to cut properly all system current consumptions before Iota LDO's pass to the limited current drive capability that characterize the sleep mode.
Referring to Figure 4-2 this time interval correspond to the period in which Iota LDO's are still active while system is already in deep sleep.
Sleep delay is configured through the VRPCCFG register address 30 page 1 [3]

The LDO's sleep configuration allows the selection of the state of the voltage regulator during sleep mode. LDO's may be configured to a reduced current rate (1mA max) or to an off state. Status of regulator during sleep mode depends on the application, attention must be paid not to leave supplied power domains communicating with non supplied ones avoiding thus unwanted current leakage.
LDO's configuration may be selected through the VRPCMSK1 register address 31 page 1 and by VRPCMSK2 register address 29 page 1 [3].

3.3 Entering in sleep mode

Following flowchart describes L1 SW activity to manage Iota transition to sleep mode for a more detailed description of timings and HW protocol please refer to APN0 [1].

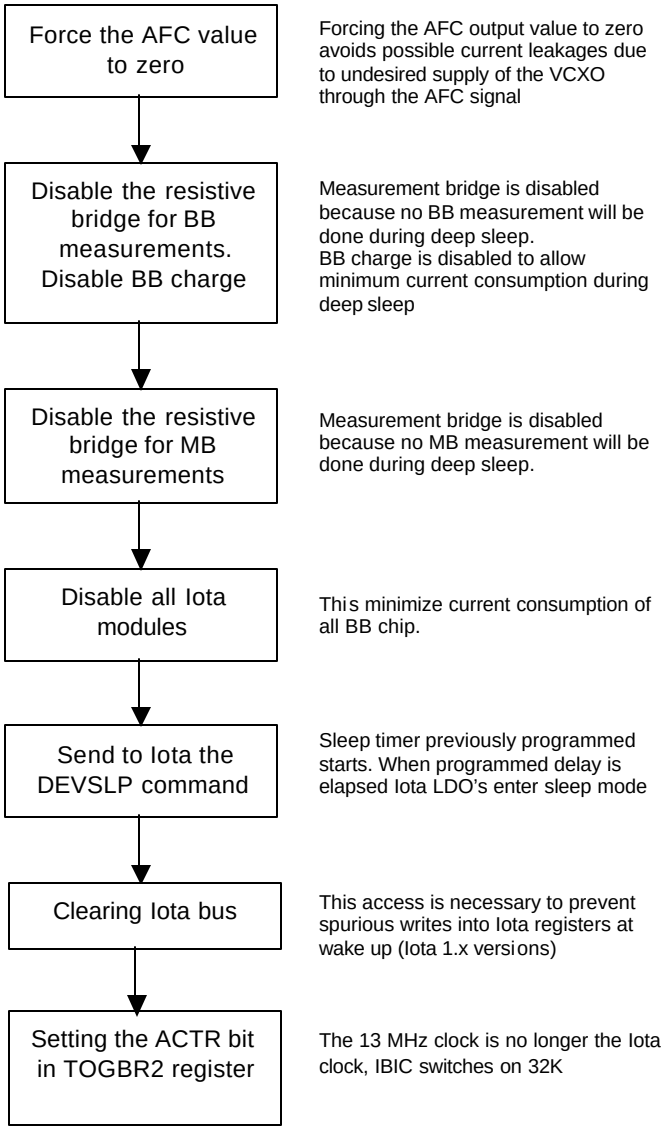

Figure 0-1 SW activity during active to sleep transitions

Note that in this sequence the DEVSLP command is sent to Iota while the ACTIVMCLK is still equal to logic 1. This despite of what was required for the Nausica/Omega case.

4 Exiting the sleep mode

Following flowchart describes L1 SW activity to manage Iota transition out of sleep mode for a more detailed description of timings and HW protocol please refer to APN0.

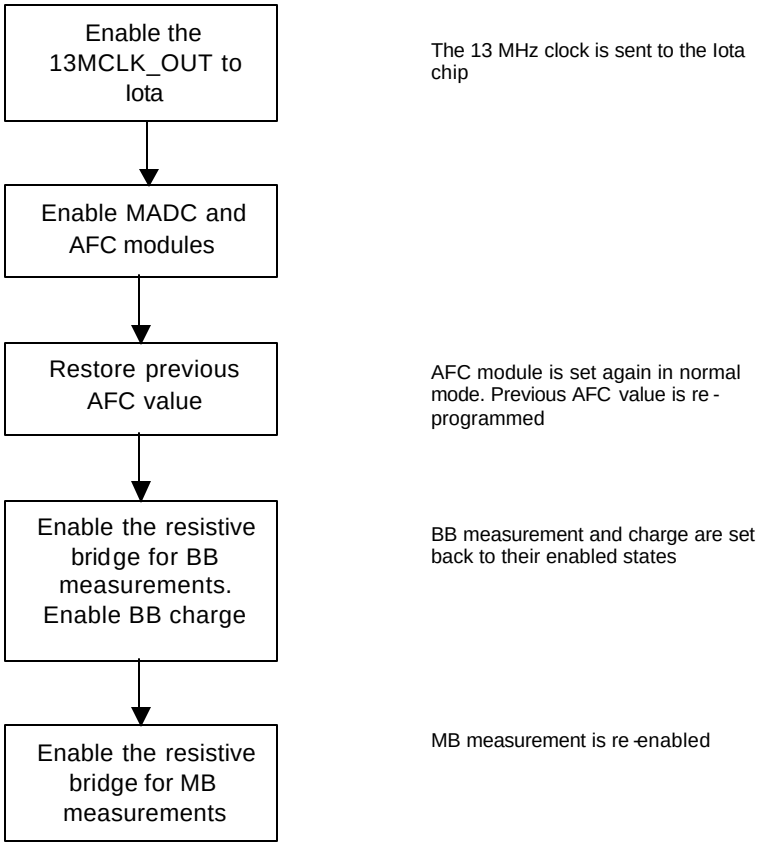

Figure 4-1 SW activity during sleep to active transitions

4.1 Current consumption measurement in sleep mode

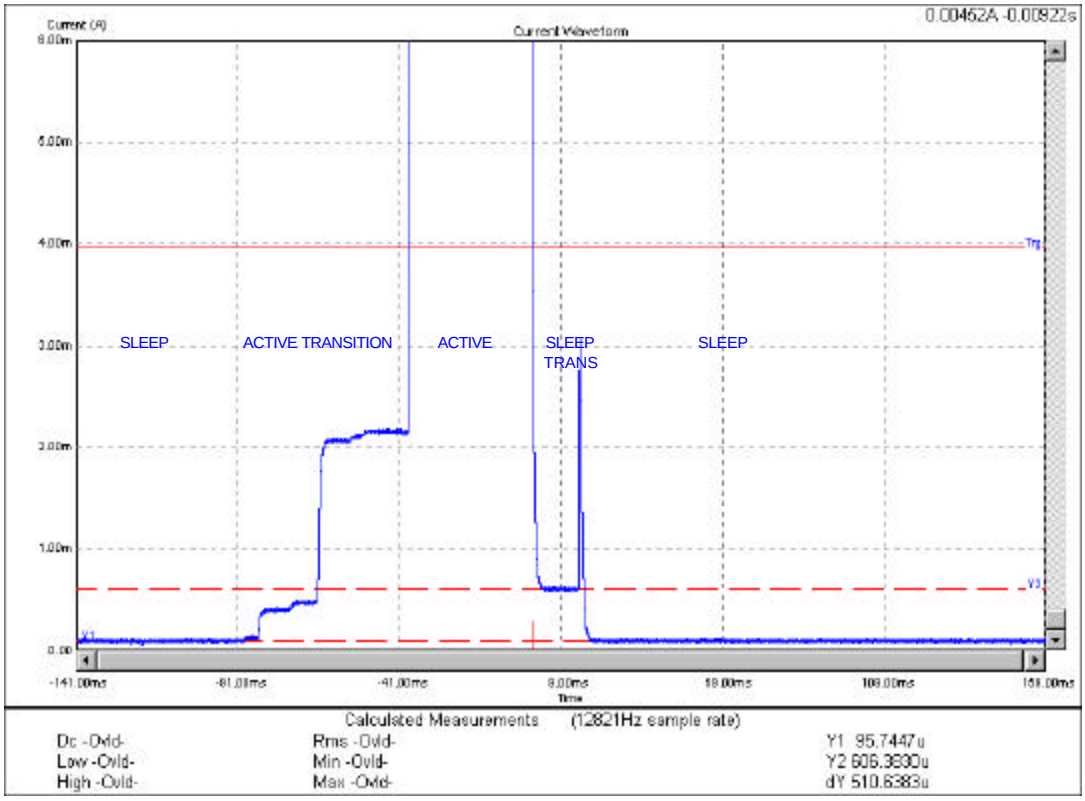

Figure 4-2 VBAT current sink on sleep to active transition.

The two markers indicates the system sleep consumption (Y1) and the Iota LDO's consumption in active mode with system already in deep sleep.

At room temperature with no SIM LDO enabled the overall EMI CONSO board consumption is around 110 uA in SLEEP mode.

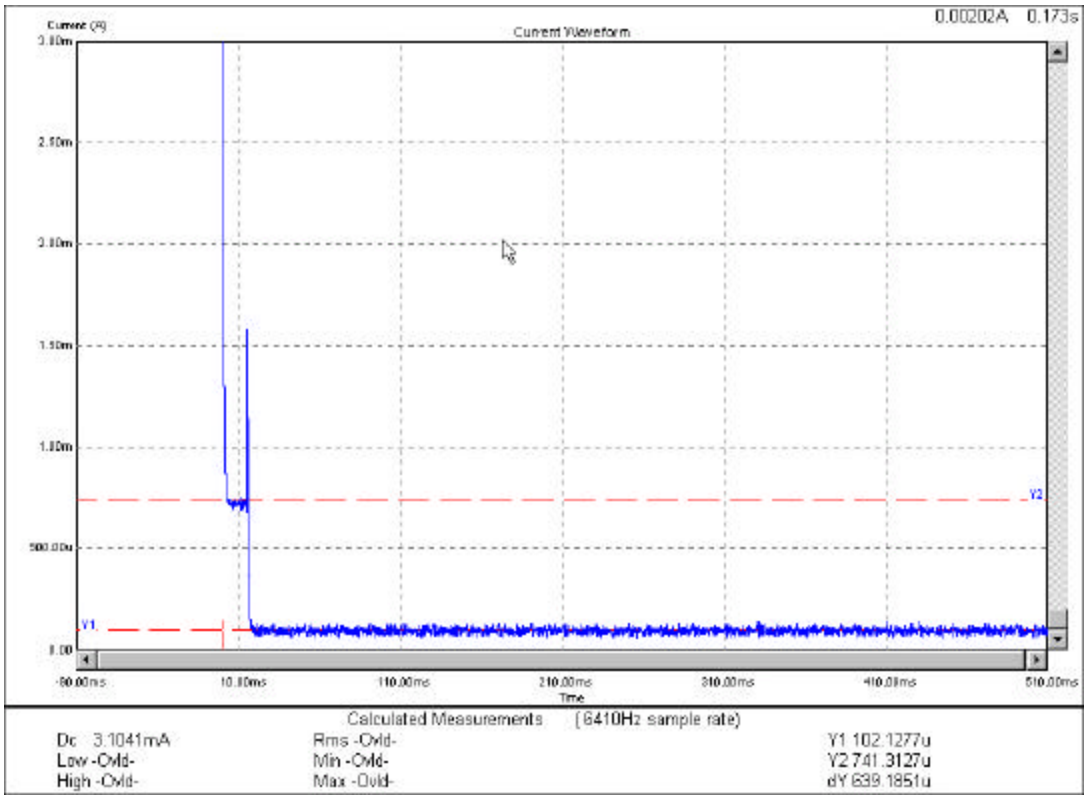

Figure 4-3 Current sink from main battery entering the sleep mode

The markers indicates the Iota LDO's consumption with DBB already in deep sleep and Iota still active (Y2) and the system sleep consumption.
The p eak of current consumption before Iota goes in sleep mode is due to LDO's external decoupling capacitor charge. In sleep mode the bandgap reference voltage is less sharp inducing a slightly higher voltage at regulators output.

4.2 Emi-Conso current consumption in paging mode

To have an average of the system [1] current consumption the following power supply configuration has been adopted.

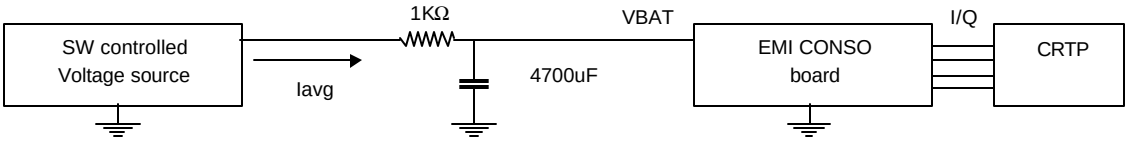

Figure 4-4 Current measurement method

The very low pass filter allows a good averaging of the current sink of the EMI CONSO board during paging modes. Thus is fairly easy to measure through the SW controlled source current flowing into the capacitor with a resolution of uA.
VBAT voltage is subjected to small variations (around 100 mV) due to capacitor discharge, in all measurement the average value of VBAT is always 3.8V.
Leakage current of the capacitor is not subtracted from system current consumption as considered not relevant at a capacitor voltage of 3.8V.

4.2.1 Adopted L1 SW and Scenario description

The L1 version adopted for this evaluation is: SOFTWAREVERSION 0x1367L .

The adopted scenarios mainly includes the following activities:

- Paging block decode 4 Rx windows
- Power monitoring on neighbour 8 Pw windows
- Gauging [2] of the 32KHz clock

A more exhaustive evaluation (slowly moving MS) should keep into account also two neighbors cells to acquire and 4 to confirm every 30s [3] (means the user is moving but not very fast, walking for instance).

[1] System has to be intended as the baseband part of the chipset Calypso/Iota and external flash, from were L1 code is executed. RF VCXO and LCD contributions are not taken into account.

[2] 32 Khz clock measurements (Gauging) are performed each 2 seconds. Block decoding including gauging lasts 13TDMA frames instead of 8 TDMA frames when gauging is not executed.

[3] The slowly moving MS power consumption evaluation must keep into account :
FCH acquisition. Statistically the FCH burst is found within the 6th frame. L1 kills the TPU/RF activity at the beginning of the frame after. This leads to L1 and RF activities for: 2 * 6 * 4.615ms every 30s. This is a large contributor to MS consumption.
SCH acquisition or confirmation: this leads to 6 SCH reading every 30s
BCCH neighbor reading: this lead to 4 Normal burst read every 5mn

4.2.2 Paging modes current measurements

Results for DRX2, DRX5, DRX9 paging modes are summarized in the following three plots.

DRX2 Average current = 1.62 mA

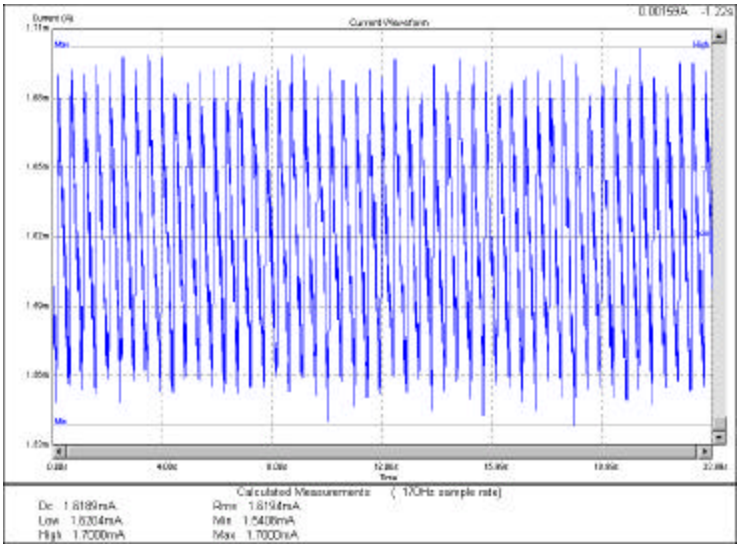

Figure 4-5 DRX2 Average current

DRX5 Average current = 740 uA

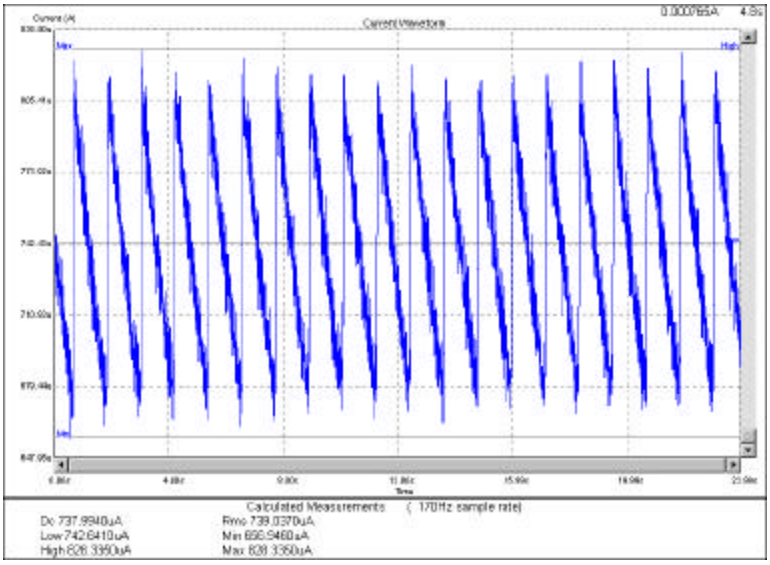

Figure 4-6 DRX5 Average current

DRX9 Average current = 477 uA

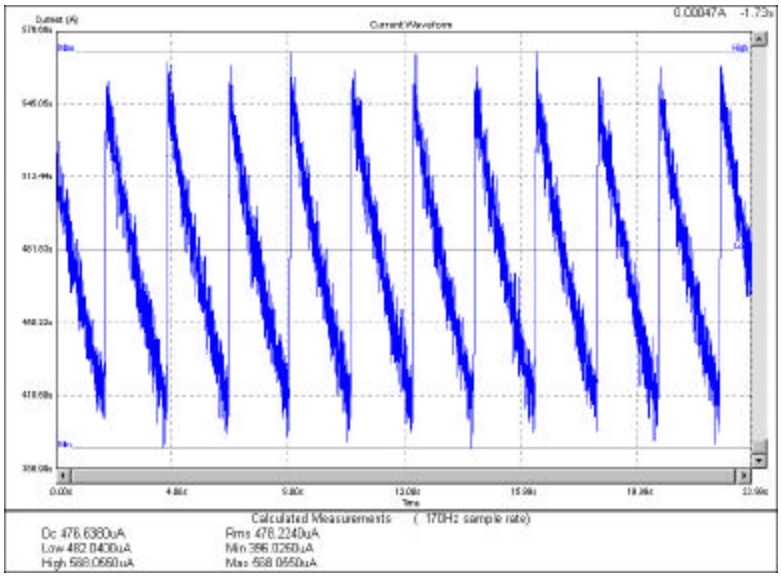

Figure 4-7 DRX9 Average current

5 Further consumption improvements

Further consumption improvements may be achieved with a fine-tuning of the HW system. Gains in terms of current consumption of those improvements are less important than the brought by the introduction of the sleep mode in the ABB. Thus they were not implemented in the actual L1 version also because they are application dependent and related to a second order optimization degree of the system consumption.

5.1 Programmation of the XO32K bias resistor.

The XO32K supply current is selected through the value of a bias resistor. Bias resistor default value is 57 kOhm allowing a quick start of the crystal. This lead to a Calypso split part consumption of 9.5 uA, typical at room temperature, refer to paragraph 2 Current consumption measurements in Backup mode.
Value of this resistor may be changed programming the Calypso register RTC_RES_REG at address 0xFFFE1815 in order to reduce the biasing current once the oscillator is started [2]. Refer to [1] (paragraph 7.2.1.1) for more detailed information on value to be programmed in this register and corresponding bias resistor. An higher value of the resistor leads to a current consumption decrease, highest value brings to a typical Calypso split part consumption of around 3uA, but also a smaller crystal oscillation amplitude. Oscillation amplitude decrease has not to affect correct 32 Khz clock gauging behavior. Thus an appropriate fine-tuning of the resistor value should be done depending on the board application.

5.2 Sleep delay tuning

A fine-tuning of this parameter could bring some improvement in term of system current consumption during paging mode.

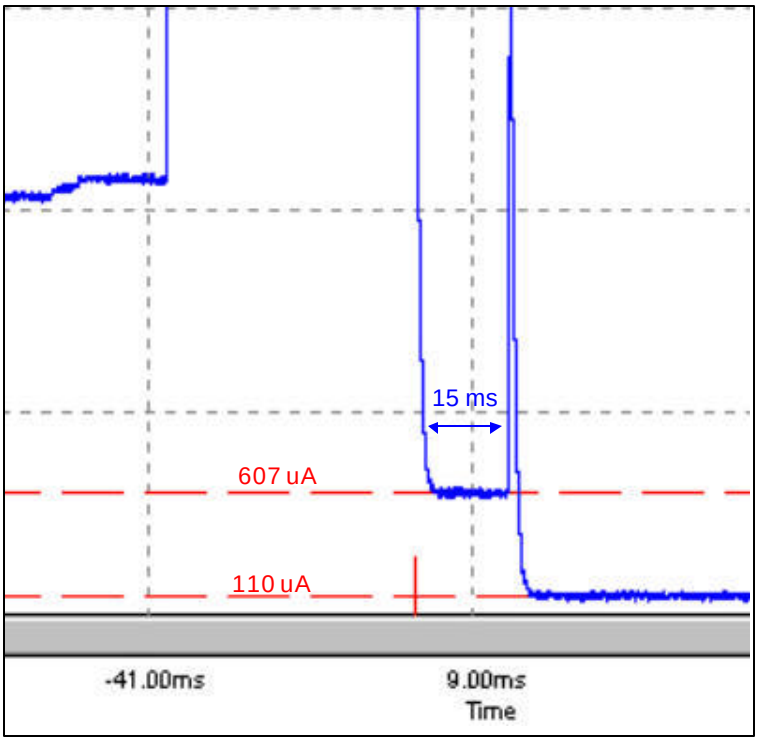

Figure 5-1 Sleep delay parameter tuning

Figure 5-1 shows current consumption of the system entering in sleep mode. The 15 ms time interval as indicated in 4.1 correspond to a system state in which Iota LDO are able to provide max current even if the overall application is already in deep sleep. This time interval can be shortened, thus current consumption reduced, through an appropriate programmation of the Iota VRPCCFG register. Once again value of the sleep delay depends on application thus it is not integrated in current L1 release.

5.3 L1 Setup time tuning

A fine-tuning of the following L1 parameters could bring some improvement in term of system current consumption during paging mode by minimizing the wakeup delay.

SETUP_CLK13: The setup_clk13 is time that the slicer takes to deliver a stable output when slicer is enabled.

SETUP_SLICER: The setup_slicer is the time that the VTCXO takes to deliver a stable output when VTCXO is enabled.

SETUP_VTCXO: The setup_vtcxo is the time the external RF device takes to deliver stable signals to the VTCXO.

SETUP_RF: The SETUP_RF value must be used to delay as much as possible the true start time of the deep sleep wake-up sequence for power consumption saving.