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Technical Report

3rd Generation Partnership Project;
Technical Specification Group Radio Access Network;
High Speed Downlink Packet Access:
Physical Layer Aspects
(Release 5)



The present document has been developed within the 3rd Generation Partnership Project (3GPP TM) and may be further elaborated for the purposes of 3GPP.

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Foreword

This Technical Report has been produced by the 3rd Generation Partnership Project (3GPP).

The contents of the present document are subject to continuing work within the TSG and may change following formal TSG approval. Should the TSG modify the contents of the present document, it will be re-released by the TSG with an identifying change of release date and an increase in version number as follows:

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1 Scope

The purpose of this document is to capture the agreements and evaluation criteria of the different techniques being considered for HSDPA with regards to the overall support of UTRAN for HSDPA.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies. In the case of a reference to a 3GPP document (including a GSM document), a non-specific reference implicitly refers to the latest version of that document in the same Release as the present document.
- [1] 3GPP TR 25.950 v4.0.0 UTRA High Speed Downlink Packet Access
- [2] 3GPP TR 25.855 v0.0.5 UTRA High Speed Downlink Packet Access
- [3] RAN2 stage2 description for HSDPA (TS25.308)

3 Background and Introduction

In RAN#11 plenary meeting a work item was approved for High Speed Downlink Packet Access. The work item includes techniques such as adaptive modulation and coding, hybrid ARQ and fast scheduling with the goal to increase throughput, reduce delay and achieve high peak rates.

4 Basic physical layer structure of HS-DSCH

4.1 HS-DSCH physical-layer structure in code domain

HS-DSCH transmission for FDD uses channelization codes at a fixed spreading factor SF=16. Multi-code transmission is allowed, which translates to UE being assigned multiple channelisation codes in the same TTI, depending on its UE capability. The same scrambling code sequence is applied to all the channelisation codes that form a single HS-DSCH CCTrCH. Furthermore, multiple UEs may be assigned channelisation codes in the same TTI i.e. multiple xing of multiple UE's in code-domain is allowed.

HS-DSCH transmission for TDD uses either a fixed spreading factor SF=16 and multi-code transmission or spreading factor SF=1 on one or more timeslots. Furthermore, a combination of code multiplexing and time multiplexing UEs within an HS-DSCH TTI is possible.

4.2 HS-DSCH physical-layer structure in time domain

For FDD , the length of the HS-DSCH TTI is $3 \times T_{slot}$, where T_{slot} is equal to 2560 chip (≈ 0.67 ms). The TTI for HS-DSCH is a static transport-format parameter.

1.28 Mcps TDD uses a fixed single 5ms TTI. The TTI for 3.84 Mcps TDD is 10 ms.

5 Channel Coding and Modulation for HS-DSCH

5.1 CCTrCH and transport channels

There is only one CCTrCH of HS-DSCH type per UE and only one HS-DSCH per CCTrCH. Also there is one transport block per HS-DSCH TTI. Therefore, there is no need, a) to balance the quality between different HS-DSCH, b) for static rate matching and c) for transport block concatenation. As for the DSCH of Release-99, flexible positions are assumed.

5.2 Code block segmentation

Code block segmentation is done as per Release-99. The maximum code block size for turbo coding is 5114 bits.

5.3 CRC Attachment

A CRC of size 24 bits is calculated and added per HS-DSCH TTI. The CRC polynomial is defined in 3G TS 25.212.

5.4 Channel Coding

HS-DSCH channel coding uses the existing rate 1/3 Turbo code and the existing Turbo code internal interleaver, as outlined in 3G TS 25.212. Other code rates are generated from the basic rate 1/3 Turbo code by applying rate matching by means of puncturing or repetition.

5.4.1 Channel Coding for Control Channels

Defined in Section 8.1 and 8.2.

5.4.2 Physical Layer Channel Coding Chain

Error! Reference source not found. Figure 1 depicts the channel coding and physical layer mapping chain for HS-DSCH.

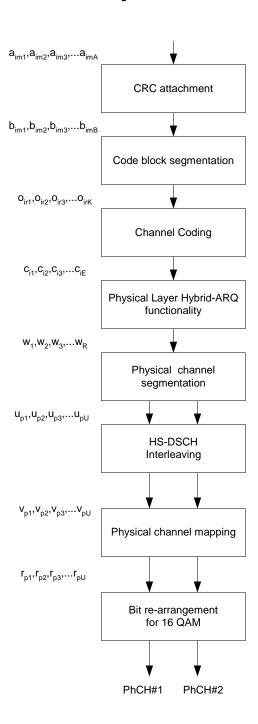


Figure 1. Transport Channel Coding Structure for HS-DSCH

5.5 Physical-layer Hybrid-ARQ functionality

The physical-layer Hybrid-ARQ functionality is an extension of the release 99 rate matching. The Hybrid-ARQ functionality matches the number of bits at the output of the channel (turbo) coder to the total number of bits of the HS-DSCH physical channels. The Hybrid-ARQ functionality is controlled by the parameter RV (Redundancy Version), i.e. the exact set of bits at the output of the physical-layer Hybrid-ARQ functionality depends on the number of input bits, the number of output bits, and the RV parameter.

The physical-layer Hybrid ARQ functionality consists of two rate-matching stages as shown in Figure 2.

The first rate-matching stage is identical to the release 99 rate-matching functionality except that the number of output bits does not match to the number of physical-channel bits available in the HS-DSCH TTI. Instead, the number of

output bits matches to the available UE soft-buffering capability, information about which is provided by higher layers. Note that, if the number of input bits does not exceed the UE soft-buffering capability, the first rate-matching stage is transparent.

The second rate matching stage matches the number of bits after first rate matching to the number of physical channel bits available in the HS-DSCH TTI. The second rate matching also uses the release 99 rate matching algorithm. However, the rate matching only considers bits that have not been punctured by the first rate matching stage and the rate matching parameters used in a particular transmission are controlled by the redundancy version (RV) parameter.

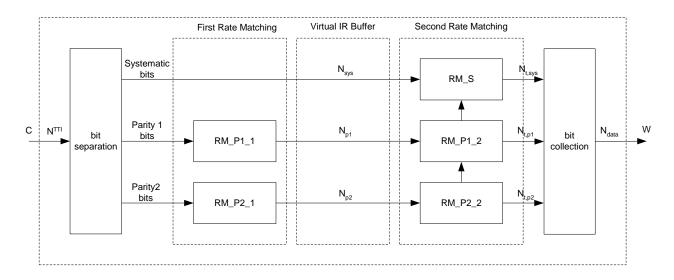


Figure 2. Physical layer Hybrid ARQ functionality

5.5.1 Parameter of First Rate Matching Stage (UE Buffer Rate Matching)

The parameters of the first rate matching stage are determined as in subclause 4.2.7.2.2.3 of [2], with parameter modifications as detailed below.

Denote the number of soft bits available at the UE for soft combining of HARQ channel n as $N_{UE,n}$ and the number of coded bits in a TTI before rate matching on TrCh i with transport format l as $N_{i,l}^{TTI}$.

If $N_{UE,n}$ is greater or equal than $N_{i,l}^{TTI}$, i.e., all turbo coded bits of the corresponding TTI can be stored, the first rate matching stage shall be transparent. This can, e.g., be achieved by setting $e_{minus} = 0$. Note, that no repetition is performed.

If $N_{UE,n}$ is smaller than $N_{i,l}^{TTI}$, the parity bit streams are punctured as in 4.2.7.2.2.3 of [2] by setting the total number of punctured bits per TTI to:

$$\Delta N_{il}^{TTI} = N_{UE,n} - N_{i,l}^{TTI}$$

5.5.2 Parameter of Second Rate Matching Stage (Channel Rate Matching)

HARQ second stage rate matching for the HS-DSCH transport channel shall be done with the general method described in 4.2.7.5 of TS25.212 with the following specific parameters.

The parameters of the second rate matching stage depend on the value of the RV parameters s and r. The parameter s can take the value 0 or 1 to distinguish self-decodable (s = 1) and non self-decodable (s = 0) transmissions. The parameter r (range 0 to r_{max}) changes the initial error variable e_{ini} in the case of puncturing. In case of repetition both

parameters r and s change the initial error variable e_{ini} . The parameters X, e_{plus} and e_{minus} are calculated as per table 1 below.

Denote the number of bits before second rate matching as N_{sys} for the systematic bits, N_{p1} for the parity 1 bits, and N_{p2} for the parity 2 bits, respectively. Denote the number of physical channels used for the CCTrCH by P. N_{data} is the number of bits available to the CCTrCH in one radio frame and defined as $N_{data} = P \times 3 \times N_{data1}$, where N_{data1} is defined in TS25.212. The rate matching parameters are determined as follows.

For $N_{data} \leq N_{sys} + N_{p1} + N_{p2}$, puncturing is performed in the second rate matching stage. The number of transmitted systematic bits in a retransmission is $N_{t,sys} = \min\{N_{sys}, N_{data}\}$ for a transmission of self-decodable type and $N_{t,sys} = \max\{N_{data} - (N_{p1} + N_{p2}), 0\}$ in the non self-decodable case.

For $N_{data} > N_{sys} + N_{p1} + N_{p2}$ repetition is performed in the second rate matching stage. A similar repetition rate in

all bit streams is achieved by setting the number of transmitted systematic bits to $N_{t,sys} = \left| N_{sys} \cdot \frac{N_{data}}{N_{sys} + 2N_{p2}} \right|$.

The number of parity bits in a transmission is: $N_{t,p1} = \left\lfloor \frac{N_{data} - N_{t,sys}}{2} \right\rfloor$ and $N_{t,p2} = \left\lceil \frac{N_{data} - N_{t,sys}}{2} \right\rceil$ for the parity 1 and parity 2 bits, respectively.

Table 1 below summarizes the resulting parameter choice for the second rate matching stage. The parameter a in the table is chosen using a = 2 for parity 1 and a = 1 for parity 2.

Table 1- Parameters for HARQ second rate matching

	Xi	e _{plus}	e _{minus}
Systematic RMS	N_{sys}	N_{sys}	$\left N_{sys}-N_{t,sys}\right $
Parity 1 RM P1_2	N_{p1}	$a \cdot N_{p1}$	$a \cdot N_{p1} - N_{t,p1} $
Parity 2 RM P2_2	N_{p2}	$a \cdot N_{p2}$	$a \cdot N_{p2} - N_{t,p2} $

The rate matching parameter e_{ini} is calculated for each bit stream according to the RV parameters r and s using

$$e_{\mathit{ini}}\left(r\right) = \left\{ \left[X_i - \left(r \cdot e_{\mathit{plus}} / r_{\mathit{max}}\right) - 1 \right] \bmod e_{\mathit{plus}} \right\} + 1 \text{ in the case of puncturing , i.e., } N_{\mathit{data}} \leq N_{\mathit{sys}} + N_{\mathit{p1}} + N_{\mathit{p2}} \text{ , and } n_{\mathit{p3}} = 1 \text{ and } n_{\mathit{p3}} = 1$$

$$e_{\mathit{ini}}\left(r\right) = \left\{ \left[X_{\mathit{i}} - \left(\left(s + 2 \cdot r\right) \cdot e_{\mathit{plus}} / \left(2 \cdot r_{\max}\right) \right) - 1 \right] \bmod e_{\mathit{plus}} \right\} + 1 \, \text{for repetition, i.e., } N_{\mathit{data}} > N_{\mathit{sys}} + N_{\mathit{p1}} + N_{\mathit{p2}} \, .$$

Where $r \in \{0,1,\dots,r_{\text{max}}-1\}$ and r_{max} is the total number of redundancy versions allowed by varying r. Note that r_{max} varies depending on the modulation mode.

Note: For the modulo operation the following clarification is used: the value of $(x \mod y)$ is strictly in the range of 0 to y-1 (i.e. -1 mod 10 = 9).

5.5.2.1 HARQ bit collection

The HARQ bit collection is achieved using a rectangular interleaver of size $N_{row} \times N_{col}$.

The number of rows and columns are determined from:

$$N_{row} = \log_2(M)$$
$$N_{col} = F / N_{row}$$

where M is the modulation size and F is the number of coded and rate-matched bits to be transmitted.

Data is written into the interleaver column by column, and read out of the interleaver column by column.

 $N_{L_{SNS}}$ is the number of transmitted systematic bits. Intermediate values N_r and N_c are calculated using:

$$N_r = \left| \frac{N_{t,sys}}{N_{col}} \right| \text{ and } N_c = \left(\frac{N_{t,sys}}{N_{col}} - N_r \right) \cdot N_{col}.$$

If N_c =0, the systematic bits are written into rows 1... N_r .

Otherwise systematic bits are written into rows $1...N_r+1$ in the first N_c columns and rows $1...N_r$ in the remaining N_c columns. The remaining space is filled with parity bits. The parity bits are written column wise into the remaining rows of the respective columns. Parity 1 and 2 bits are written in alternating order.

In the case of 16QAM for each column the bits are read out of the interleaver in the order row 1, row 3, row 2, row 4. In the case of QPSK for each column the bits are read out of the interleaver in the order row 1, row 2.

$$N_{t,sys} = \max \{ N_{data} - (N_{p1} + N_{p2}), 0 \}$$

5.6 DTX indication bits

DTX insertion is not employed. Since only one transport channel per TTI is supported, the rate-matching algorithm is used to fill the available physical resource, instead of using DTX insertion.

5.7 Interleaving

The interleaving for FDD is done as shown in figure below, separately for each physical channel. For QPSK the interleaver is the same as Rel-99 2^{nd} interleaver described in Section 4.2.11 of TS25.212. The interleaver is of fixed size: R2=32 rows and C2=30 columns.

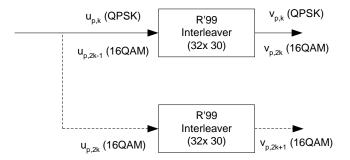


Figure 3. Interleaver structure for HSDPA

For 16QAM, there are two identical interleavers of the same fixed size $R2 \times C2 = 32 \times 30$. The output bits from the physical channel segmentation are divided between the interleavers: all odd numbered bits to interleaver one and all even numbered bits to interleaver two.

Note: the outputs of the interleavers will result in mapping to 16QAM symbols such that the output of first interleaver is mapped to the more reliable positions (i_1 and q_1) whereas the output of the second interleaver is mapped to the less reliable positions (i_2 and q_2).

For TDD, interleaving adaptation has to be done to the HS-DSCH TTI length.

5.8 Physical channel mapping

The bits can be mapped to multiple physical channels in the same way as in release 99.

5.9 Bit re-arrangement for 16 QAM

This function only applies to 16 QAM modulated bits. In case of QPSK it is transparent.

The following table describes the operations that produce the different rearrangements.

The bits of the input sequence are mapped in groups of 4 so that v_{pk} , v_{pk+1} , v_{pk+2} , v_{pk+3} map to $i_1i_2q_1q_2$, where k mod 4 = 0

Bit **Output bit** rearrangement Operation sequence parameter b 0 None $i_1q_1i_2q_2$ 1 Swapping i_1 with i_2 and q_1 with q_2 $i_2q_2i_1q_1$ 2 XOR with 0011 (equivalent to inversion of the logical values of i_2 and q_2) $i_1q_1i_2q_2$ 3 Swapping i_1 with i_2 and q_1 with q_2 and XOR with 0011 $i_2 q_2 i_1 q_1$

Table 1. Bit re-arrangement for 16 QAM

The output bit sequences from the table above map to the output bits in groups of 4, i.e. r_{pk} , r_{pk+1} , r_{pk+2} , r_{pk+3} , where k mod 4 = 0.

5.10 Modulation

Two types of modulations namely QPSK and 16-QAM may be applied for HS-DSCH.

6 Link Adaptation

For HS-DSCH, the transport format, including the modulation scheme and code rate, can be selected based on the downlink channel quality. The selection of transport format is done by the MAC-HS located in Node B and can be based on e.g. channel-quality feedback reported by the UE, see Section 9, or from the transmit power of an associated DPCH. Other methods may also be possible.

7 Hybrid ARQ

7.1 Choice of Hybrid ARQ combining schemes

- a) For a retransmission, the transport-block set is the same as for the initial transmission. This means that, for a retransmission, the number of information bits N_{INFO} to be transmitted is the same as for the initial transmission. Furthermore, for a retransmission, the modulation scheme and the channelisation-code set, including the size of the channelisation-code set, and the transmission power, may be different compared to the initial transmission. This means that, for a retransmission, the number of available channel bits N_{ch} may differ compared to the initial transmission. Even if the number of available channel bits N_{ch} is the same, the set of channel bits may be different for the retransmission compared to the initial transmission (Incremental Redundancy).
- b) Regardless of the number of information bits N_{INFO} , channel coding is done using a Turbo code with rate $R_{basic} = 1/3$. Each retransmission may use a different redundancy version, where each redundancy version is a different subset of the coded bits. Each subset may contain a different number of bits. Chase combining corresponds to defining or using only a single redundancy version.

7.2 Physical layer aspects of Hybrid ARQ

The following signalling is needed to support Hybrid ARQ. The details of signalling are described in Section 9.

Downlink Signaling

The HARQ information includes the Hybrid ARQ process identifier in the corresponding HS-DSCH TTI. The HARQ information also includes information about the redundancy version of the transmission in the corresponding HS-DSCH TTI.

Uplink Signaling

For communicating the HARQ acknowledgements, an I-bit ACK/NACK indication is used in the uplink.

8 Associated Signalling

8.1 Downlink

8.1.1 Overall Structure

Figure 4 illustrates the basic physical-channel structure for the HS-DSCH-related associated downlink signalling as seen from the UE point-of-view. It consists of a downlink DPCH and a number of HS-SCCHs. For each HS-DSCH TTI, each Shared Control Channel (HS-SCCH) carries HS-DSCH-related downlink signaling for one UE. The number of HS-SCCHs can range from a minimum of one HS-SCCH (M=1) to a maximum of four HS-SCCH's (M=4). Note that this is the number of HS-SCCH as seen from the UE point-of-view. More than four HS-SCCH can be configured per cell. The UE has the capability to simultaneously monitor 4 HS-SCCH.

In case of HS-DSCH transmission to the same UE in consecutive HS-DSCH TTIs, the same HS-SCCH should be used for the corresponding associated downlink signalling.

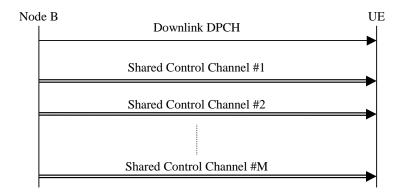


Figure 4. Basic physical-channel structure for HS-DSCH-related associated downlink signalling

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8.1.2 Detailed Structure FDD

Shared Control Channel

For FDD, following information is carried on the HS-SCCH:

- Transport-format and Resource related Information (TFRI)
- Channelization-code set: 7 bits
- Modulation scheme: 1 bit
- Transport-block size: 6 bits
- Hybrid-ARQ-related Information (HARQ information)

- Hybrid-A RQ process number: 3 bits

- Redundancy version: 3 bits

New-data indicator: 1 bit

- UE ID: [10] bits implicitly encoded (see also section on CRC attachment)

The exact number of bits for the Hybrid-ARQ-related information is to be confirmed with RAN2.

The HS-SCCH information is split into two parts:

- Part-1: Channelization code set and modulation scheme (8 bits)
- Part-2: Transport-block size and Hybrid-ARQ-related information ([12] bits)

CRC attachment

Figure 5 illustrates the CRC attachment for HS-SCCH. One CRC is calculated over and attached to the HS-SCCH information.

- CRC (Release 99 16-bits CRC) is calculated over Part-1 + Part-2 and appended to Part-2.

The [10] bits UE ID is included in the calculation of CRC-1.

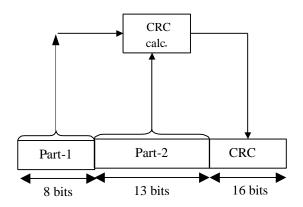


Figure 5. CRC attachment for HS-SCCH

Channel coding

Part 1 is convolutionally coded using R99 R=1/2 coding with 8 tail bits. Part 2 and the CRC is convolutionally coded using R99 R=1/2 coding with 8 tail bits.

Interleaving and rate matching

After convolutional coding, interleaving and rate matching to 120 SCCH-HS channel bits (3 slots) is applied. The interleaving and rate matching is carried out separately for the two parts of the coded SCCH-HS to allow for early extraction of the time-critical information of Part-1 of the SCCH-HS information.

Scrambling of Part-1 by UE Specific ID

The post convolutionally encoded Part-1 is scrambled by the UE ID as shown in Figure 6. The scrambler is based on a (32,10) block code specified in TS 25.212. At the receiver, after descrambling by the UE specific ID, the metric of the maximum likelihood path during the Viterbi decoder process may be used to form a basis for the validity of the Part-1 information. This is required so that the Part 1 information is available before the start of HS-DSCH TTI.

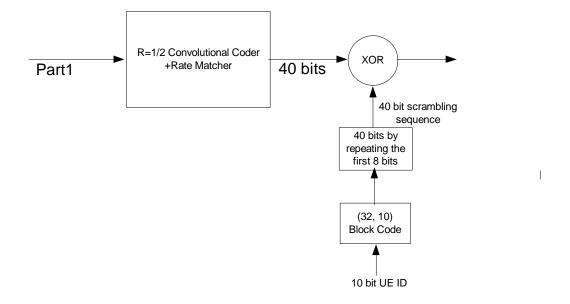


Figure 6. Scrambling of Part-1 by UES pecific ID

Redundancy and constellation version coding

The redundancy version (RV) parameters r, s and constellation version parameter b are coded jointly to produce the value X_{rv} . X_{rv} is alternatively represented as the sequence $x_{rv,1}$, $x_{rv,2}$, $x_{rv,3}$ where $x_{rv,1}$ is the msb. This is done according to the following tables according to the modulation mode used:

X_{rv} (value) b n

Table 2. RV coding for 16 QAM

Table 3. RV coding for QPS K

X _{rv} (value)	S	r
0	1	0
1	0	0
2	1	1
3	0	1
4	1	2
5	0	2
6	1	3
7	0	3

Timing relations for HS-DSCH-related downlink signalling

Figure 7 illustrates the timing structure for the HS-DSCH control signalling. The fixed time offset between the HS-SCH information and the start of the corresponding HS-DSCH TTI equals $\tau_{\text{HS-DSCH-control}}$ (2*T_{slot}=5120chips).

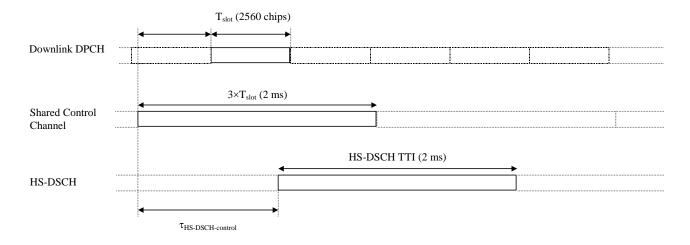


Figure 7. Timing structure for HS-DSCH control signalling

8.1.3 Detailed Structure TDD

The TDD overall downlink signalling structure is based on associated dedicated channels and HS-SCCHs. As in Release-99, the associated dedicated channel can also be a fractionated channel for efficient resource usage with a corresponding repetition period in terms of TTIs. The UE is informed of an HS-DSCH allocation by means of a signalling message on an HS-SCCH. The UE shall be allocated a set of up to 4 HS-SCCHs, and shall monitor all of these HS-SCCHs continuously. In any given TTI, a maximum of one of these HS-SCCHs may be addressed to the UE. In the case that a UE detects a message for it on a specific HS-SCCH, then it may restrict its monitoring of HS-SCCHs to only that HS-SCCH in the next TTI.

8.1.3.1 HS-SCCH

For each HS-DSCH TTI, each HS-SCCH carries HS-DSCH-related downlink signalling for one UE. The following information is carried on the HS-SCCH:

• UE Identifier

Since the HS-SCCH may be being monitored by more than one UE, an identifier is required to identify the intended recipient. The UE Identifier is a 10 bit field that is combined with a 16 bit CRC. The combined field is generated by computing the CRC as normal, and then scrambling the computed CRC by the modulo 2 addition of an extended UE identifier. The UE identifier shall be extended by zero padding.

• Transport-format and Resource related Information (TFRI) The TFRI includes information about the dynamic part of the HS-DSCH transport format that identifies to the UE which resources are being used for the HS-DSCH, and how the data is being carried by these resources. The TFRI information fields required by the UE are:

Table 4: TFRI Information Fields

Para meter	1.28 Mcps TDD (5ms TTI)	3.84 Mcps TDD (10ms TTI)
Resource Allocation	13 bits (code + timeslot allocation)	21 bits (code + timeslot allocation)
Modulation	1 bit	1 bits
Transport Block Size	6 bits	9 bits

The mapping scheme for the Resource Allocation field is shown in **Figure** 8 and **Figure** 9 below where, for 3.84 Mcps, $\{Xi : i = 0..N; N£12\}$ is the set of downlink timeslots available for use by the HS-DSCH. To signal an SF=1 allocation to the UE, a (Start Code, Stop Code) combination of (16, 1) shall be signalled.

Start Code	Stop Code	TS2	TS3	TS4	TS5	TS6
(4 bits)	(4 bits)	(1 bit)				

Figure 8: TFRI Resource Allocation Field Mapping for 1.28 Mcps TDD

Start Code	Stop Code	TSX ₀	TSX₁	TSX _N
(4 bits)	(4 bits)	(1 bit)	(1 bit)	(1 bit)

Figure 9: TFRI Resource Allocation Field Mapping for 3.84 Mcps TDD

HARQ

This is information that identifies to the UE the relationship between the current data being sent and other blocks sent previously.

- HARQ process identifier = 3 bits
- New data indicator = 1 bit
- Incremental redundancy version number = 3 bits
- Uplink Synchronisation (1.28 Mcps TDD only)
 2 SS bits are used to maintain synchronisation for the associated HS-SICH.
- TPC (1.28 Mcps TDD only)
 2 TPC bits are used to control the power of the associated HS-SICH.

8.1.3.2 Associated Downlink DPCH

For 1.28 Mcps TDD, each UE requires an associated downlink DPCH to provide SS commands to the UE in order to maintain associated uplink DPCH and HS-SICH timing. For 3.84 Mcps TDD, there is no explicit requirement for an associated downlink DPCH to support the physical layer. However, there may be higher layer requirements.

8.1.3.3 Timing relations for the HS-DSCH related Downlink Signalling

For 3.84 Mcps, there is a minimum of 5 timeslots between HS-SCCH and HS-DSCH. For 1.28 Mcps, there is a minimum of 2 timeslots between the HS-SCCH and the HS-DSCH.

8.1.3.4 HS-SCCH Coding

8.1.3.4.1 1.28 Mcps TDD

The information fields of the HS-SCCH are multiplexed together to form a single 43 bit field, which is then encoded using the R99 ½-rate convolutional coder, which yields an encoded block size of 153 bits. The encoded block is mapped to two bursts, one using Slot Format 0, which has a payload of 88 bits, and the other using Slot Format 5, which has a payload of 84 bits, plus TPC and SS bits for the HS-SICH. The R99 rate-matching algorithm is used to adapt the encoded block size to the actual slot payload.

The coding and multiplexing process for the 1.28 Mcps TDD HS-SCCH is shown below.

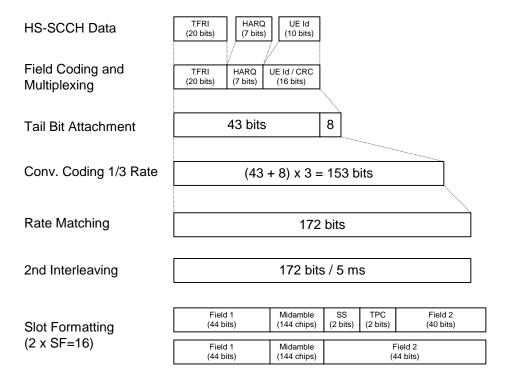
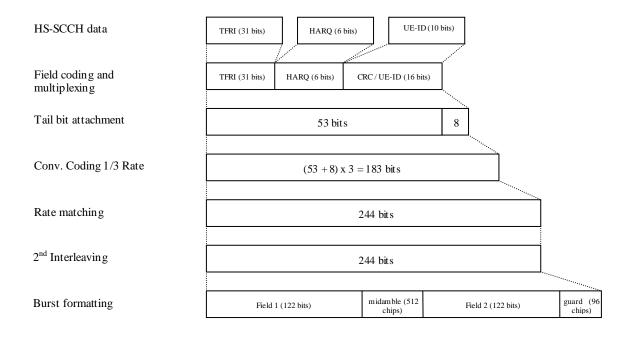


Figure 10. Coding and Multiplexing Scheme for HS-SCCH

8.1.3.4.2 3.84 Mcps TDD

Burst Type 1, which has a data payload of 244 bits is used for HS-SCCH. The TFRI, HARQ information and CRC / UE-ID are combined into a single 53 bit field. The Release 99 rate 1/3 convolutional encoder expands this field to 183 bits. Rate matching matches these 183 bits to the 244 bits available in burst type 1. The coding and multiplexing process for HS-SCCH is given in the figure below:



Coding and Multiplexing Scheme for 3.84 Mcps HS-SCCH

8.1.3.5 HS-SCCH Power Control

For both 1.28 Mcps and 3.84 Mcps TDD, the initial transmit power of the HS-SCCH shall be specified by higher layers. If there exists a downlink DPCH between the NodeB and the UE, the initial power could be a UE specific offset from the current transmit power to this DPCH.

Following the initial transmission, the NodeB may optionally power control the HS-SCCH. This may be done using TPC commands sent by the UE in the HS-SICH, or by using additional information available to the NodeB, such as missing HS-SICHs or the transmit power of the associated downlink DPCH. This procedure need not be standardised. However, when TPC bits are used, the method of generating these bits in the UE does need to be standardised. TPC bits in the HS-SCCH are mandatory for 1.28 Mcps TDD. The following procedure shall be used in the UE to generate these TPC bits:

- 1. The UE shall be signalled a BLER target for the HS-SCCH by higher layers. The initial SIR target value shall be set autonomously by the UE.
- 2. The UE shall not adapt its SIR target until it has detected an HS-SCCH transmission intended for it. Errors in HS-SCCH transmissions received before this first detected transmission shall not count towards the BLER target.
- 3. Once the UE has detected this first HS-SCCH transmission, it may start to adapt its SIR target in order to meet the specified BLER target. For the purposes of BLER estimation, the UE shall assume that an HS-SCCH message is scheduled for it in every TTI following the first detected HS-SCCH transmission (whether this is true or not).
- 4. If, following the detection of the first HS-SCCH transmission intended for the UE, a period of 8 TTIs elapses during which the UE does not detect any HS-SCCH transmissions intended for it, the UE shall reset its SIR target to the initial value and shall not start adapting it again until it has detected a subsequent HS-SCCH transmission intended for it. Errors in HS-SCCH transmissions received during this period (i.e. after the last detected HS-SCCH transmission intended for the UE but before the subsequent detected HS-SCCH transmission intended for the UE) shall not count towards the BLER target.

In scenarios where the NodeB does schedule HS-SCCH transmissions to the UE continuously between the first detected and last detected transmissions, the target BLER should be met if the NodeB follows the TPC commands received from the UE. If this is not the case, then the BLER target may not be met, and alternative methods of power controlling the HS-SCCH should be considered.

8.1.4 Other aspects

{This section should describe how the downlink signalling operates in soft-handoff mode etc.}

8.2 Uplink

8.2.1 Overall Structure

In FDD, the HS-DSCH related uplink signalling uses DPCCH-HS with SF=256 that is code multiplexed with the existing dedicated uplink physical channels. The HS-DSCH related uplink signalling consists of H-ARQ acknowledgement and channel quality indicator.

In contrast to FDD, the TDD UE does not use its dedicated channel in uplink for transmitting ACK/NACK information, due to the associated fractionated dedicated channel option. To enable a SYNC UL scheme for HARQ, the UE will use a shared uplink resource for transmitting ACK/NACK information. The relation between the HS-SCCH in DL and shared UL resource can be pre-defined and is not signalled dynamically on the HS-SCCH.

8.2.2 Detailed Structure FDD

8.2.2.1 HS-DSCH Associated Uplink Dedicated Control Channel

The following information is carried on the HS-DSCH associated uplink dedicated control channel (DPCCH-HS):

- H-ARQ acknowlegemnt

A 1-bit Ack/Nack indication is used for a H-ARQ acknowledgement. The acknowledgement bit is repetition coded to

10 bits and transmitted in one slot. H-ARQ acknowledgement field is DTX'ed when there is no ACK/NACK information being sent.

- Measurement feedback information

Measurement feedback information contains channel quality indicator that may be used to select transport format and resource by HS-DSCH serving Node-B. A 5-bit channel quality indicator is coded and transmitted over two slots. The channel quality information is coded using a (20,5) code. The code words of the (20,5) code are a linear combination of the 5 basis sequences denoted $M_{\rm in}$ defined in the table below.

ı	M _{i,0}	M _{i,1}	M _{i,2}	M _{i,3}	M _{i,4}
0	1	0	0	0	1
1	0	1	0	0	1
2	1	1	0	0	1
3	0	0	1	0	1
4	1	0	1	0	1
5	0	1	1	0	1
6	1	1	1	0	1
7	0	0	0	1	1
8	1	0	0	1	1
9	0	1	0	1	1
10	1	1	0	1	1
11	0	0	1	1	1
12	1	0	1	1	1
13	0	1	1	1	1
14	1	1	1	1	1
15	0	0	0	0	1
16	0	0	0	0	1
17	0	0	0	0	1
18	0	0	0	0	1
19	0	0	0	1	0

Table 5. Basis sequences for (20,5) code

The transmission cycle and timing for channel quality indicator is determined by UTRAN and signalled by higher layer. (*Note: It is to be determined whether the transmission cycle is influenced by HS-DSCH activity* or downlink channel quality) Details for measurement feedback procedure is described in section 8.2.2.2.

The format for the additional DPCCH is shown in Figure 11. The ACK/NACK message is transmitted with a power offset $\Delta P_{\rm AN}$ for ACK and $\Delta P_{\rm NAN}$ for NACK relative to the Release '99 uplink DPCCH. The power offset $\Delta P_{\rm AN}$ and $\Delta P_{\rm NAN}$ is a higher-layer parameter. The UE shall repeat the transmission of the ACK/NACK information over $N_{\rm acknack_transmit}$ consecutive HS-DPCCH sub-frames, in the slots allocated to the HARQ-ACK. When $N_{\rm acknack_transmit}$ is greater than one, the UE shall not attempt to receive nor decode transport blocks from the HS-PDSCH in HS-DSCH sub-frames n+1 to $n+(N_{\rm acknack_transmit}-1)$ where n is the number of the last HS-DSCH sub-frame in which a transport block has been received.

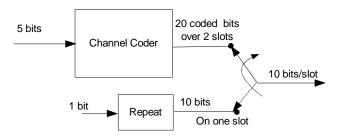


Figure 11. Format for additional DPCCH for HS-DSCH related uplink signalling

8.2.2.2 Measurement feedback procedure

8.2.2.2.1 UE procedure

This section provides an example for UE internal procedure used in adaptive modulation and coding operation. (*Note: following procedures need to be checked by WG4*)

UE procedure for reporting channel quality indication (CQI):

- 1) The UE derives the CQI from observations of the P-CPICH (alternatively S-CPICH in case of beamforming with S-CPICH is used).
- 2) The UE shall transmit the CQI on the HS-DPCCH sub frame which satisfies:

 $HSFN \mod k = l$

where HSFN is the sub frame counter version of SFN and defined as

HSFN = 5*SFN + HS-DPCCH sub frame

- 3) The UE shall repeat the transmission of the CQI feedback information derived in 1) over *N_cqi_transmit* consecutive HS-DPCCH sub frames in the slots respectively allocated to the CQI.
- 4) The UE shall not transmit the CQI in other subframes than those described in 2) and 3).

8.2.2.2.2 Parameters provided to the UE measurement feedback operation

- 1) Following connection specific parameters are informed to the UE by higher layer signal ling:
 - 1) HS-SCCH set to be monitored
 - 2) Repetition factor of ACK/NACK: N_acknack_transmit
 - 3) Channel Quality Indicator (CQI) feedback cycle k. k has a possible value of [1,5, 10,20,40,80] corresponding to the feedback cycle of [2,10,20,40,80, 160] msec. In addition, with the indication k=0, measurement feedback can be shut off completely
 - 4) CQI feedback offset *l*.
 - 5) Repetition factor of CQI: N_cqi_transmit

The use for the measurement feedback cycle *k* and feedback offset *l* is illustrated in Figure 12. (*Note: The timing relations in the figure do not reflect the differences in DPCH frame offset.*)

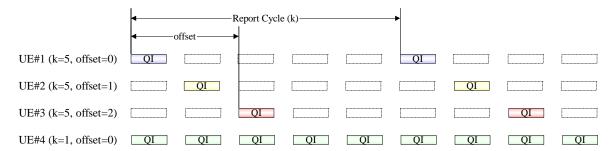


Figure 12 An illustration of feedback measurement transmission timing

8.2.2.2.3 Measurement feedback or Channel Quality Indicator (CQI) definition

CQI reports one value at a time from the CQI report definition. CQI report definition is a table containing 32 values, each of which is defined with N parameters. These parameters shall consist of one or more of the following: [the transport block size, the coding rate, the number of HS-PDSCH codes, modulation, power offsets, BLER_{threshold}, P_{hs} =default power offset between HS-DSCH code channel and CPICH]

8.2.2.3 Uplink DPCCH/HS-DPCCH timing relation

Figure 13 shows the timing offset between the downlink associated DPCH and the uplink DPCCH. The code-multiple xed uplink HS-DPCCH starts m*256 chips after the start of the uplink DPCCH with m selected by the UE such that the ACK/NACK transmission (of duration 1 timeslot) commences within the first 0-255 chips after 7.5 slots following the end of the received HS-DSCH. The UE processing time is therefore maintained at 7.5 slots (5.0 ms) as the offset between DPCCH and HS-DPCCH varies. The ACK bit is sent on the first slot of the code multiple xed uplink HS-DPCCH. This leaves approximately 4.5 slots-512 chips (prop delay)-256 chips (HS-DPCCH offset) = 2.8 msec ($T_{\text{Node-B}}$) for Node-B to perform scheduler and signal processing functions.

Every first slot on the HS-DPCCH, chosen according to the parameters above, are reserved for ACK/NACK signaling. Other slots on the HS-DPCCH can be used for Quality Indicator transmission according to the measurement feedback cycle and offset parameter provided by UTRAN as described in section 8.2.2.2. All slots not used for ACK/NACK or Quality Indicator signaling are DTX'ed.

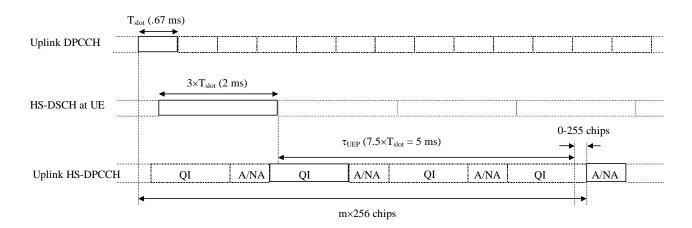


Figure 13. Timing structure at UE for UL HS-DPCCH control signaling

8.2.3 Detailed Structure TDD

This section describes the detailed structure of the TDD HSDPA uplink signalling.

8.2.3.1 HS-SICH

This section considers the structure of the HSDPA Shared Information Channel (HS-SICH). Three data fields have been identified that must be carried by the HS-SICH:

ACK / NAK

If the transport block set received by the UE on the associated HS-DSCH is received without error, then an acknowledgement (ACK) is sent to the NodeB. If an error is detected, a negative acknowledgement (NAK) is sent. The UE can detect an error in the transport block set via the CRC. The ACK/NAK signalling consists of only a single bit of information, and the following mapping is proposed:

Message	Bit Field Representation
ACK	1
NAK	0

Table 6: Mapping of ACK / NAK Message to Bit Field

• Quality Indicator

In order to assist the NodeB in selecting the appropriate modulation scheme and coding rate for the channel conditions currently being experienced by the UE, the UE sends quality information to the NodeB. This quality information is the recommended TFRC for the resources currently being employed by the NodeB for the UE, and consists of recommended Transport Block Set Size and Modulation Format fields for the TFRI. The quality indicator thus consists of 7 bits in total for 1.28 Mcps and 10 bits for 3.84 Mcps.

• TPC (1.28 Mcps TDD only)

The HS-SICH carries 2 TPC bits which are set by the UE based on the received HS-SCCH SIR. An outer loop algorithm for setting the target SIR is described in Section 8.1.3.5.

8.2.3.2 Uplink DPCH

An associated uplink DPCH is not required by the physical layer. However, if an associated downlink DPCH is established then the uplink DPCH may be used to support power control.

8.2.3.3 Timing relations for the HS-DSCH related Uplink Signalling

For 3.84 Mcps TDD, there is a minimum of 18 timeslots between HS-DSCH and the ACK / NACK signal on the associated HS-SICH. For 1.28 Mcps, there is a minimum of 8 timeslots between the HS-DSCH and associated HS-SICH allocation. The exact relationship between the HS-SCCH and the corresponding HS-SICH shall be signalled by higher layers.

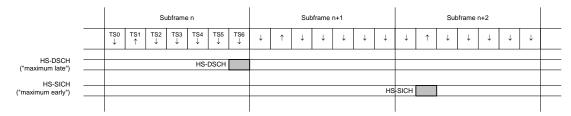


Figure 14. 1.28 Mcps HS-DSCH uplink control signaling

Figure 14 depicts an example of the timing structure for 1.28 Mcps HS-DSCH uplink control signalling.

8.2.3.4 HS-SICH Coding

8.2.3.4.1 1.28 Mcps TDD

The HS-SICH shall be mapped to Slot Format 5. The ACK/NAK field of the HS-SICH shall be repetition coded to 36 bits. The 6 bits of the Transport Block Size field of the quality indicator shall be coded to 32 bits using a (32, 6) 1st order Reed-Muller code. The 1 bit of the Modulation Format bit shall be repetition coded to 16 bits. The encoded fields are then multiplexed together and inserted into the slot payload. The mapping scheme is shown in the figure below.

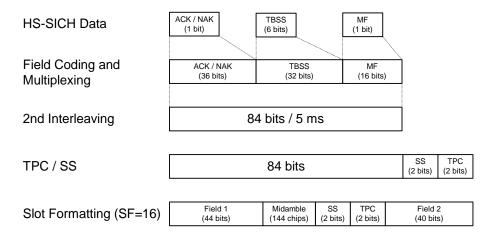


Figure 15: Coding and Multiplexing Scheme for the HS-SICH for 1.28 Mcps TDD

8.2.3.4.2 3.84 Mcps TDD

The HS-SICH shall use burst type 1. The ACK / NACK field shall be repetition coded to 36 bits. The 9 bits of the recommended transport block size and the 1 bit of the recommended modulation level are combined into a 10 bit field which is coded to 32 bits using the (32,10) 1st order Reed-Muller code (as used for TFCI). The encoded fields are multiplexed together and zero padded and inserted into the slot payload. The mapping scheme is shown in the figure below:

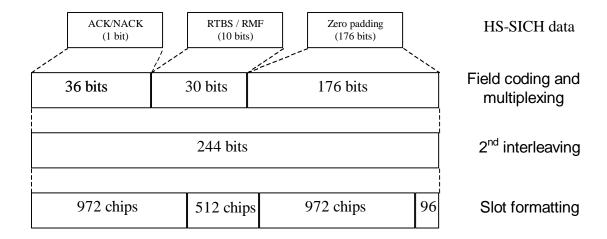


Figure 16: Coding and Multiplexing Scheme for HS-SICH for 3.84 Mcps TDD

8.2.3.5 Measurement Feedback Procedure

The quality indicator sent by the UE on the HS-SICH is a recommended TFRC. The recommended TFRC is based on the resources currently being employed by the NodeB for the UE and refers to the possible transport formats and modulation schemes as configured by higher layers. Hence the quality indicator consists only of the Transport Block Set Size and Modulation Format fields of the TFRI. The UE adopts the same mapping table for these fields as does the NodeB.

The reporting procedure is as follows:

- 1. The UE receives a message on a HS-SCCH telling it, amongst other things, which resources have been allocated to it for the next associated HS-DSCH transmission.
- 2. The UE reads the HS-DSCH transmission, and makes whatever quality measurements on this as are deemed necessary in order for it to be able to make a TFRC recommendation.
- 3. Based on the acquired quality information, the UE selects a combination of modulation format and transport block set size that it estimates would give it the highest throughput for the allocated resources whilst still meeting a specified threshold BLER. The threshold BLER would be defined identically to that proposed in section 8.2.2.2.2.
- 4. The UE reports the most recently derived recommended modulation format and transport block set size to the NodeB in the next available HS_SICH.
- 5. The NodeB can use the TFRC recommendation at its discretion. If the resources that the NodeB allocates to the UE for the next HS-DSCH transmission are changed, then the NodeB must re-interpret the TFRC recommendation for the new resource allocation.

8.2.3.6 HS-SICH Power Control

The transmit power of the HS-SICH shall be set by the UE according to the procedures described below. In the case that a NAK is being transmitted on the HS-SICH, the UE shall apply a power offset to the transmit power of the entire HS-SICH. This power offset shall be signalled by higher layers.

For 1.28 Mcps TDD, TPC commands are mandatory in the HS-SCCH for controlling the HS-SICH. On receipt of a TPC command in the HS-SCCH, the UE shall adjust the HS-SICH transmit power according to the power control step size specified by higher layers. However, for the first HS-SICH transmission following the first detected HS-SCCH transmission, or the first HS-SICH transmission following a gap of one or more detected HS-SCCH transmissions to the UE, the UE shall use open loop power control to set the HS-SICH transmit power for that transmission. In this case, the transmit power of the HS-SICH, $P_{\rm HS-SICH}$, shall be calculated using the following equation:

$$P_{HS-SICH} = L_{P-CCPCH} + PRX_{HS-SICH,des}$$

where $L_{P\text{-}CCPCH}$ is the measured pathloss from the NodeB (based on the P-CCPCH received power level) and PRX_{HS-SICH,des} is the desired receive power level on the HS-SICH when an ACK is being transmitted, which shall be signalled to the UE by higher layers.

8.2.3.7 Establishment and Maintenance of HS-SICH Synchronisation

8.2.3.7.1 1.28 Mcps

The initial transmit timing for the HS-SICH shall be taken from that of the associated uplink DPCH. The UE shall then adjust the timing of the HS-SICH according to SS commands transmitted to it on the HS-SCCH. The step size for these commands shall be signalled to the UE by higher layers. In the case that there is a gap of one or more subframes during which no HS-SCCH transmissions, and thus no SS commands, are received by the UE, the UE shall adjust the timing of the HS-SICH according to SS commands received on the associated downlink DPCH until such time as another HS-SCCH transmission is received.

8.2.3.7.2 3.84 Mcps TDD

The UE may infer the timing for the HS-SICH from that of the associated uplink DPCH if one is available.

8.2.4 Other aspects

{This section should describe how the uplink signalling operates in soft-handoff mode etc.}

9 UE Capability

9.1 HS-DSCH UE capability parameters

9.1.1 FDD

The HS-DSCH UE capabilities are classified according to the following categories:

HS-DSCH	Maximum number	Minimum	Maximum number of	Total Number of soft
category	of HS-DSCH codes	inter-TTI	HS-DSCH transport-	channel bits
	received	interval	channel bits that can	
			be received within an	
			HS-DSCH TTI	
Category 1	15	1	20456	172800
Category 2	10	1	14600	115200
Category 3	5	1	7300	57600
Category 4	5	2	7300	28000
Category 5	5	3	7300	19200
Category 6	10	1	14600	153600
Category 7	5	1	7300	96000
Category 8	5	1	7300	76800
Category 9	5	3	7300	48000
Category 10	5	3	7300	38400
Category 11	15	1	[28800]	172800

The downlink capability on DCH when HS-DSCH is in use (any of the Categories) is defined to be 64 kbits .

9.1.2 1.28 Mcps TDD

For 1.28 Mcps TDD, the allowed ranges for the HS-DSCH UE capability parameters are given in Table 7 below.

Table 7: 1.28 Mcps TDD UE Radio Access Capability Parameter Value Ranges

	UE radio access capability parameter	Value range	
RLC and MAC-	Total buffer size (kbytes)	50, 100	
HS parameters	Maximum number of AM RLC entities	6	
PHY parameters	HS-DSCH Category	Category 1, Category 2, Category 3, Category 4, Category 5, Category 6, Category 7, Category 8, Category 9, Category 10, Category 11, Category 12, Category 13	

The allowed HS-DSCH Category values are defined as follows :

Category	Maximum number of HS- DSCH codes per timeslot	Maximum number of HS- DSCH timeslots per TTI	Maximum number of HS- DSCH transport channel bits that can be received within an HS- DSCH TTI	Total number of soft channel bits	Support of SF=1 for HS-PDSCH
Category 1	8	5	7040	28160	No
Category 2	8	5	7040	56320	No
Category 3	8	5	7040	84480	No
Category 4	8	5	14080	56320	Yes
Category 5	8	5	14080	112640	Yes
Category 6	12	5	10228	40912	No
Category 7	12	5	10228	81824	No
Category 8	12	5	10228	122736	No
Category 9	12	5	14080	56320	Yes
Category 10	12	5	14080	112640	Yes
Category 11	16	5	14080	56320	Yes
Category 12	16	5	14080	112640	Yes
Category 13	16	5	14080	168960	Yes

9.1.3 3.84 Mcps TDD

For 3.84 Mcps TDD, the allowed ranges for the HS-DSCH UE capability parameters are given in Table 8 below.

Table 8: 3.84 Mcps TDD UE Radio Access Capability Parameter Value Ranges

	UE radio access capability parameter	Value range
RLC and MAC-	Total buffer size (kbytes)	Tbd
HS parameters	Maximum number of AM RLC entities	Tbd
PHY parameters	HS-DSCH Category	Category 1, Category 2, Category 3, Category 4, Category 5, Category 6, Category 7, Category 8, Category 9, Category 10, Category 11, Category 12, Category 13, Category 14, Category 15, Category 16, Category 17, Category 18, Category 19, Category 20, Category 21, Category 22, Category 23, Category 24, Category 25, Category 26, Category 27, Category 28, Category 29, Category 30, Category 31, Category 32, Category 33, Category 34, Category 35, Category 36, Category 37, Category 38

The allowed HS-DSCH Category values are defined as follows :

Category	Maximum number of HS- DSCH codes per timeslot	Maximum number of HS- DSCH timeslots per TTI	Maximum number of HS- DSCH transport channel bits that can be received within an HS- DSCH TTI	Total number of soft channel bits	Support of SF=1 for HS-PDSCH
Category 1	16	13	12000	64000	No
Category 2	16	13	12000	96000	No
Category 3	16	13	12000	144000	No
Category 4	16	13	36000	192000	No
Category 5	16	13	36000	288000	No
Category 6	16	13	36000	460000	No
Category 7	16	13	72000	384000	No
Category 8	16	13	72000	460000	No
Category 9	16	13	102000	460000	No
Category 10	16	13	12000	64000	Yes
Category 11	16	13	12000	96000	Yes
Category 12	16	13	12000	144000	Yes
Category 13	16	13	36000	192000	Yes
Category 14	16	13	36000	288000	Yes
Category 15	16	13	36000	460000	Yes
Category 16	16	13	72000	384000	Yes
Category 17	16	13	72000	460000	Yes
Category 18	16	13	102000	460000	Yes
Category 19	8	13	12000	64000	No
Category 20	8	13	12000	96000	No
Category 21	8	13	12000	144000	No
Category 22	8	13	36000	192000	No
Category 23	8	13	12000	64000	Yes
Category 24	8	13	12000	96000	Yes
Category 25	8	13	12000	144000	Yes
Category 26	8	13	36000	192000	Yes
Category 27	12	13	12000	64000	No
Category 28	12	13	12000	96000	No
Category 29	12	13	12000	144000	No
Category 30	12	13	36000	192000	No
Category 31	12	13	36000	288000	No
Category 32	12	13	72000	384000	No
Category 33	12	13	12000	64000	Yes
Category 34	12	13	12000	96000	Yes

Category 35	12	13	12000	144000	Yes
Category 36	12	13	36000	192000	Yes
Category 37	12	13	36000	288000	Yes
Category 38	12	13	72000	384000	Yes

9.2 Reference UE radio access capability combinations

9.2.1 FDD

Some reference combinations for HS-DSCH capabilities are shown in Table 9. These combinations are specific for HS-DSCH and are thus separate from Rel-99 combinations.

Table 9. UE radio access capability parameter combinations, DL HS-DSCH parameters

Reference combination	1.2 Mbps capability	3.6 Mbps capability	[7] Mbps capability	[10] Mbps capability
RLC and MAC-HS parameters				
Total buffer size (kbytes)	tbd	tbd	tbd	tbd
Maximum number of AM RLC entities	tbd	tbd	tbd	tbd
Phy parameters				
{Maximum number of HS-DSCH codes received, Minimum inter-TTI interval, Maximum number of HS-DSCH transport-channel bits that can be received within an HS-DSCH TTI}	{5, 3, 9600}		{10, 1, [15342]} or {10, 1, 19200}	or
Total number of soft channel bits	19200	57600	115200	172800

9.2.2 1.28 Mcps TDD

Reference combinations for HS-DSCH capabilities are shown in Table 10 below.

Table 10: 1.28 Mcps UE radio access capability parameter combinations, DL HS-DSCH parameters

Reference combination	1.4 Mbps Capability	2.0 Mbps Capability	2.8 Mbps Capability	
RLC and MAC-HS parameters				
Total buffer size (kbytes)	50	50	100	
Maximum number of AM RLC entities	6	6	6	
PHY parameters				
HS-DSCH Category	Category 1	Category 6	Category 11	

9.2.3 3.84 Mcps TDD

Reference combinations for HS-DSCH capabilities are shown in Table 11 below.

Table 11: 3.84 Mcps UE radio access capability parameter combinations, DL HS-DSCH parameters

Reference combination	1.2 Mbps Capability	3.6 Mbps Capability	7.2 Mbps Capability	10.2 Mbps capability
RLC and MAC-HS parameters				
Total buffer size (kbytes)	tbd	tbd	tbd	tbd
Maximum number of AM RLC entities	tbd	tbd	tbd	tbd
PHY parameters				
HS-DSCH Category	Category 19	Category 13	Category 16	Category 18

Annex A:

Requirements for the evaluation of techniques for High Speed Downlink Packet Access

The following considerations should be taken into account in the evaluation of the different techniques proposed for HSDPA.

- 1. The focus shall be on the streaming, interactive and background services. It should be noted that it may not be possible to simultaneously optimise the characteristics of HSDPA for all of the above traffic classes.
- 2. System performance improvement shall be obtained with the concomitant reduction in delay of service.
- 3. Priority shall be given to urban environments and then to indoor deployments. The techniques shall not be limited to these environments however.
- 4. The techniques accepted shall be optimised at speeds typical of urban environments but techniques should apply at other speeds also. Full mobility shall be supported, i.e., mobility should be supported for high-speed cases also, but optimisation should be for low-speed to medium-speed scenarios.
- 5. Features or group of features considered should demonstrate significant incremental gain.
- 6. Features accepted shall provide the benefit at reasonable cost to the operators. The value added per feature should be considered in the evaluation.
- 7. The techniques should be compatible with advanced antenna and receiver techniques.
- 8. The techniques should take into account the impact on R99 networks both from a protocol and hardware perspective.
- 9. The choice of techniques (such as HARQ) shall take into account UE processing time and memory requirements.
- 10. The UE complexity shall be minimised for a given level of system performance.

An evolutionary philosophy shall be adopted as opposed to a revolutionary one in adopting new techniques and architectures.

Annex B: History

Change history							
Date	TSG#	TSG Doc.	CR	Rev	Subject/Comment	Old	New
08/03/02	RAN_15	RP-020255			Approved at TSG RAN #15 and placed under Change Control	-	5.0.0